

Silicon P-Channel Power MOSFET

Description

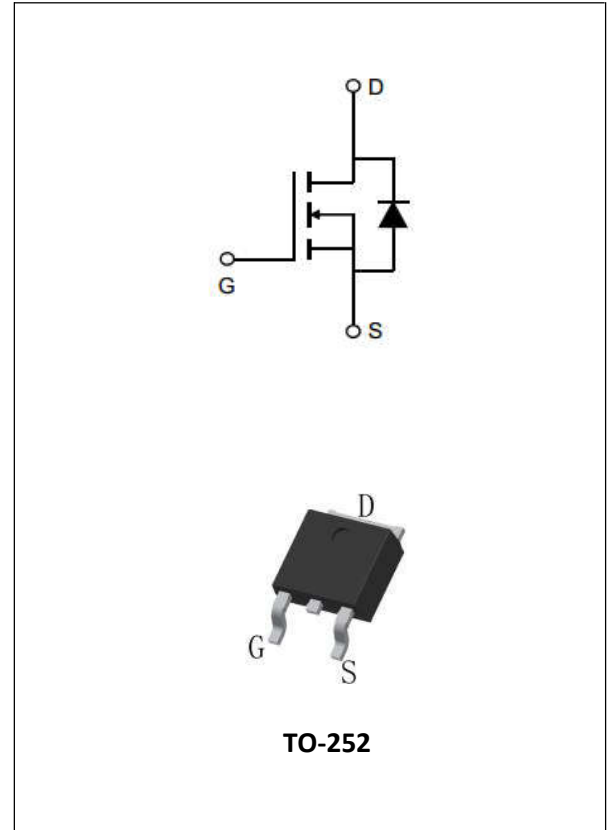
The MDT20P04D uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

KEY CHARACTERISTICS

- ① $V_{DS} = -40V, I_D = -20A$
- ② $R_{DS(ON)} < 35m\Omega @ V_{GS} = -10V$ $R_{DS(ON)} < 45m\Omega @ V_{GS} = -4.5V$
- ③ High density cell design for lower R_{dson}
- ④ Fully characterized avalanche voltage and current
- ⑤ Good stability and uniformity with high E_{AS}
- ⑥ Excellent package for good heat dissipation

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
Uninterruptible power supply



ORDERING INFORMATION

Ordering Codes	Package	Product Code	Packing
MDT20P04D	TO-252	MDT20P04D	Reel

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-20	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	-60	A
Maximum Power Dissipation($T_c=25^\circ C$)	P_D	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (TO-252)	$R_{\theta JC}$	3.0	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient (SOP-8)	$R_{\theta JA}$	57	$^\circ C/W$

Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.5	-2.4	V
Drain-Source On-State Resistance ^(Note 2)	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-10A$	-	29	35	m Ω
		$V_{GS}=-4.5V, I_D=-5A$	-	34	45	
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-15A$	-	10	-	S
Dynamic Characteristics ^(Note 3)						
Input Capacitance	C_{iss}	$V_{DS}=-20V, V_{GS}=0V,$ $f=1.0MHz$	-	930	-	pF
Output Capacitance	C_{oss}		-	85	-	pF
Reverse Transfer Capacitance	C_{rss}		-	35	-	pF
Switching Characteristics ^(Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-20V, R_L=-1\Omega,$ $V_{GS}=-10V, R_{GEN}=3\Omega$	-	8	-	ns
Turn-on Rise Time	t_r		-	4	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	32	-	ns
Turn-Off Fall Time	t_f		-	7	-	ns
Total Gate Charge	Q_g	$V_{DS}=-20V, I_D=-15A$ $V_{GS}=-10V$	-	25	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	7	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=-15A$	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
3. Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

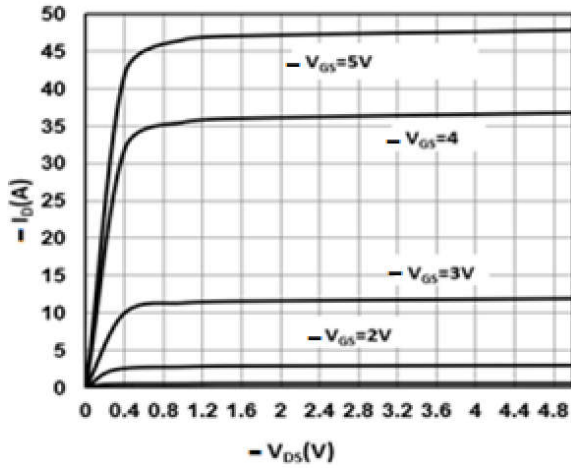


Figure 2 Transfer Characteristics

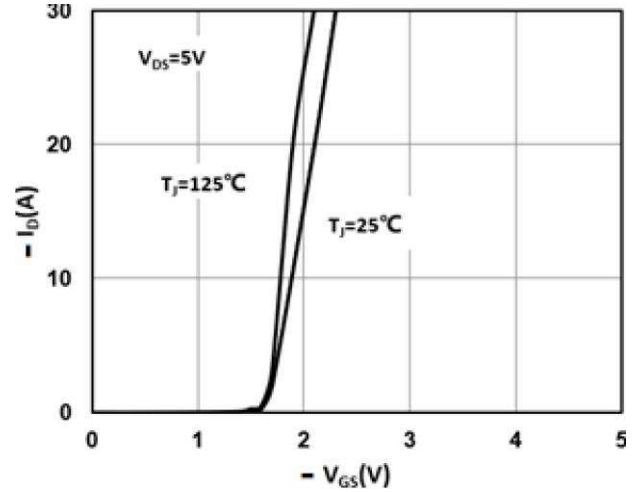


Figure 3 On-Resistance vs. I_D and V_{GS}

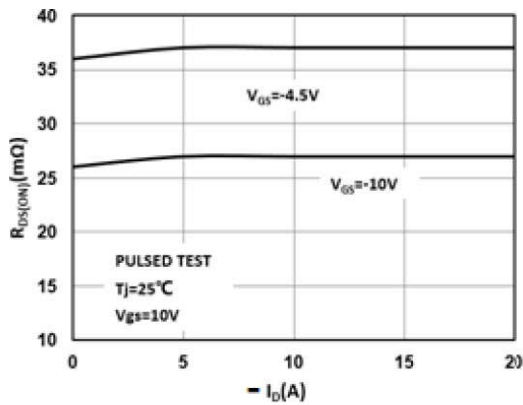


Figure 4 On-Resistance vs. Junction Temperature

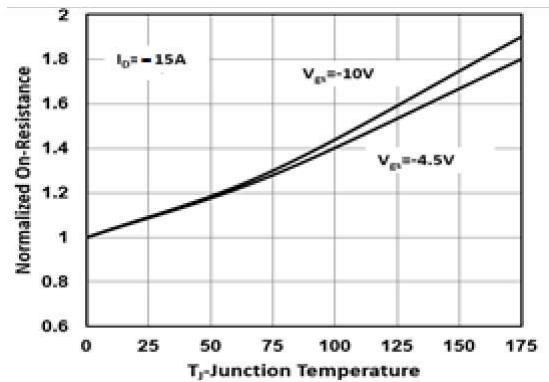


Figure 5 On-Resistance vs. V_{GS}

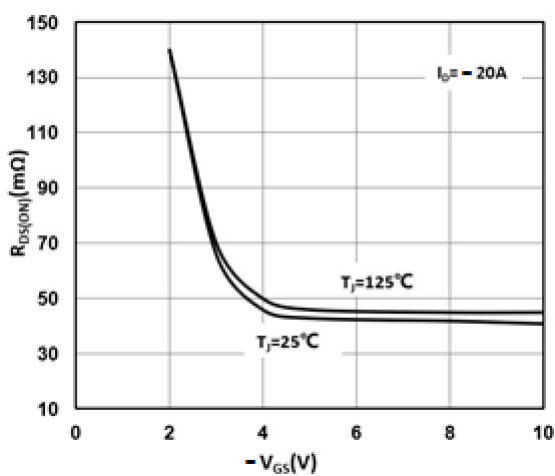


Figure 6 Body Diode Forward Voltage

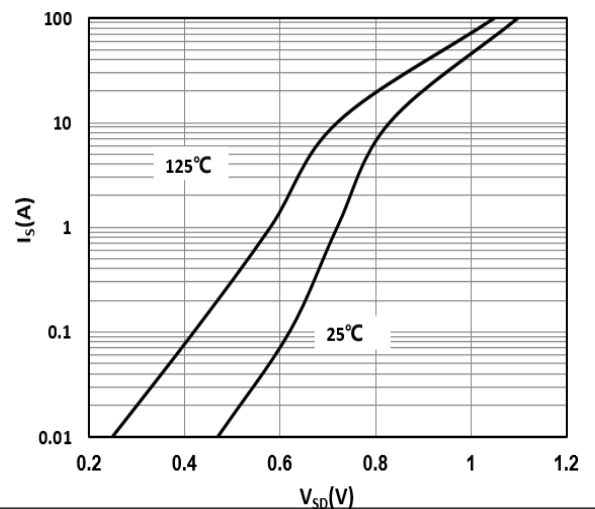


Figure 7 Gate-Charge Characteristics

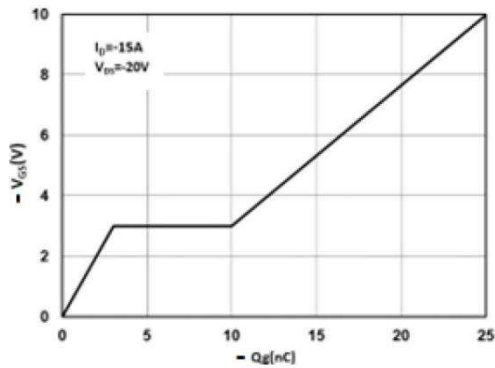


Figure 8 Capacitance Characteristics

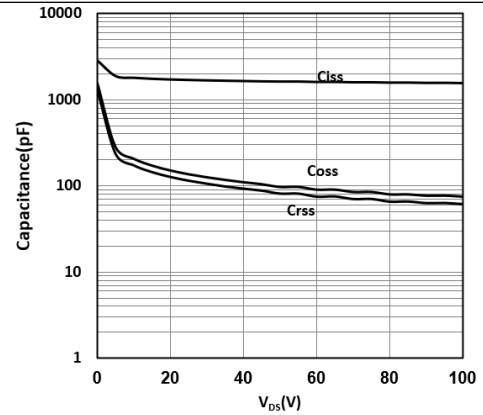


Figure 9 Maximum Forward Biased Safe Operation Area(TO-252)

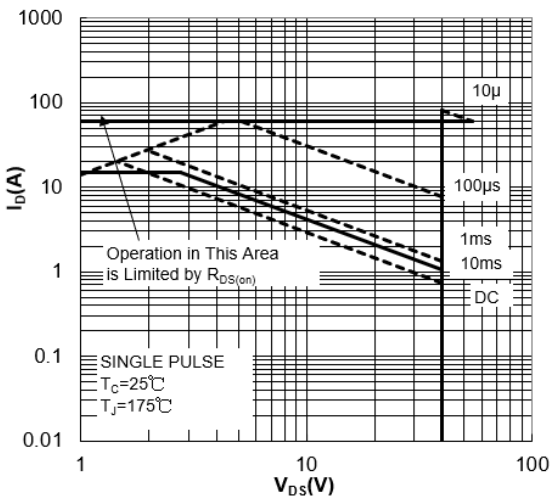


Figure 10 Single Pulse Power Rating Junction-to-Ambient(TO-252)

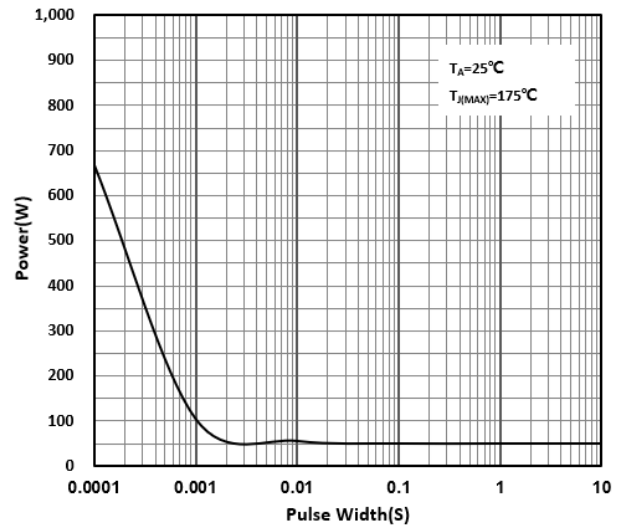


Figure 11 Normalized Maximum Transient Thermal Impedance(TO-252)

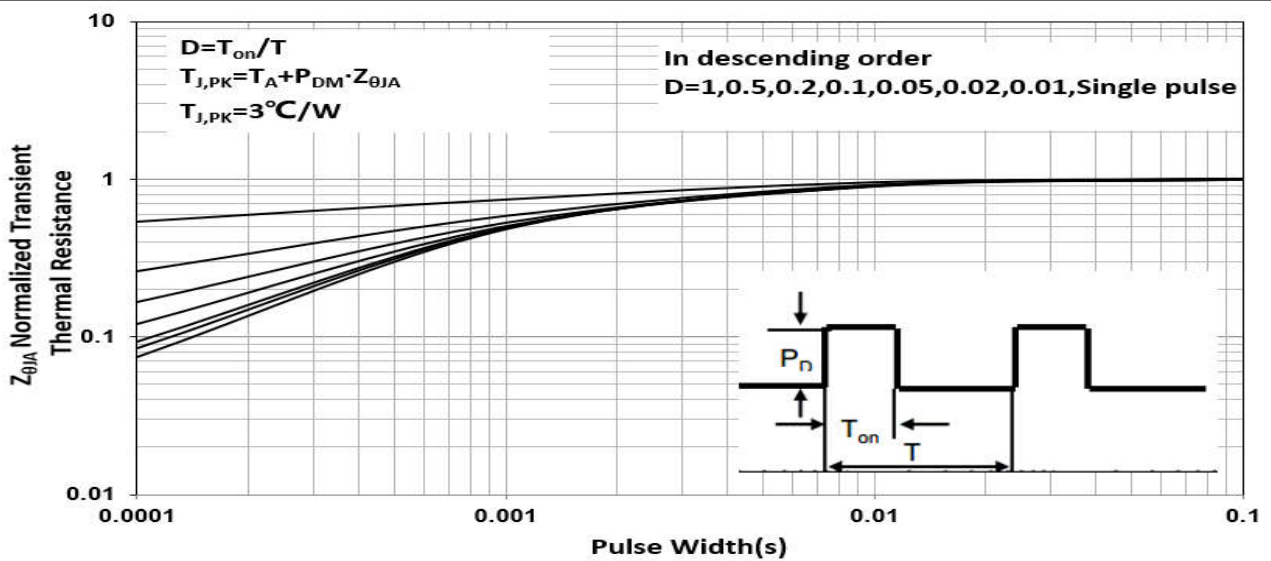


Figure 9 Maximum Forward Biased Safe Operation Area(SOP-8)

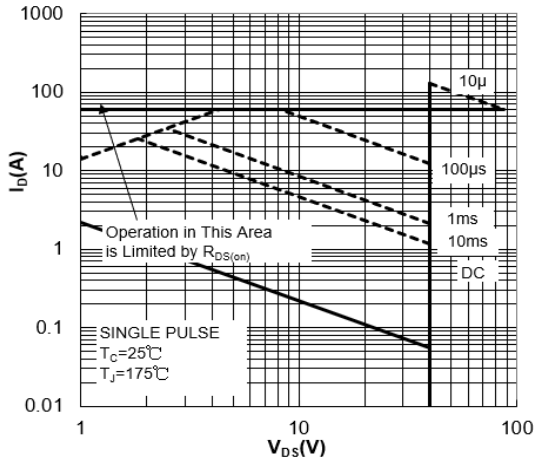


Figure 10 Single Pulse Power Rating Junction-to-Ambient(SOP-8)

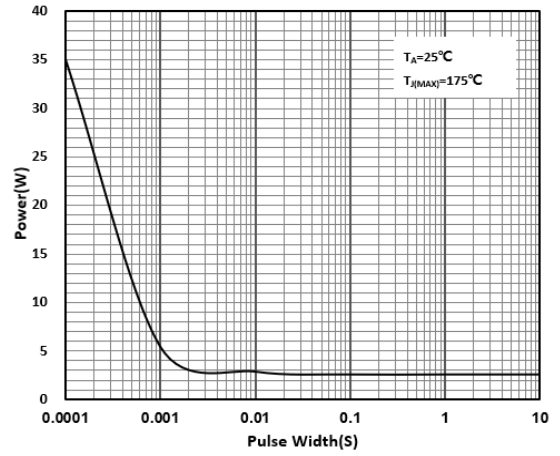
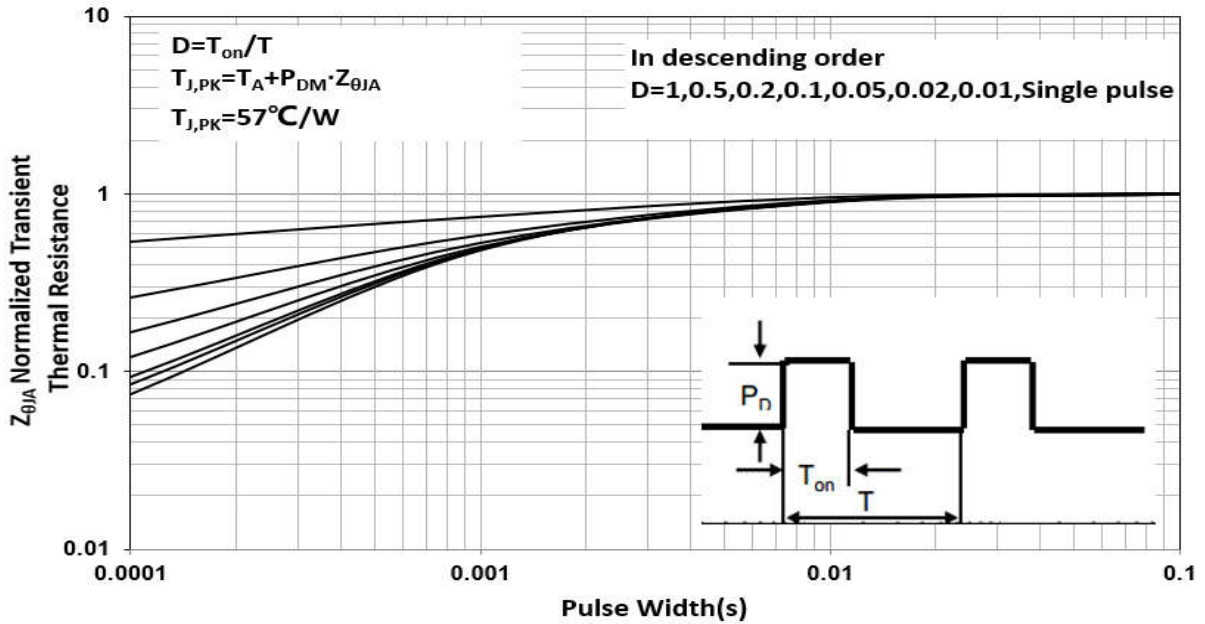
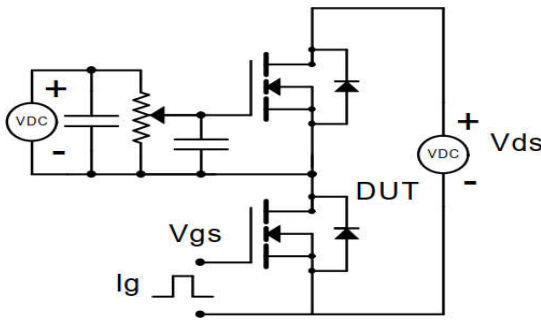
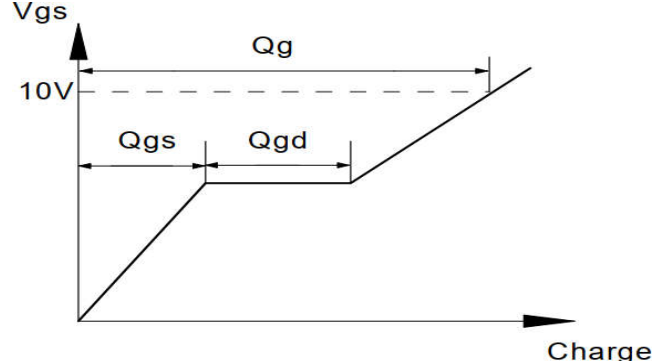
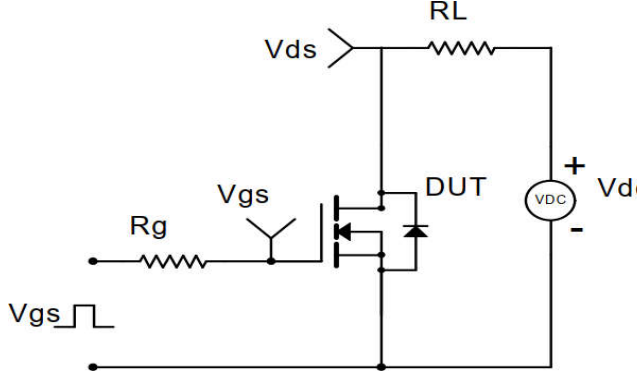
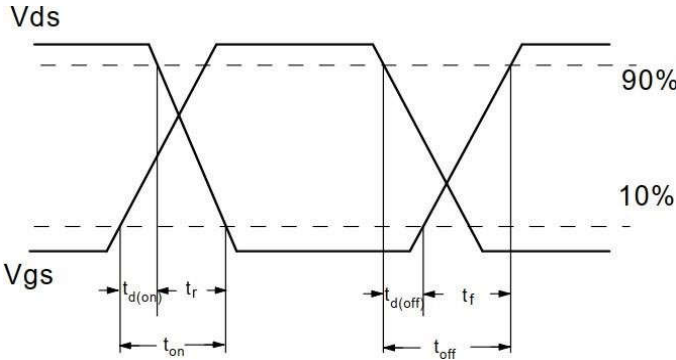
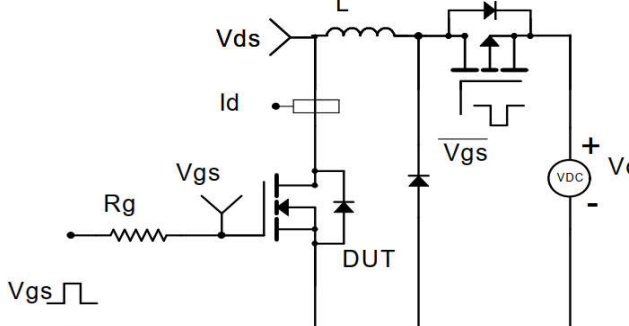
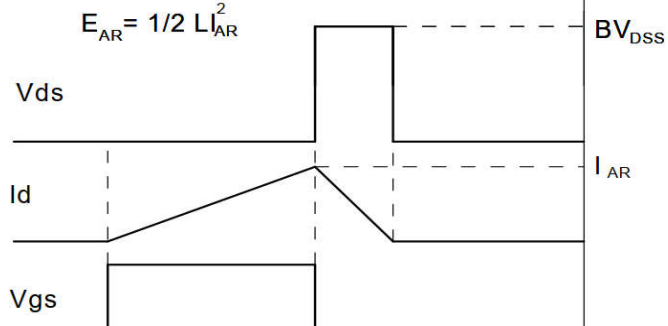
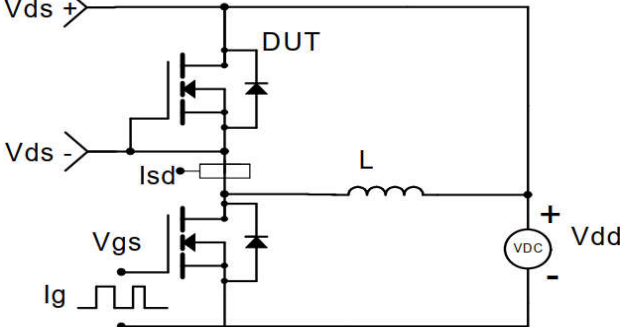
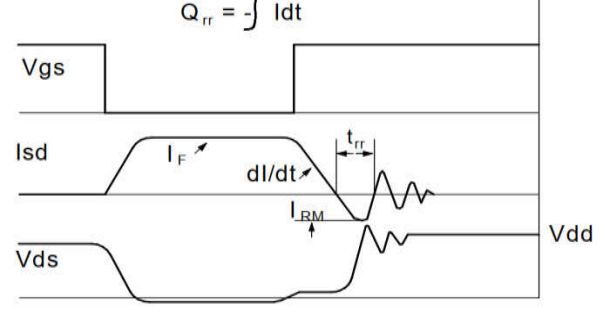


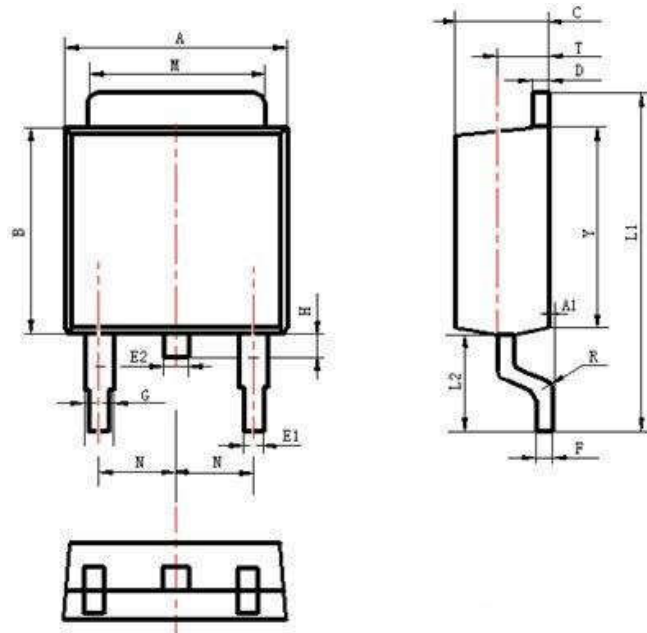
Figure 11 Normalized Maximum Transient Thermal Impedance(SOP-8)



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC source (VDC). The source is connected to ground. A current source (Ig) is also shown connected to the gate.</p>	 <p>The waveform shows Vgs on the y-axis and Charge on the x-axis. The gate voltage rises linearly to 10V, stays constant for a time interval Qgs, and then falls linearly. The total gate charge is Qg, and the gate discharge charge is Qgd.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to a load resistor (RL) and a DC source (VDC). The source is connected to ground.</p>	 <p>The waveforms show Vds and Vgs on the y-axis and time on the x-axis. Vgs is a square wave. Vds shows a trapezoidal shape during switching. Key time intervals are labeled: t_{d(on)}, t_{tr}, t_{on}, t_{d(off)}, t_{tr}, and t_{off}. The Vds levels are marked at 90% and 10%.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a diode. The source is connected to ground. A DC source (VDC) is connected to the drain.</p>	 <p>The waveforms show Vds, Id, and Vgs on the y-axis and time on the x-axis. Vgs is a square wave. Id shows a linear rise and fall. Vds shows a trapezoidal shape during switching. The energy stored in the inductor is given by the equation: $E_{AR} = 1/2 L I_{AR}^2$. The Vds levels are marked at BV_{DSS} and I_{AR}.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a pulse generator (Vgs) through a gate resistor (Rg). The drain is connected to an inductor (L) and a diode. The source is connected to ground. A DC source (VDC) is connected to the drain.</p>	 <p>The waveforms show Vgs, Isd, and Vds on the y-axis and time on the x-axis. Vgs is a square wave. Isd shows a linear rise and fall. Vds shows a trapezoidal shape during switching. The reverse recovery time (trr) is indicated. The equation for reverse recovery charge is given as: $Q_{rr} = -\int Idt$. Other parameters shown include I_F, dI/dt, and I_{RM}.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	6.30	6.90
A1	0	0.13
B	5.70	6.30
C	2.10	2.50
D	0.30	0.60
E1	0.60	0.90
E2	0.70	1.00
F	0.30	0.60
G	0.70	1.20
L1	9.60	10.50
L2	2.70	3.10
H	0.60	1.00
M	5.10	5.50
N	2.09	2.49
R	0.3	
T	1.40	1.60
Y	5.10	6.30

TO-252 Package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

CONTACT:

深圳市迈诺斯科技有限公司（总部）

地址：深圳市福田区华富街道田面社区深南中路4026号田面城市大厦22B-22C

邮编：518025

电话：0755-83273777