

54F/74F676 16-Bit Serial/Parallel-In, Serial-Out Shift Register

General Description

The 'F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is HIGH, information present on the parallel data (P_0 - P_{15}) inputs is entered on the falling edge of the Clock Pulse (\overline{CP}) input signal. When M is LOW, data is shifted out of the most significant bit position while information present on the Serial (SI) input shifts into the least significant bit position. A HIGH signal on the Chip Select (\overline{CS}) input prevents both parallel and serial operations.

Features

- 16-bit parallel-to-serial conversion
- 16-bit serial-in, serial-out
- Chip select control
- Slim 24 lead 300 mil package

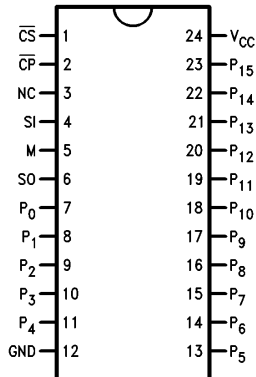
Commercial	Military	Package Number	Package Description
74F676PC		N24A	24-Lead (0.600" Wide) Molded Dual-In-Line
74F676SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F676DM (Note 2)	J24A	24-Lead (0.600" Wide) Ceramic Dual-In-Line
	54F676SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F676SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F676FM (Note 2)	W24C	24-Lead Cerpack
	54F676LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMOB, FMOB and LMOB.

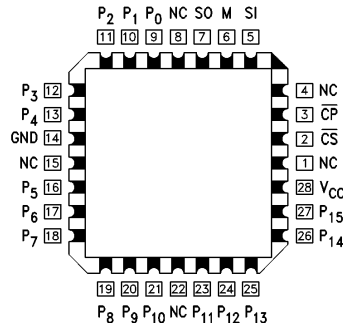
Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak



TL/F/9588-2

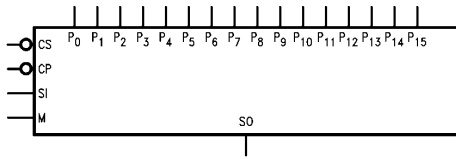
Pin Assignment
for LCC



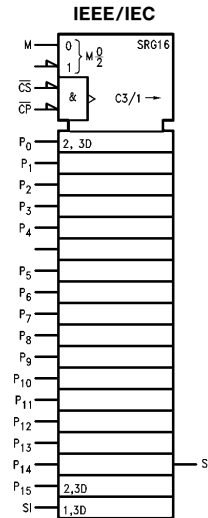
TL/F/9588-3

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Logic Symbols



TL/F/9588-1



TL/F/9588-4

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0 – P_{15}	Parallel Data Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{CS}	Chip Select Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
\overline{CP}	Clock Pulse Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
M	Mode Select Input	1.0/1.0	20 μ A/–0.6 mA
SI	Serial Data Input	1.0/1.0	20 μ A/–0.6 mA
SO	Serial Output	50/33.3	–1 mA/20 mA

Functional Description

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

HOLD—a HIGH signal on the Chip Select (\overline{CS}) input prevents clocking, and data is stored in the sixteen registers.

Shift/Serial Load—data present on the SI pin shifts into the register on the falling edge of \overline{CP} . Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load—data present on P_0 – P_{15} are entered into the register on the falling edge of \overline{CP} . The SO output represents the Q_{15} register output.

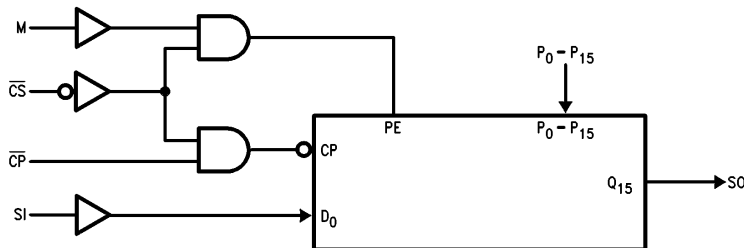
To prevent false clocking, \overline{CP} must be LOW during a LOW-to-HIGH transition of \overline{CS} .

Shift Register Operations Table

Control Input			Operating Mode
\overline{CS}	M	\overline{CP}	
H	X	X	Hold
L	L	\sim	Shift/Serial Load
L	H	\sim	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 \sim = HIGH-to-LOW Transition

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE® Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				
		74F 5% V _{CC}	2.7				
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			
I _{IH}	Input HIGH Current	54F		20.0	μA	Max	V _{IN} = 2.7V
		74F		5.0			
I _{BVI}	Input HIGH Breakdown Test	54F		100	μA	Max	V _{IN} = 7.0V
		74F		7.0			
I _{CEX}	Output HIGH Leakage Current	54F		250	μA	Max	V _{OUT} = V _{CC}
		74F		50			
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV, All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current			-60	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current			72	mA	Max	

AC Electrical Characteristics

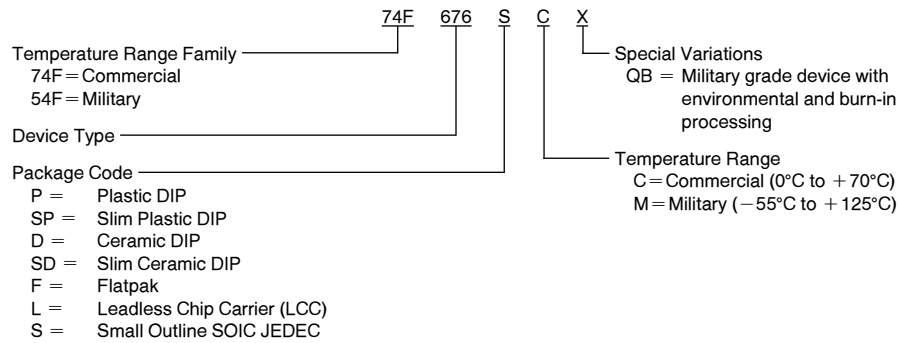
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	110		45		90		MHz
t _{PLH}	Propagation Delay CP to SI	4.5	9.0	11.0	4.5	17.0	4.5	12.0	ns
t _{PHL}	CP to SO	5.0	9.0	12.5	5.0	14.5	5.0	13.5	

AC Operating Requirements

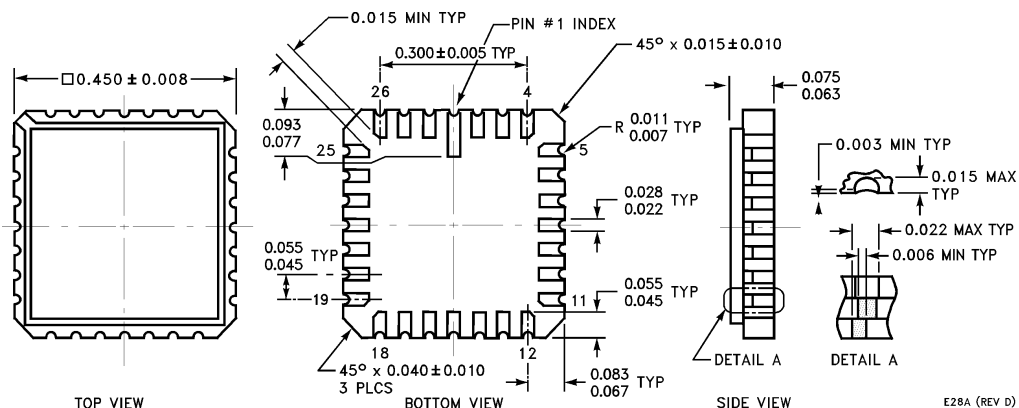
Symbol	Parameter	74F		54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V		T _A , V _{CC} = Mil		T _A , V _{CC} = Com		
		Min	Max	Min	Max	Min	Max	
t _s (H)	Setup Time, HIGH or LOW SI to CP	4.0		4.0		4.0		ns
t _s (L)	SI to CP	4.0		4.0		4.0		
t _h (H)	Hold Time, HIGH or LOW SI to CP	4.0		4.0		4.0		ns
t _h (L)	SI to CP	4.0		4.0		4.0		
t _s (H)	Setup Time, HIGH or LOW P _n to CP	3.0		3.0		3.0		ns
t _s (L)	P _n to CP	3.0		3.0		3.0		
t _h (H)	Hold Time, HIGH or LOW P _n to CP	4.0		4.0		4.0		ns
t _h (L)	P _n to CP	4.0		4.0		4.0		
t _s (H)	Setup Time, HIGH or LOW M to CP	8.0		8.0		8.0		ns
t _s (L)	M to CP	8.0		8.0		8.0		
t _h (H)	Hold Time, HIGH or LOW M to CP	2.0		2.0		2.0		ns
t _h (L)	M to CP	2.0		2.0		2.0		
t _s (L)	Setup Time, LOW CS to CP	10.0		12.0		10.0		ns
t _h (H)	Hold Time, HIGH CS to CP	10.0		10.0		10.0		
t _w (H)	CP Pulse Width HIGH or LOW	4.0		5.0		4.0		ns
t _w (L)	HIGH or LOW	6.0		9.0		6.0		

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

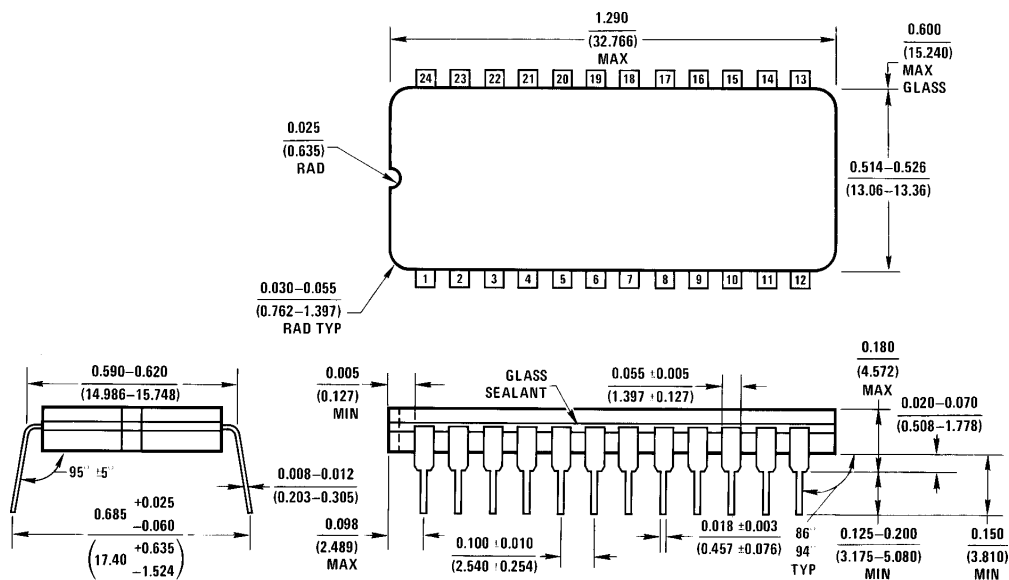


Physical Dimensions inches (millimeters)



**28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A**

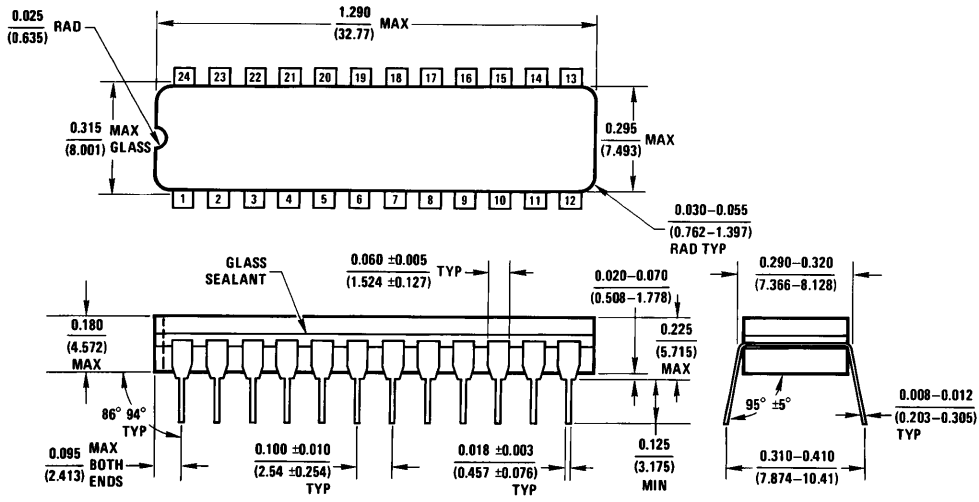
E28A (REV D)



**24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24A**

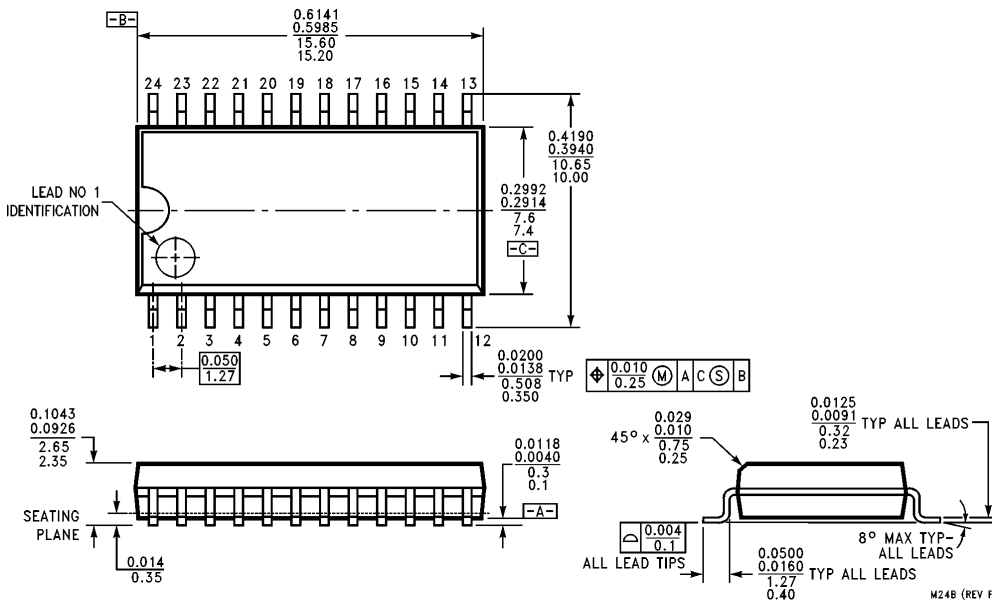
J24A (REV H)

Physical Dimensions inches (millimeters) (Continued)



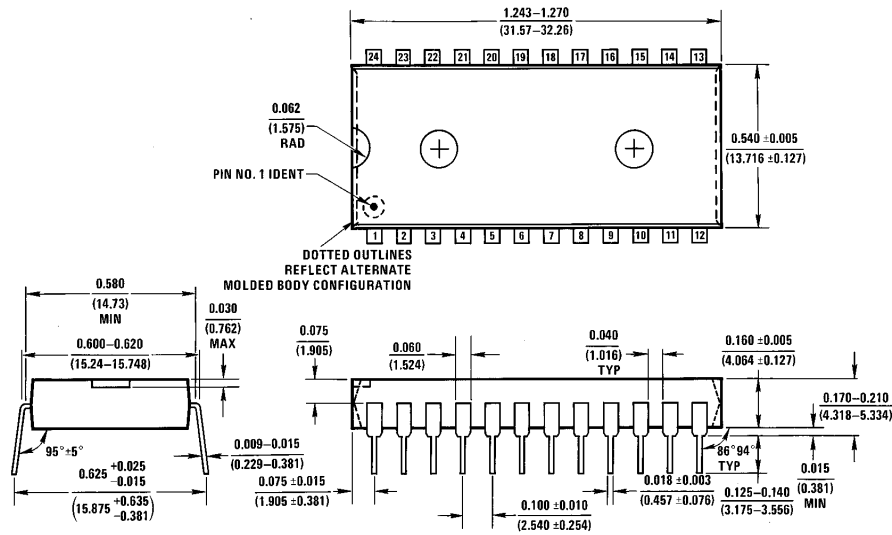
J24F (REV G)

24-Lead (0.300" Wide) Ceramic Dual-In-Line Package (SD)
NS Package Number J24F



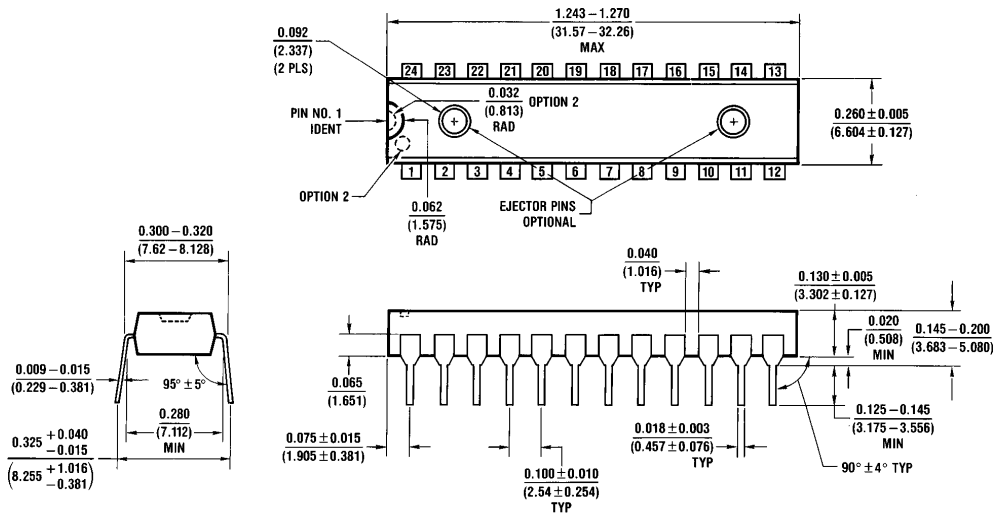
24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)



N24A (REV E)

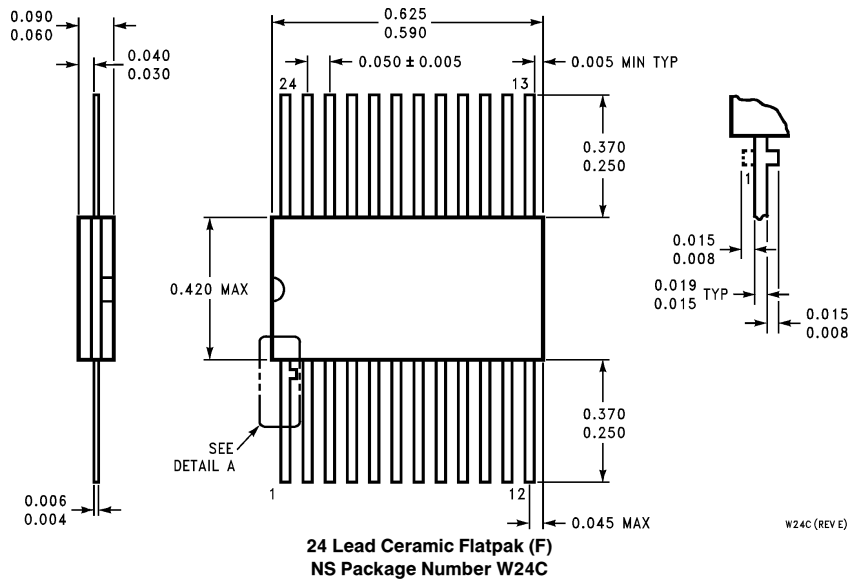
24-Lead (0.600" Wide) Molded Dual-In-Line Package (P)
NS Package Number N24A



N24C (REV F)

24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)



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