C3M0040120J1

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology
N-Channel Enchancement Mode

Features

- 3rd generation SiC MOSFET technology
- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

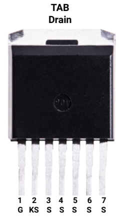
Benefits

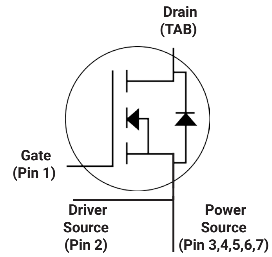
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Datacenter and Telecom Power Supplies
- EV Battery Chargers
- High voltage DC/DC converters
- Energy Storage Systems
- Solar Inverters

Package





Part Number	Package	Marking
C3M0040120J1	TO-263-7L XL	C3M0040120J1

Maximum Ratings (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain - Source Voltage	1200	V	V_{GS} = 0 V, I_D = 100 μA	
V_{GSmax}	Gate - Source Voltage (dynamic)	-8/+19	V	AC (f >1 Hz)	Note 1
V_{GSop}	Gate - Source Voltage (static)	-4/+15	V	Static	Note 2
I_D	Continuous Drain Current	64	A	V_{GS} = 15 V, T_C = 25˚C	Fig. 19
		42		V_{GS} = 15 V, T_C = 100˚C	
$I_{D(pulse)}$	Pulsed Drain Current	100	A	Pulse width t_P limited by T_{jmax}	
P_D	Power Dissipation	272	W	T_C=25˚C, T_J = 150 ˚C	Fig. 20
T_J , T_{stg}	Operating Junction and Storage Temperature	-40 to +150	˚C		
T_L	Solder Temperature	260	˚C	1.6mm (0.063") from case for 10s	

Note (1): When using MOSFET Body Diode V_{GSmax} = -4V/+19V
Note (2): MOSFET can also safely operate at 0/+15 V

Electrical Characteristics (T$_C$ = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.7	3.6	V	V_{DS} = V_{GS}, I_D = 9.2 mA	Fig. 11
			2.2		V	V_{DS} = V_{GS}, I_D = 9.2 mA, T_J = 150ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		40	53.5	mΩ	V_{GS} = 15 V, I_D = 33.3 A	Fig. 4, 5, 6
			60			V_{GS} = 15 V, I_D = 33.3 A, T_J = 150ºC	
g_{fs}	Transconductance		21		S	V_{DS}= 20 V, I_{DS}= 33.3 A	Fig. 7
			20			V_{DS}= 20 V, I_{DS}= 33.3 A, T_J = 150ºC	
C_{iss}	Input Capacitance		2900		pF	V_{GS} = 0 V, V_{DS} = 1000 V f = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		103				
C_{rss}	Reverse Transfer Capacitance		5				
E_{oss}	C_{oss} Stored Energy		60		μJ		Fig. 16
E_{ON}	Turn-On Switching Energy (Body Diode FWD)		339		μJ	V_{DS} = 800 V, V_{GS} = -4 V/+15 V, I_D = 33.3 A, $R_{G(ext)}$ = 2.5Ω, L= 99 μH,	Fig. 26
E_{OFF}	Turn Off Switching Energy (Body Diode FWD)		67				
$t_{d(on)}$	Turn-On Delay Time		13		ns	V_{DD} = 800 V, V_{GS} = -4 V/15 V $R_{G(ext)}$ = 2.5 Ω, I_D = 33.3 A, L= 99 Timing relative to V_{DS}, Inductive load	Fig. 27
t_r	Rise Time		18				
$t_{d(off)}$	Turn-Off Delay Time		22				
t_f	Fall Time		8				
$R_{G(int)}$	Internal Gate Resistance		3.5		Ω	f = 1 MHz, V_{AC} = 25 mV	
Q_{gs}	Gate to Source Charge		35		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 33.3 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		27				
Q_g	Total Gate Charge		94				

Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	5.5		V	V_{GS} = -4 V, I_{SD} = 20 A, T_J = 25°C	Fig. 8, 9, 10
		4.5		V	V_{GS} = -4 V, I_{SD} = 20 A, T_J = 150°C	
I_S	Continuous Diode Forward Current		44	A	V_{GS} = -4 V, T_C = 25˚C	Note 1
$I_{S, pulse}$	Diode pulse Current		100	A	V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	Note 1
t_{rr}	Reverse Recover time	11		ns	V_{GS} = -4 V, I_{SD} = 33.3 A, V_R = 800 V dif/dt = 9890 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	323		nC		
I_{rrm}	Peak Reverse Recovery Current	52		A		
t_{rr}	Reverse Recover time	17		ns	V_{GS} = -4 V, I_{SD} = 33.3 A, V_R = 800 V dif/dt = 1815 A/µs	Note 1
Q_{rr}	Reverse Recovery Charge	150		nC		
I_{rrm}	Peak Reverse Recovery Current	16		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.46	°C/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance From Junction to Ambient	40			

Typical Performance

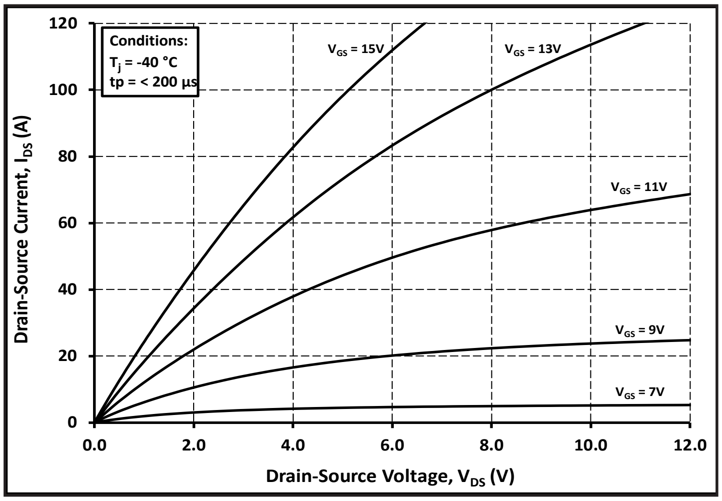


Figure 1. Output Characteristics T_J = -40 °C

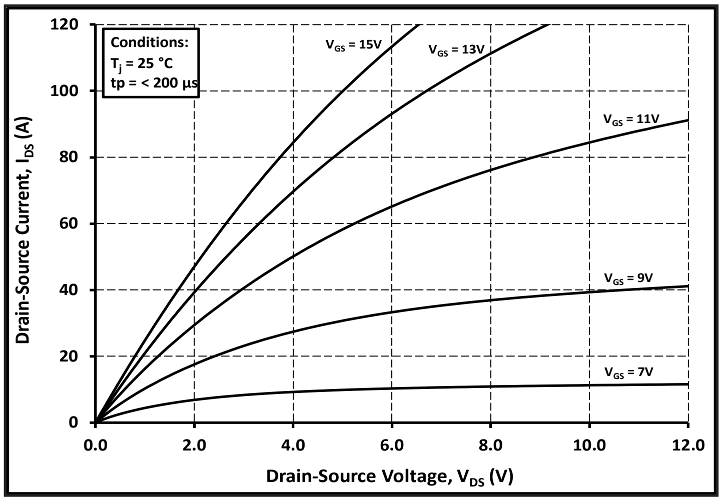


Figure 2. Output Characteristics T_J = 25 °C

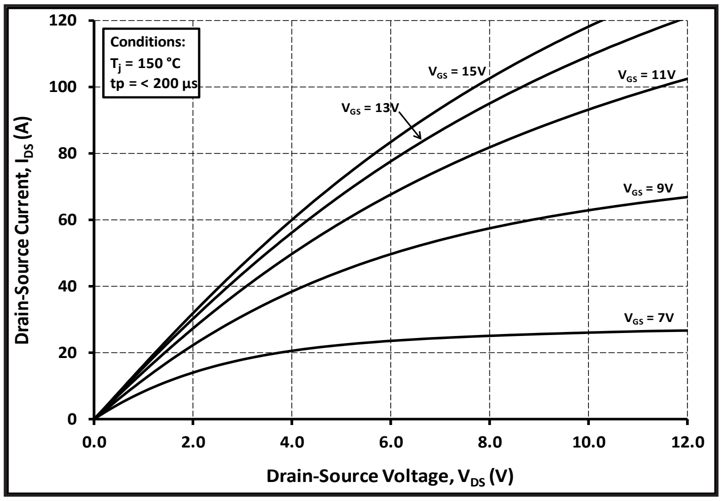


Figure 3. Output Characteristics T_J = 150 °C

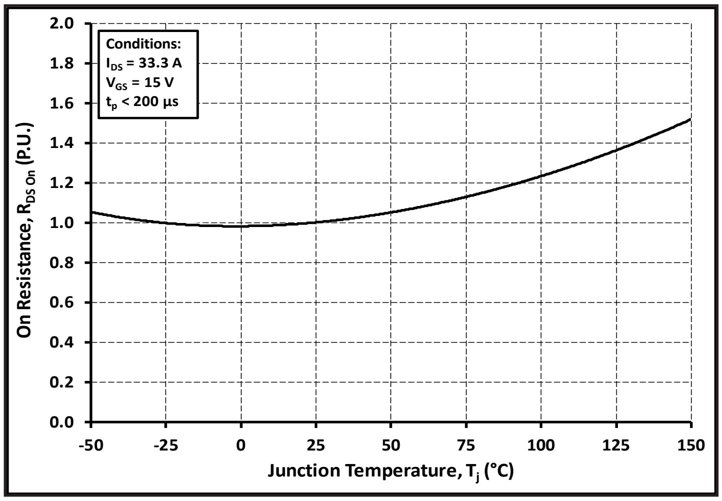


Figure 4. Normalized On-Resistance vs. Temperature

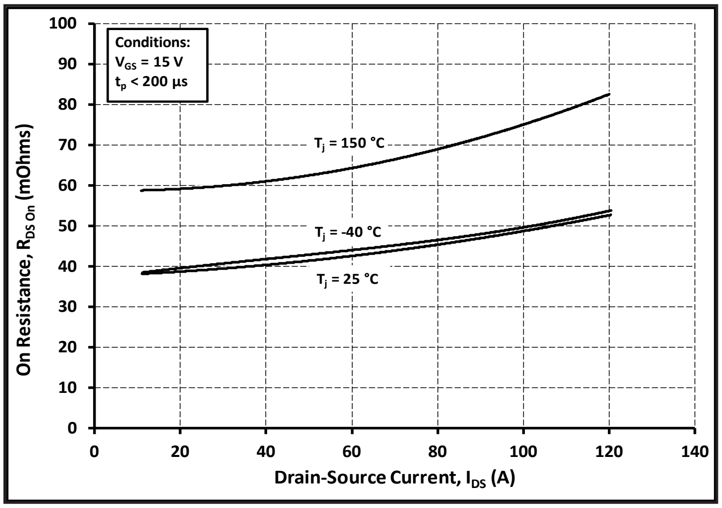


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

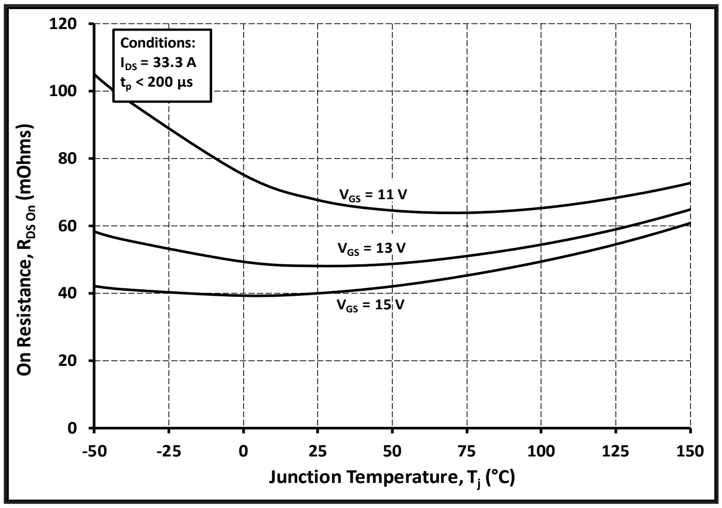


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

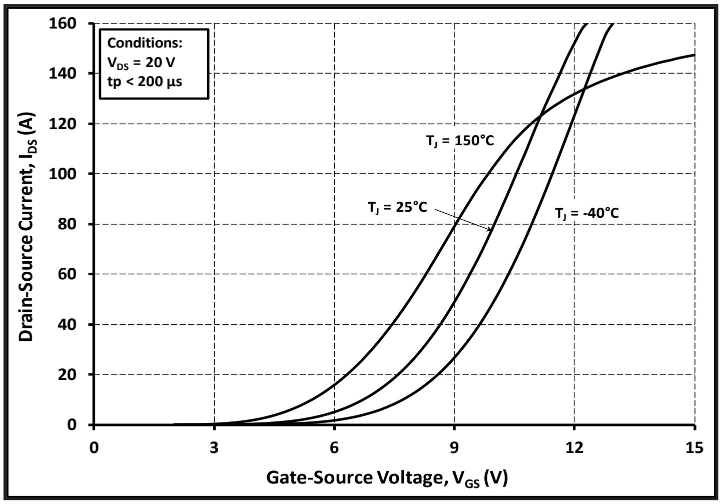


Figure 7. Transfer Characteristic for Various Junction Temperatures

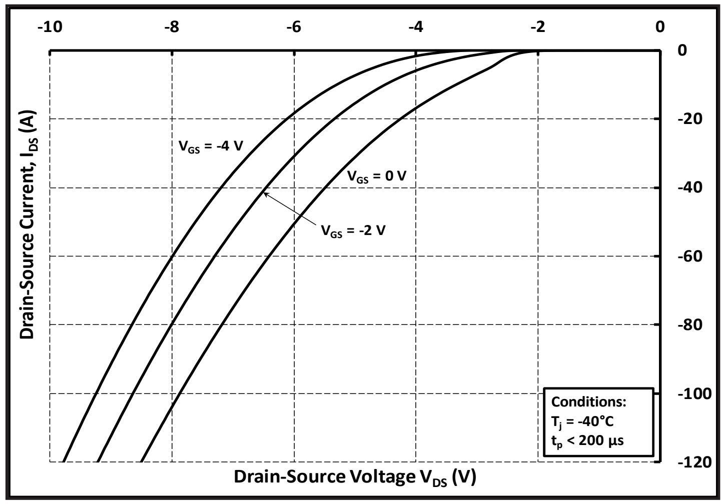


Figure 8. Body Diode Characteristic at -40 °C

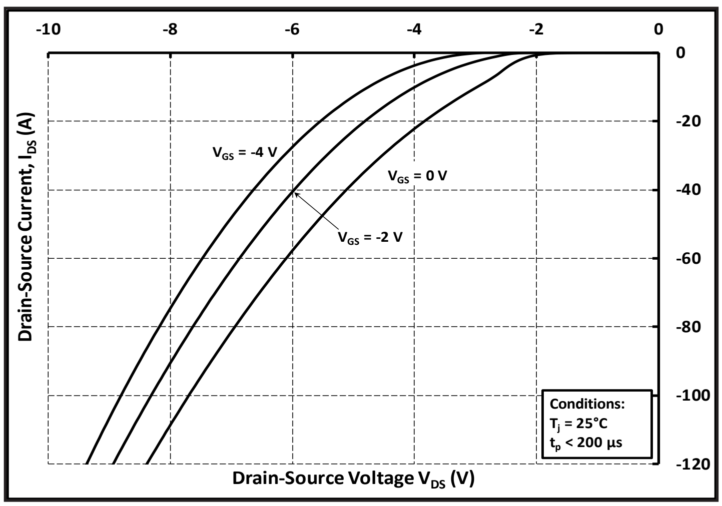


Figure 9. Body Diode Characteristic at 25 °C

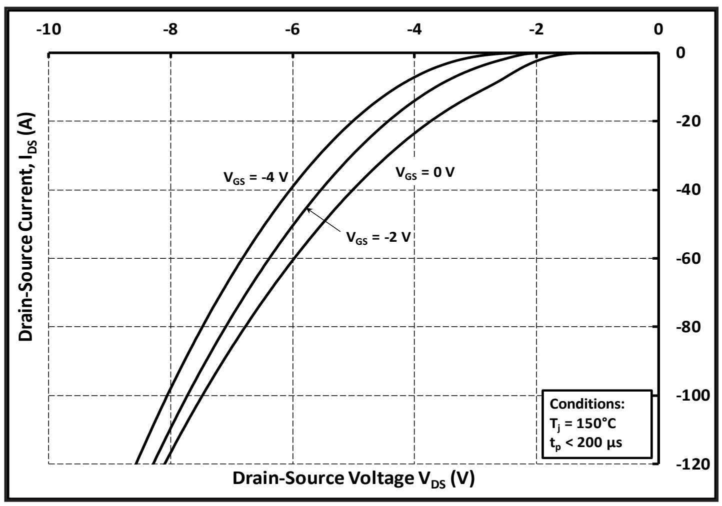


Figure 10. Body Diode Characteristic at 150 °C

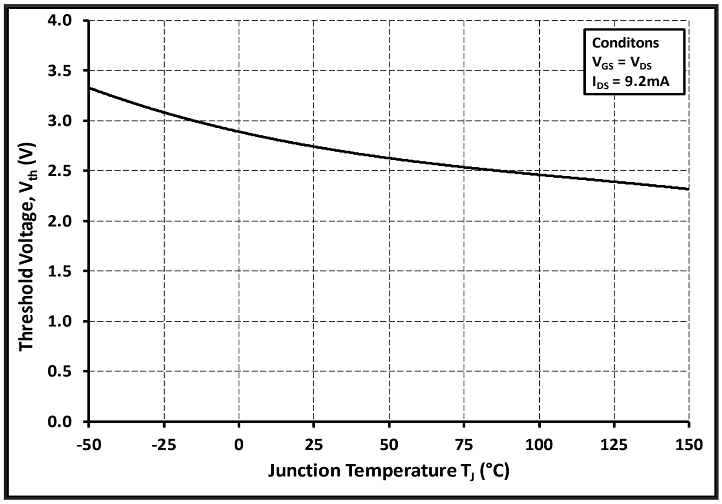


Figure 11. Threshold Voltage vs. Temperature

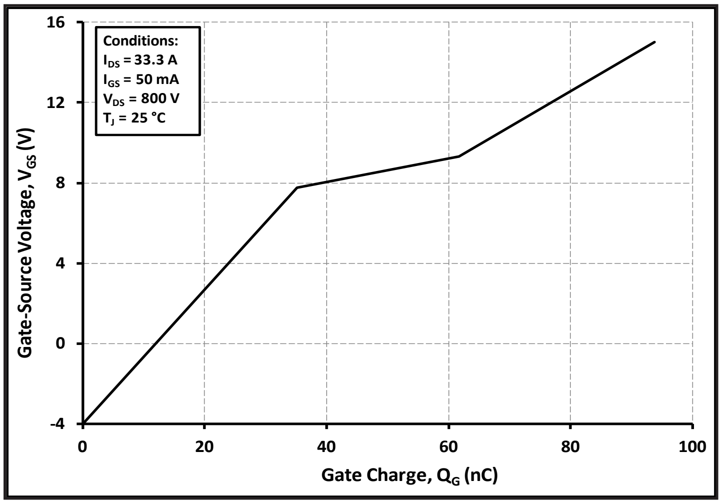


Figure 12. Gate Charge Characteristics

Typical Performance

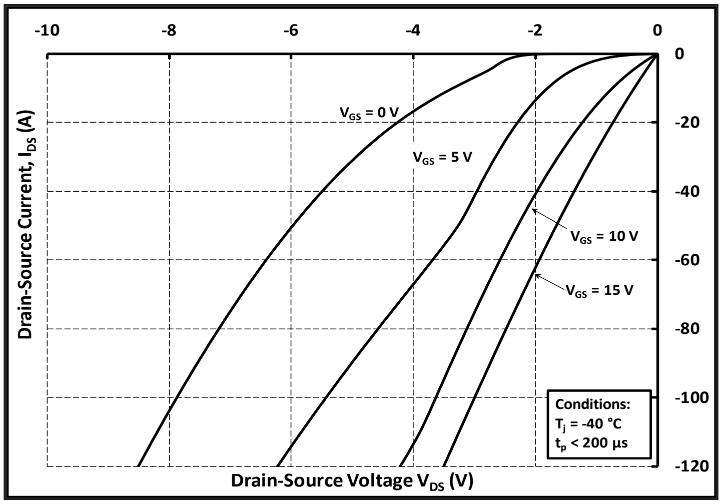


Figure 13. 3rd Quadrant Characteristic at -40 °C

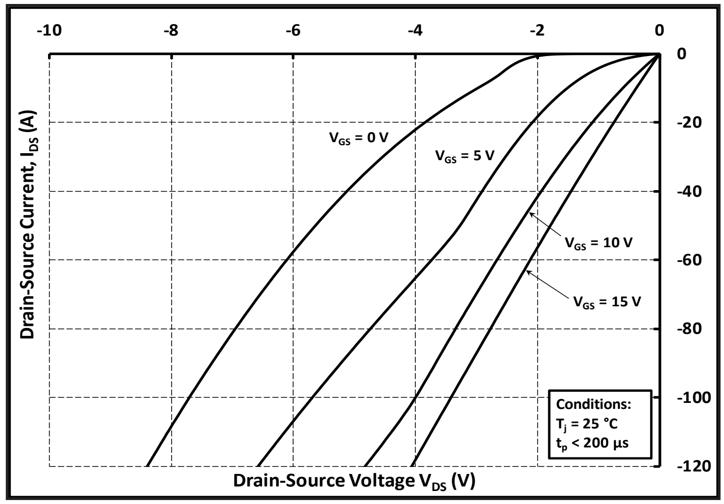


Figure 14. 3rd Quadrant Characteristic at 25 °C

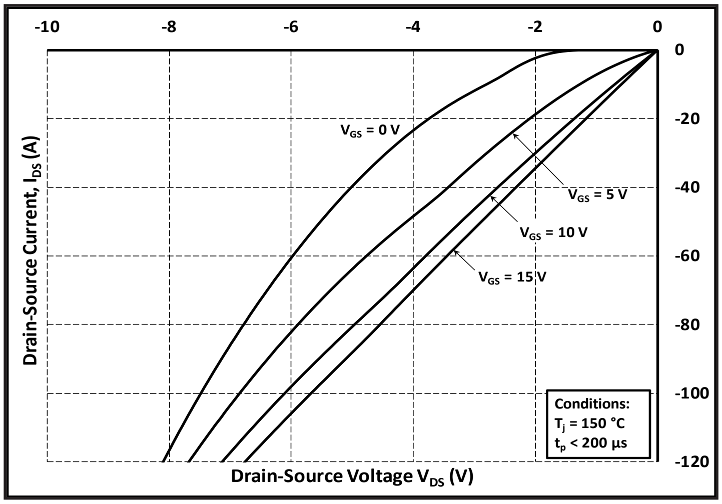


Figure 15. 3rd Quadrant Characteristic at 150 °C

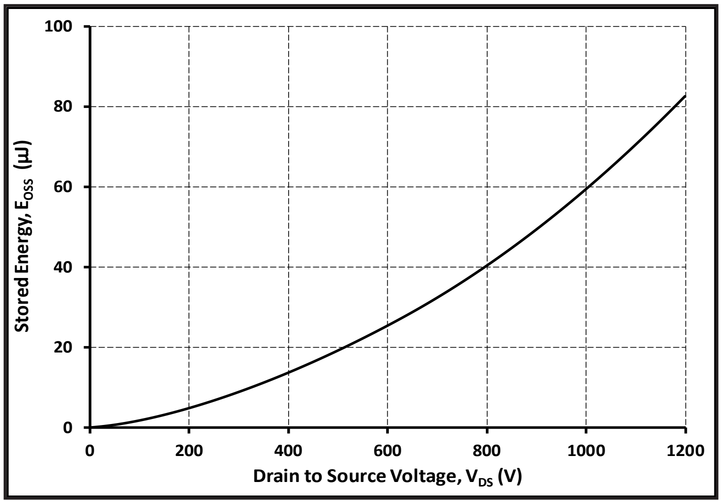


Figure 16. Output Capacitor Stored Energy

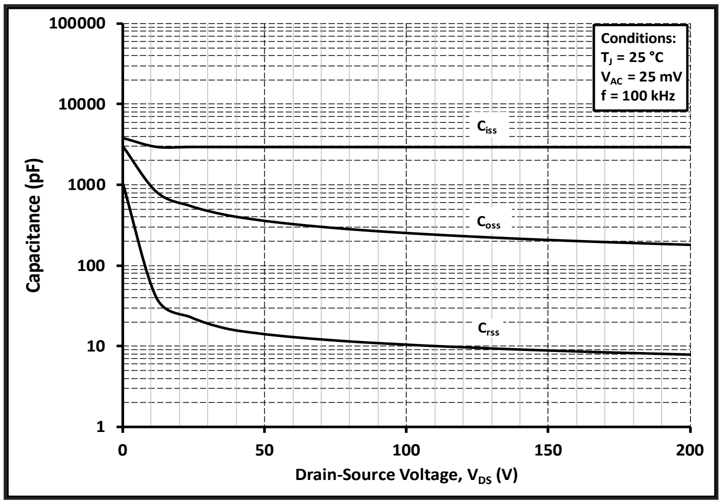


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

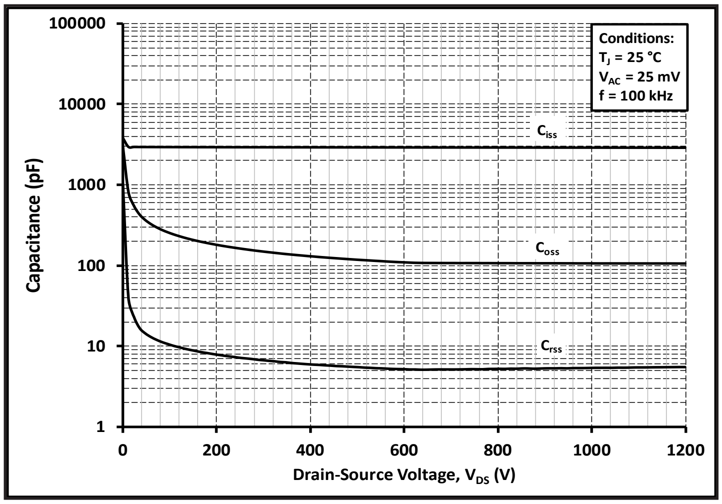


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

Typical Performance

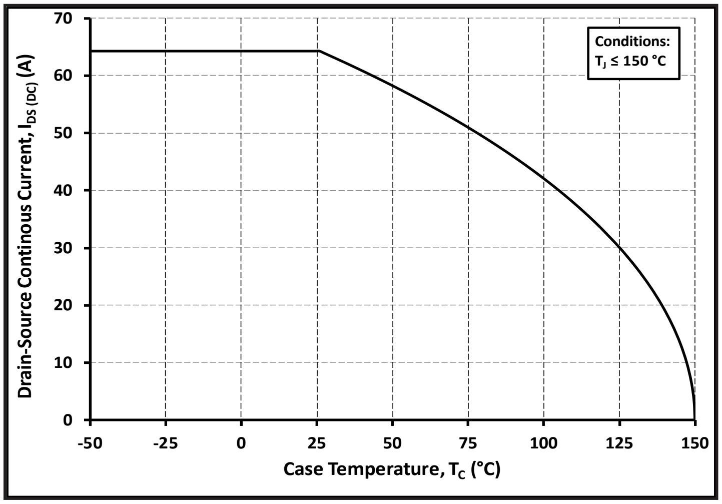


Figure 19. Continuous Drain Current Derating vs. Case Temperature

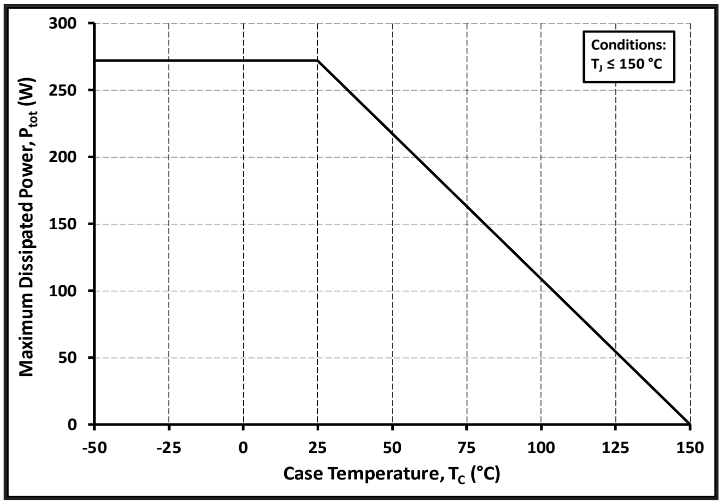


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

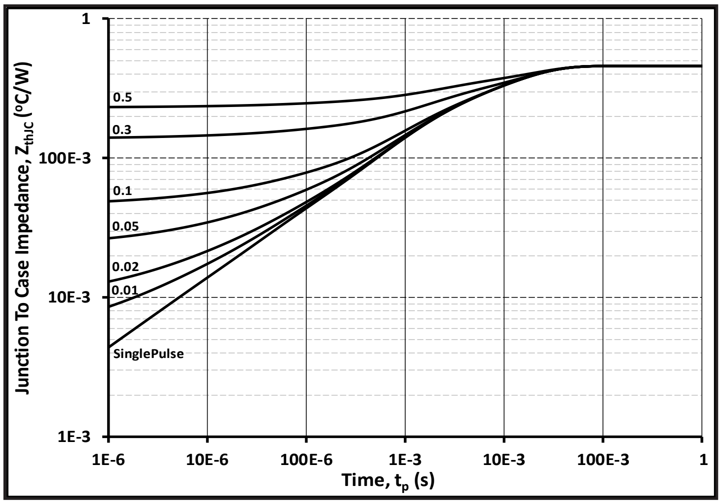


Figure 21. Transient Thermal Impedance (Junction - Case)

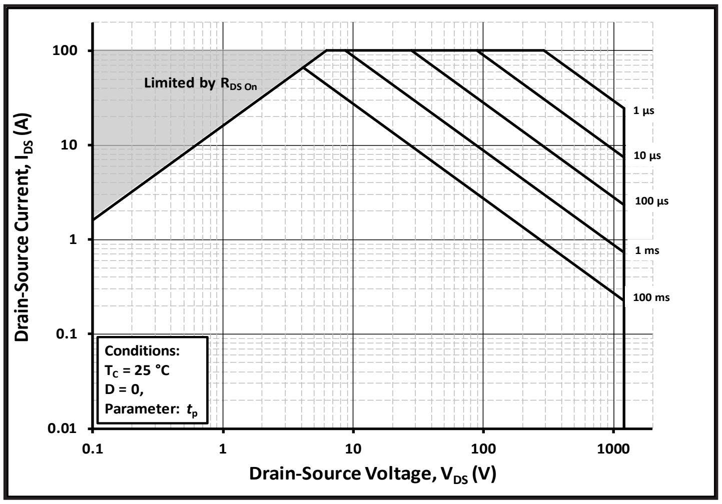


Figure 22. Safe Operating Area

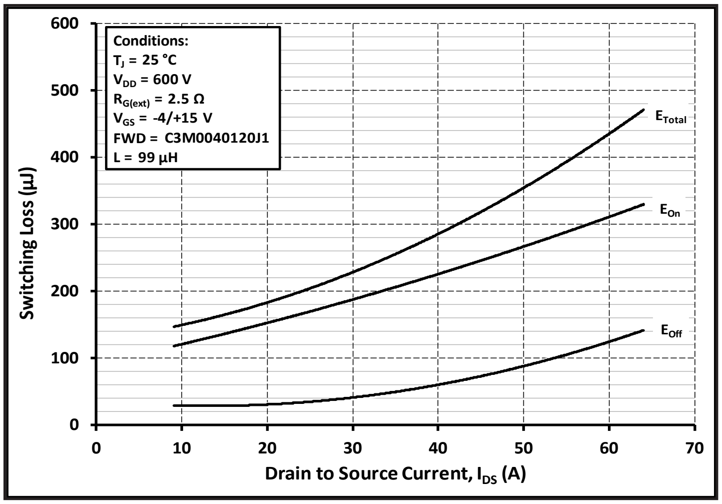


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

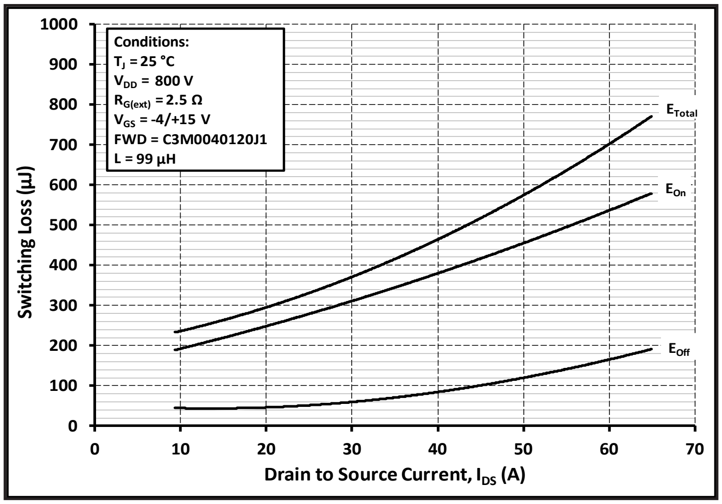


Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

Typical Performance

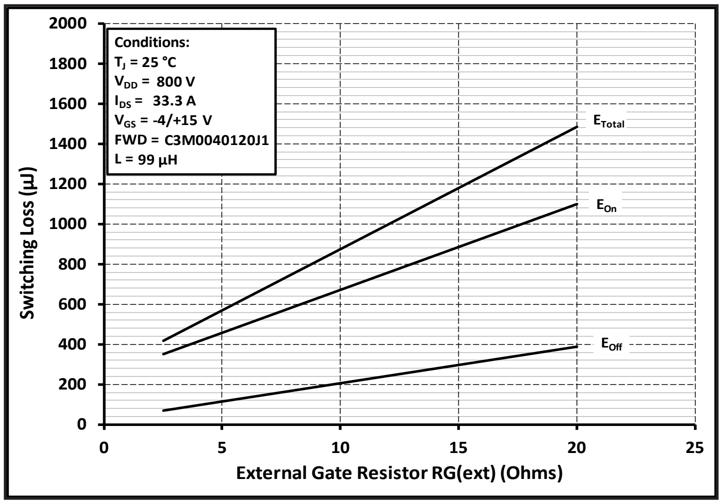


Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

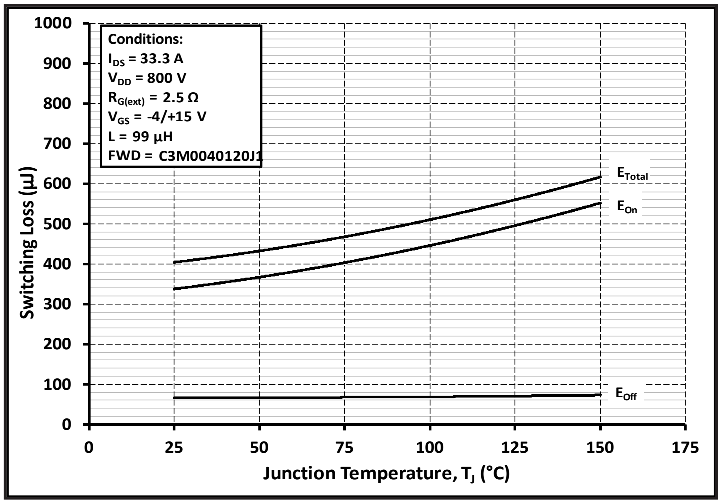


Figure 26. Clamped Inductive Switching Energy vs. Temperature

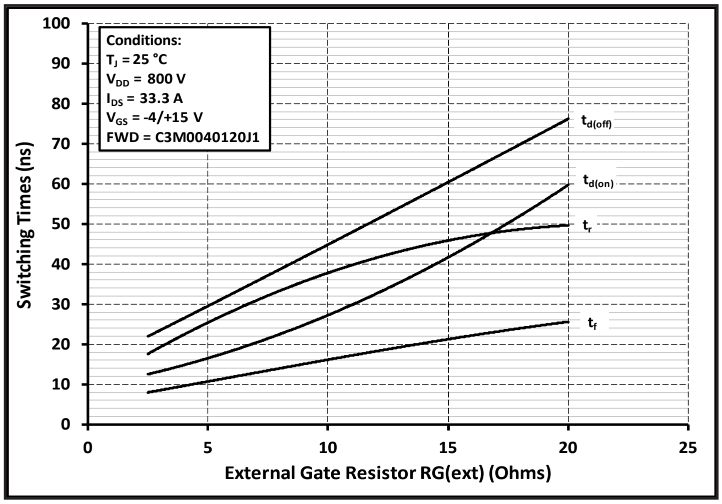


Figure 27. Switching Times vs. $R_{G(ext)}$

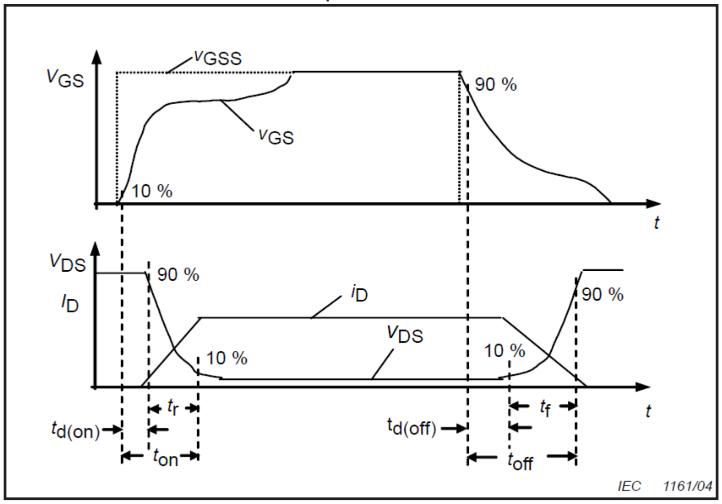


Figure 28. Switching Times Definition

Test Circuit Schematic

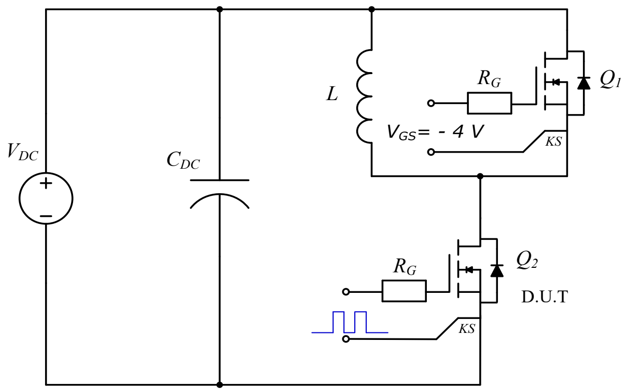
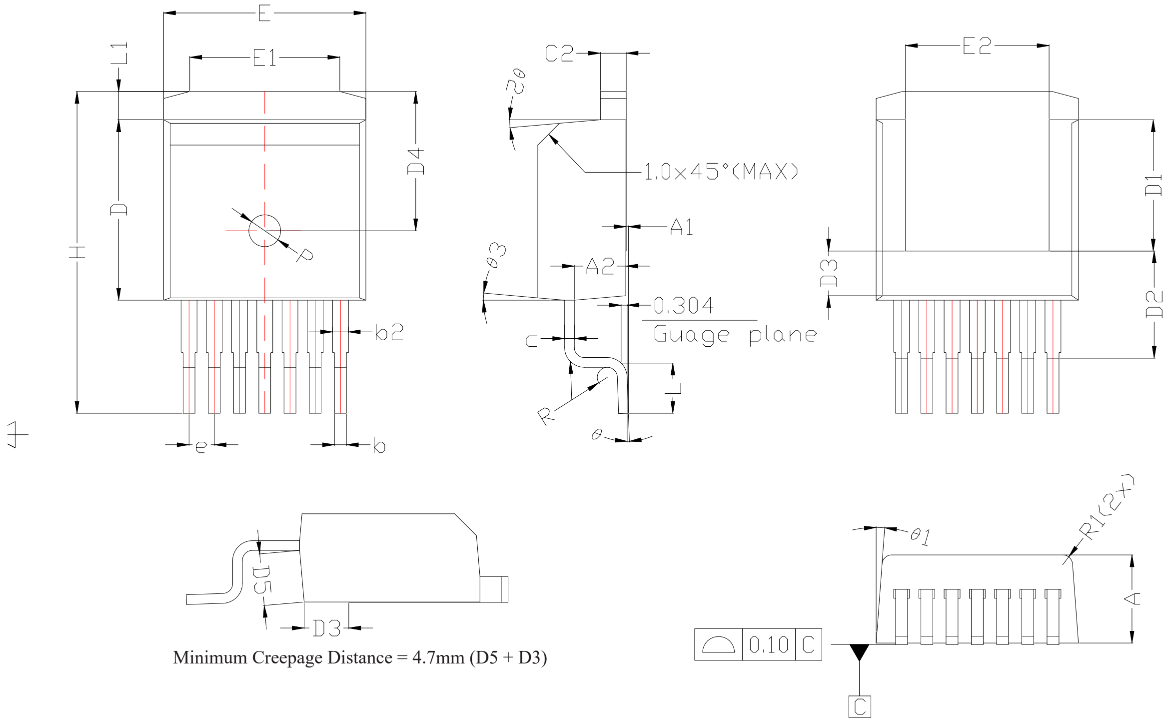


Figure 28. Clamped Inductive Switching
Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

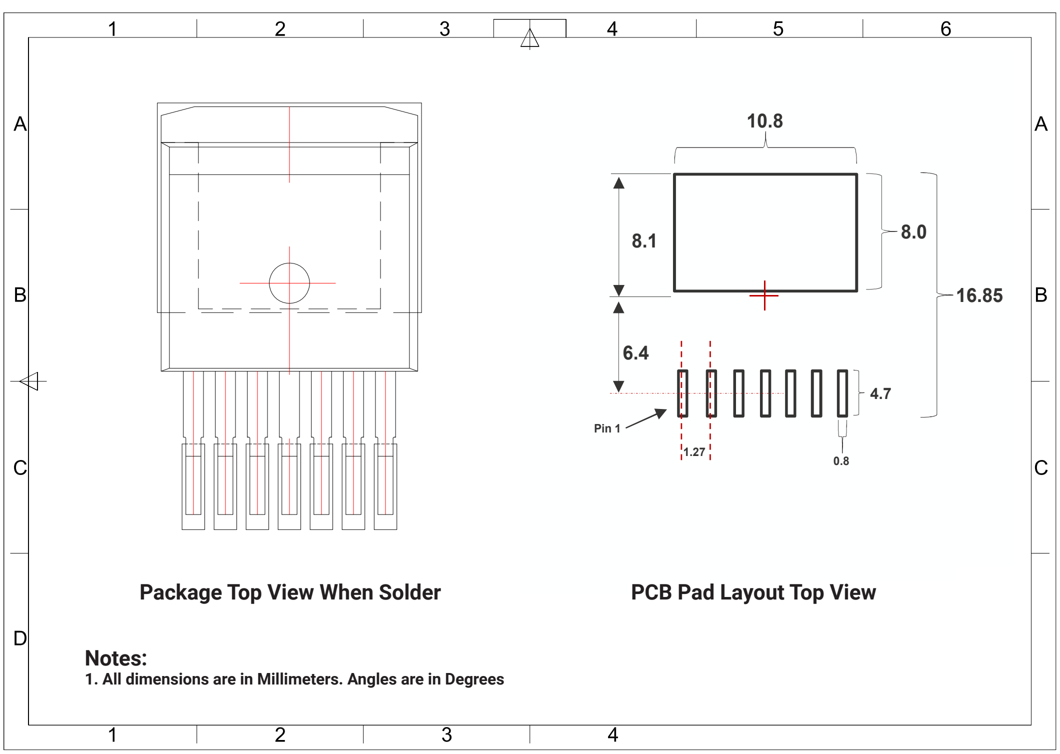
Package Dimensions

TO-263-7L XL



DIM	MIN	MAX	TYP
D	9.025	9.125	9.075
E	10.13	10.23	10.18
A	4.30	4.57	4.435
H	15.043	17.313	16.178
D1	6.50	6.70	6.60
E1	6.50	8.60	7.55
D2	5.39 REF.		
E2	6.778	7.665	7.223
D3	2.148	——	2.248
D4	7.00 REF.		
D5	2.555	——	2.605
A1	0	0.25	0.125
A2	2.595 REF.		
e	1.27 TYP.		
L	2.324	2.70	2.512
b	0.50	0.70	0.60
L1	0.968	1.868	1.418
b2	0.60	1.00	0.80
C2	1.17	1.37	1.27
c	0.281	0.481	0.381
R	0.506 REF.		
R1	0.50 REF.		
P	Ø1.60 REF.		
θ	0°	8°	4°
θ1	4.5°	5.5°	5°
θ2	4°	6°	5°
θ3	4°	6°	5°

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETER. ANGLES ARE IN DEGREE.
2. DIMENSION "D" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH SHALL NOT EXCEED 0.50 MM PER SIDE. DIMENSION "E" DOES NOT INCLUDE MOLD FLASH, GATE BURRS,THE GATE BURRS SHALL NOT EXCEED 0.30MM .
3. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKGE BOTOM. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTERMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH,BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
4. "b2" DIMENSION DON'T INCLUDE DAMBAR PROTRUSION.
5. THE VOID SHOULD BE CONTROL WITHIN 0.25MM.



Notes

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REACh Compliance
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