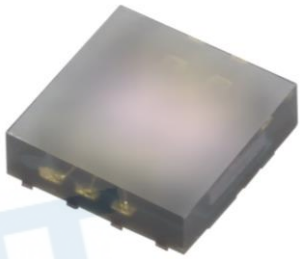
DATASHEET

RGBW Color Sensor with I²C Interface
CLS-16D24-44-DF8/TR8

Features



- I²C interface (Fast Speed Mode at 400kHz/s)
- Supply Voltage Range from 2.4V to 3.6V
- I²C BUS Voltage Range from 1.7V to 3.6V
- Operating Temperature Range from-40°C to +65°C
- Support parallel output for (R, G, B, W, IR)
- Up to 16-bit Digital Output (0~65535)
- Programmable Dynamic Range Ratio (x1, x4, x8, x32, x96)
- High resolution (0.002 Lux/count)
- Maximum detection lux (204,679 Lux)
- Programmable integration time
- 50Hz/60Hz flicker noise and IR rejection
- Individual programmable low and high threshold for interrupt function
- The product itself will remain within RoHS compliant version
- Compliance with EU REACH
- Compliance Halogen Free(Br < 900ppm, Cl < 900ppm, Br+Cl < 1500ppm)

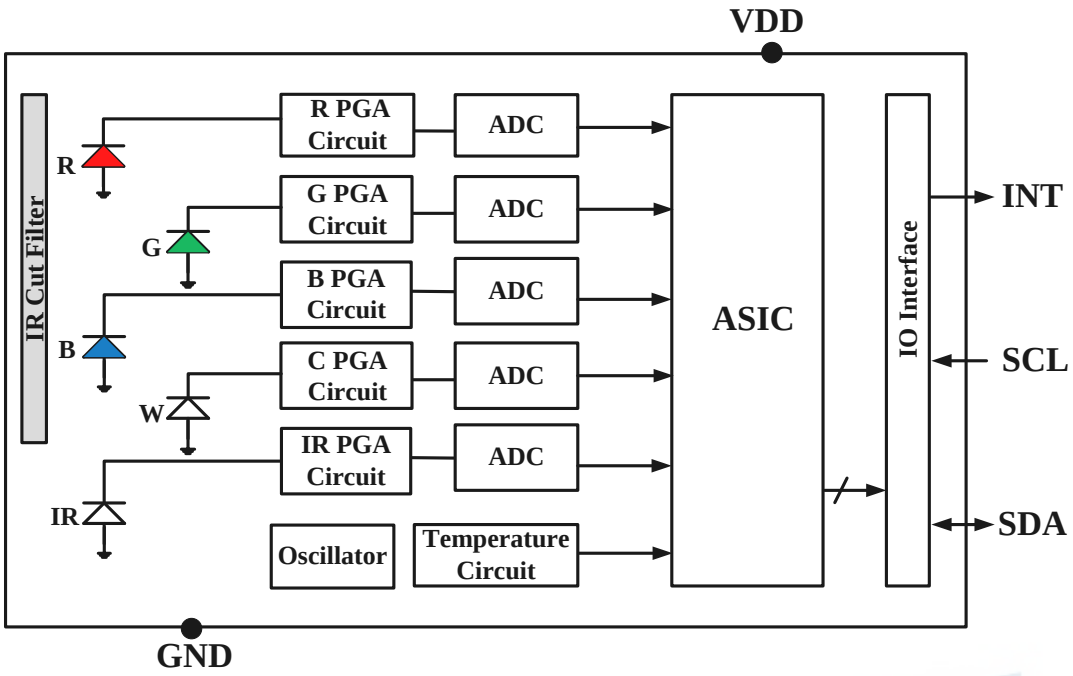
Description

The CLS-16D24-44-DF8/TR8 is a low power, high sensitivity, Color light sensor with an I²C interface. This color sensor senses red, green, blue, white (RGBW) and infrared light and converts them to digital values. The RGBW sensor is designed to reject IR in light sources allowing the device to operate in environments from sunlight to dark rooms. The integrating ADC rejects 50Hz and 60Hz flicker caused by artificial light sources. A selectable range allows the user to optimize sensitivity suitable for the illuminance and color temperature of ambient light for adjusting LCD backlight of TV, mobile phone and tablet PC. The CLS-16D24-44-DF8/TR8 supports hardware and software user programmable interrupt thresholds.

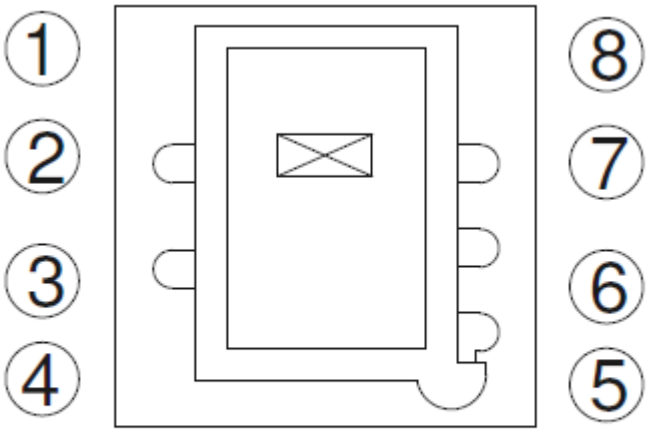
Applications

- Detection of ambient for controlling the backlight of TFT LCD display.
- Automatic residential and commercial lighting management.
- Automatic contrast enhancement for electronic signboard.
- Mobile phone, Smart phone, PDA, Tablet PC.

Block Diagram



I/O Pins Configuration



Top view

Pad Description

Pin	I/O Type	Pin Name	Description
1	NC	NC	No connection
2	PWR	VDD	Power supply
3	GND	GND	Ground
4	NC	NC	No connection
5	I	SCL	I²C serial clock line
6	I/O	SDA	I²C serial data line
7	O	INT	Interrupt pin
8	NC	NC	No connection

Direction denotation:

I/O Type	Dir.	I/O Type	Dir.
O	Output	GND	Ground
I	Input	I/O	Input / Output
PWR	Power	NC	Not Connect

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	VDD	4.5	V
I²C Bus Pin Voltage	SCL, SDA, INT	-0.2 to 4.5	V
Operating Temperature	T_{ope}	-40 to +65	℃
Storage Temperature	T_{stg}	-40 to +100	℃
ESD Rating	Human Body Model	2	KV

Note:

Exceeding these ratings could cause damage to the device. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminal.

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage (Note 1)	V_{DD}	2.4	-	3.6	V	-
I²C Bus Pin Voltage	V_{Bus}	1.62	1.8	V_{DD}	V	$V_{Bus} \leq V_{DD}$
Operating Temperature	T_{ope}	-40	-	+65	℃	-
I²C Bus Input High Voltage (Note2)	V_{IH_SCL}, V_{IH_SDA}	V_{Bus} x 0.7	- -	- -	V	-
I²C Bus Input Low Voltage Note2	V_{IL_SCL}, V_{IL_SDA}	- -	- -	0.5	V	-

Notes:

1. The power supply need to make sure the VDD slew rate at least 1.0V/ms. CLS-16D24-44-DF8/TR8 has a power on reset function. When VDD drops below 2V at room temp, the IC will be reset automatically. After power back up at the required slew rate, the I2C registers need to be set again to the required values.
2. The specs are defined under V_{DD}=3.3V, T_a=25°C

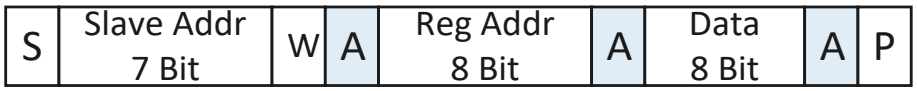
Electro-Optical Characteristics (V_{DD}=3.3V, T_a = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Current	I_{DD}	-	210	-	μA	E_V = 0 lx (Note 1)
	I_{PD}	-	2.5	-	μA	Sleep mode E_V = 0 lx I^2C inactive
A/DC resolution	-	10	-	16	bit	-
ADC integration time	T_{INT}	2.067	-	2116	ms	INT_TIME x CLSCONV
Sensing Area	DIOD_SELT	1	-	2	-	-
Full ADC counts value	-	1023	-	65535	counts	-
Dark ADC Count	RCH GCH BCH WCH	0	1	3	counts	E_V = 0 lx (Note 2)
Irradiance response	RCH	-	1500	-	counts	λ_P=632 nm LED (Note 3,5)
	GCH	-	3300	-	counts	λ_P=518 nm LED (Note 3,6)
	BCH	-	2100	-	counts	λ_P=468 nm LED (Note 3,7)
CLS detection resolution	-	-	-	0.002	lx/count	White LED 6500K (Note 2)
CLS maximum detection intensity	-	-	-	204K	Lux	White LED 6500K (Note 4)
Peak sensitivity wavelength	λ_{PRed} λ_{PGreen} λ_{PBlue}	-	610 550 470	-	nm	-

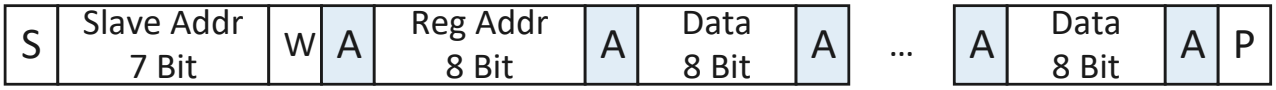
Note :

1. The testing condition: **EN_CLS**=1, **DIOD_SELT**=2, **PGA_CLS**=x4, **INT_TIME**=64 T, **CLSCONV**=1 **INT_TIME**
2. The testing condition: **EN_CLS**=1, **DIOD_SELT**=2, **PGA_CLS**=x96, **INT_TIME**=64 T, **CLSCONV**=16 **INT_TIME**
3. The testing condition: **EN_CLS**=1, **DIOD_SELT**=2, **PGA_CLS**=x96, **INT_TIME**=16 T, **CLSCONV**=6 **INT_TIME**
4. The testing condition: **EN_CLS**=1, **DIOD_SELT**=1, **PGA_CLS**=x1, **INT_TIME**=1 T, **CLSCONV**=1 **INT_TIME**
5. Red LED is used as optical source. (I_e = 20 μW/cm²)
6. Green LED is used as optical source. (I_e = 20 μW/cm²)
7. Blue LED is used as optical source. (I_e = 20 μW/cm²)

I2C Write Format

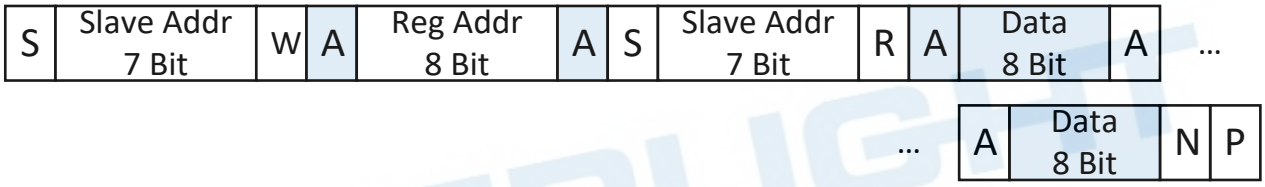


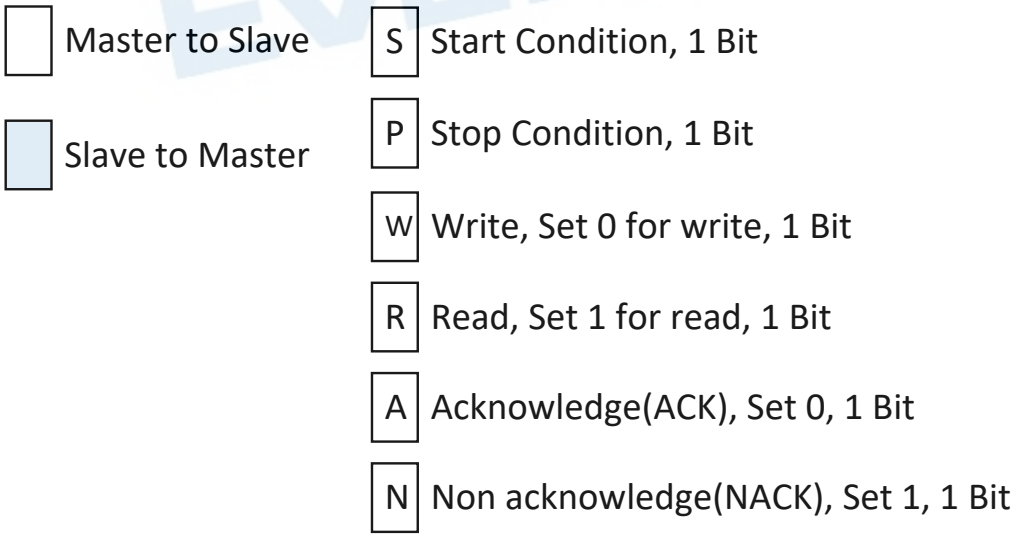
I2C Block Write Format



I2C Read Format

I2C Block Read Format





I2C Slave Address and R/W bit

This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). A '0' indicates a transmission (WRITE), a '1' indicates a request for data (READ). The slave address of this device is 0x38.

Register Set

The CLS-16D24-44-DF8/TR8 is operated over the I²C bus with registers that contain configuration, status, and result information. All registers are 8 bits long.

Address	Name	Type	Default value	Description
0x00	SYSM_CTRL	RW	0x00	CLS operation mode control, waiting mode control, SW reset
0x01	INT_CTRL	RW	0x03	Interrupt pin control, interrupt persist control
0x02	INT_FLAG	RW	0x00	Interrupt flag, error flag, power on reset(POR) flag
0x03	WAIT_TIME	RW	0x00	Waiting time setting
0x04	CLS_GAIN	RW	0x00	CLS analog gain setting
0x05	CLS_TIME	RW	0x00	CLS integrated time setting
0x0B	PERSISTENCE	RW	0x11	CLS persistence setting
0x0C	CLS_THRES_LL	RW	0x00	CLS lower interrupt threshold - LSB
0x0D	CLS_THRES_LH	RW	0x00	CLS lower interrupt threshold - MSB
0x0E	CLS_THRES_HL	RW	0xFF	CLS higher interrupt threshold - LSB
0x0F	CLS_THRES_HH	RW	0xFF	CLS higher interrupt threshold - MSB
0x16	INT_SOURCE	RW	0x08	CLS interrupt source
0x17	ERROR_FLAG	RW	0x00	Error flag
0x1C	RCH_DATA_L	R	0x00	RCH output data - LSB
0x1D	RCH_DATA_H	R	0x00	RCH output data - MSB
0x1E	GCH_DATA_L	R	0x00	GCH output data - LSB
0x1F	GCH_DATA_H	R	0x00	GCH output data - MSB
0x20	BCH_DATA_L	R	0x00	BCH output data - LSB
0x21	BCH_DATA_H	R	0x00	BCH output data - MSB
0x22	WCH_DATA_L	R	0x00	WCH output data - LSB
0x23	WCH_DATA_H	R	0x00	WCH output data - MSB
0x24	IRCH_DATA_L	R	0x00	IRCH output data - LSB
0x25	IRCH_DATA_H	R	0x00	IRCH output data - MSB
0xBC	PROD_ID_L	R	0x12	Product ID - LSB
0xBD	PROD_ID_H	R	0x07	Product ID - MSB

SYSM_CTRL

0x00	SYSM_CTRL, System Control (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	SWRST	EN_WAIT	0	0	0	0	EN_IR	EN_CLS

SWRST：Software reset. Reset all register to default value.

0: (Default)

1: Reset will be triggered.

EN_WAIT：Waiting time will be inserted between two measurements.

0: Disable waiting function. (Default)

1: Enable waiting function.

EN_IR：Enables IR function.

0: Disable IR function. (Default)

1: Enable IR function.

EN_CLS：Enables CLS function.

0: Disable CLS function. (Default)

1: Enable CLS function.

INT_CTRL

0x01	Interrupt Pin Control (Default = 0x01)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	CLS_ SYNC	0	0	0	EN_CINT

CLS_SYNC：Measurement is pended when CLS interrupt is triggered. Until clear the interrupt then start the next measurement.

0: Disable pending CLS function. (Default)

1: Enable pending CLS function.

EN_CINT：The CLS interrupt (INT_CLS) flag can trigger the INT pin to low.

0: Disable **INT_CLS** effect INT pin.

1: Enable **INT_CLS** effect INT pin. (Default)

INT_FLAG

0x02	INT_FLAG, System Control (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	INT_POR	DATA_ FLAG	0	0	0	0	0	INT_CLS

INT_POR： Power-On-Reset Interrupt flag trigger the INT pin when the flag sets to one. Write zero to clear the flag.

0: Clear the flag

1: This bit will be set to one when it satisfy one of the following conditions:

- Power On
- VDD < 2.0V
- SWRST

DATA_FLAG： It shows if any data is invalid after completion of each conversion cycle. This bit is read-only.

0: data valid.

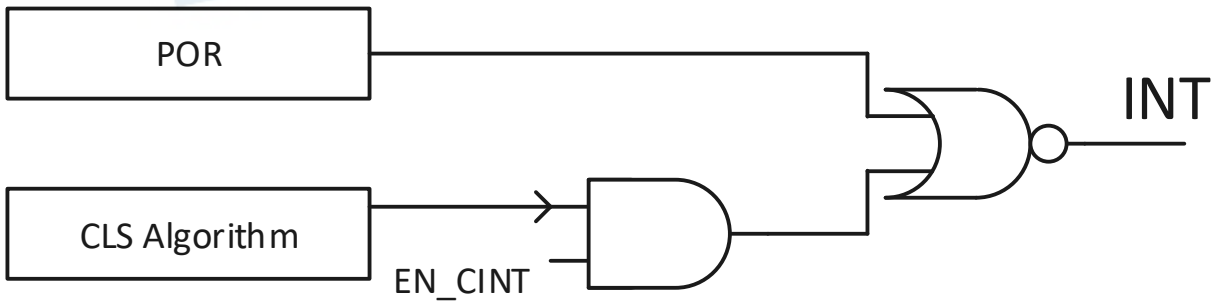
1: data invalid.

INT_CLS： CLS Interrupt flag. It correlation with sensor data and CLS high/low threshold. Write zero to clear the flag.

0: CLS Interrupt not trigger or be cleared.

1: CLS interrupt triggered

Interrupt Behavior:



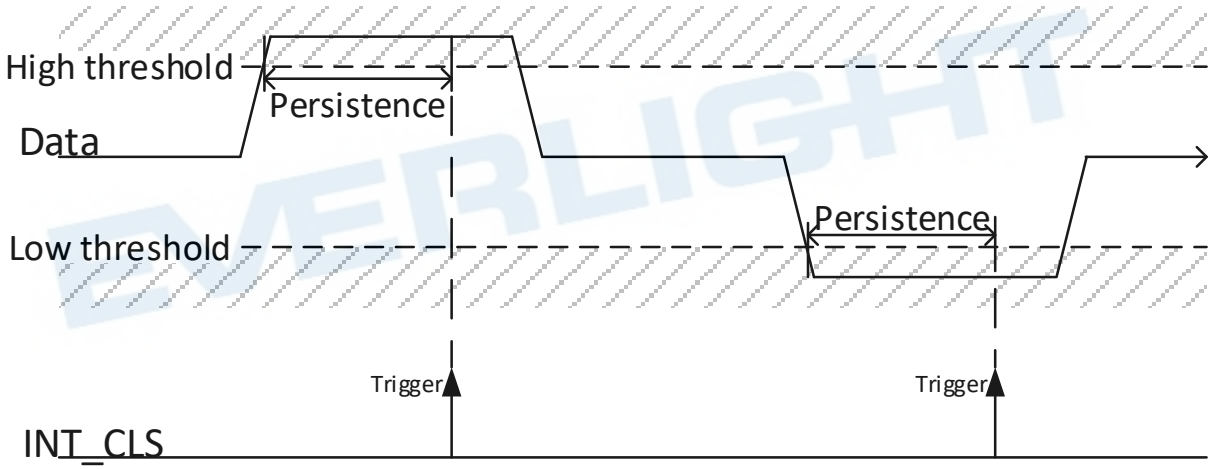
CLS Interrupt Algorithm

Correlative register:

The CLS Interrupt (**INT_CLS, register 0x02, bit0).**
The CLS Persistence (**PRS_CLS**, register 0x0B, bit0 to bit3),
The CLS Data (**W channel data**, register 0x22 to 0x23),
The CLS Low Threshold (**CLS_THRES_L**, register 0x0C to 0x0D),
The CLS High Threshold (**CLS_THRES_H**, register 0x0E to 0x0F).

INT_CLS triggered condition:

1. Rule of active interrupt: **DATA**>**CLS_THRES_H** or **DATA**<**CLS_THRES_L.**
2. If the **DATA** meets the rule, the **interrupt** count increases one.
   If the **DATA** fails in the rule, the interrupt count will be clear.
3. When the **interrupt** count equal to **PRS_CLS setting**, **INT_CLS** will be triggered and reset the interrupt counter.
4. If **PRS_CLS** is set to zero, **threshold** will be ignored and **DATA** will meet the active interrupt rule forcibly.



WAIT_TIME

0x03	WAIT_TIME, waiting time (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	WTIME							

WTIME： This register controls the time unit of waiting state which is inserted between two measurements. It is 10 ms per time unit.

0x00: 1 time unit.
0x01: 2 time units
……
0xFF: 256 time units

CLS_GAIN

0x04	CLS_GAIN, CLS analog gain (Default = 0x81)							
BIT	7	6	5	4	3	2	1	0
R/W	DIOD_SELT	0	0	PGA_CLS				

DIOD_SELT：CLS sensor area select.

0: x1
1: x2 (default)

PGA_CLS： CLS sensing gain.

0x01: x1 (default)
0x02: x4
0x04: x8
0x08: x32
0x10: x96

CLS_TIME

0x05	CLS_TIME, CLS integrated time (Default = 0x03)							
BIT	7	6	5	4	3	2	1	0
R/W	CLSCONV				0	0	INT_TIME	

CLSCONV：This register controls the conversion time of AD converter at CLS mode (T_{CLS}), and the resolution of output data.

0x0: The maximum count of **output data is**1023, T_{CLS} = 1 INT_TIME (default)
0x1: The maximum count of **output data is**2047, T_{CLS} = 2 INT_TIME
……
0xf: The maximum count of **output data is**16384, T_{CLS} = 16 INT_TIME

INT_TIME：This register controls the integrated time.

0x0: 1 INT_TIME (T) = 2.0667 ms.
0x1: 4 INT_TIME (4T)= 8.2668 ms.
0x2: 16 INT_TIME (16T)= 33.0672 ms.
0x3: 64 INT_TIME (64T)= 132.2688 ms.

The conversion time of CLS function (T_{CLS}) is decided by **CLSCONV and INT_TIME**.
T_{CLS}= 3.827+ [**INT_TIME** x (**CLSCONV** + 1)] (ms)
EX :
Setting INT_TIME= 0x01 (4T UNIT) and CLSCONV = 0x01
The maximum count of **output data is** minimum of
[1024 x [INT_TIME * (CLSCONV+1)] - 1 , 65535]
= [1024 x [4 * (1+1)] - 1 , 65535].

PERSISTENCE

0x0B	PERSISTENCE, CLS persistence setting (Default = 0x00)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	0	PRS_CLS			

PRS_CLS：This register sets the number of similar consecutive CLS interrupt events before the interrupt pin is triggered.

0x0: interrupt always on independent from CLS values, don't use.
0x1: if one single CLS value fulfills the interrupt condition an interrupt will be triggered
……
0xf: 15 consecutive CLS values must fulfill the interrupt condition to trigger an interrupt

CLS_THRES_L

0x0C 0x0D	CLS_THRES_L, CLS low interrupt threshold (Default = 0x0000)							
BIT	7	6	5	4	3	2	1	0
R/W	CLS_THRE_LL							
R/W	CLS_THRE_LH							

This register sets the lower threshold value of CLS interrupt. The interrupt algorithm compares the selected CLS data and CLS threshold value.

CLS_THRE_LL：CLS lower interrupt threshold value, LSB. (Reg. 0x0C)

CLS_THRE_LH：CLS lower interrupt threshold value, MSB. (Reg. 0x0D)

CLS_THRES_H

0x0E 0x0F	CLS_THRES_H, CLS high interrupt threshold (Default = 0xFFFF)							
BIT	7	6	5	4	3	2	1	0
R/W	CLS_THRE_HL							
R/W	CLS_THRE_HH							

This register sets the high threshold value of CLS interrupt. The interrupt algorithm compares the selected CLS data and CLS threshold value.

CLS_THRE_HL：CLS high interrupt threshold value, LSB. (Reg. 0x0E)

CLS_THRE_HH：CLS high interrupt threshold value, MSB. (Reg. 0x0F)

INT_SOURCE

0x16	INT_SOURCE, CLS interrupt source (Default = 0x08)							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	INT_SRC				

INT_SRC：This register sets to select the CLS data for the CLS Interrupt algorithm.

0x01: Select RCH_DATA.
0x02: Select GCH_DATA.
0x04: Select BCH_DATA.
0x08: Select WCH_DATA. (default)
0x10: Select IRCH_DATA.

ERROR_FLAG

0x17	ERROR_FLAG, Error flag status							
BIT	7	6	5	4	3	2	1	0
R/W	0	0	0	ERR_IRCH	ERR_WCH	ERR_BCH	ERR_GCH	ERR_RCH

This register indicates the CLS data status. If the CLS data is outside of measurable range, the corresponding error flag (ERR_RCH, ERR_GCH, ERR_BCH, ERR_WCH, and ERR_IRCH) will set to one. That also means the data is invalid.

RCH_DATA

0x1C 0x1D	RCH_DATA, R channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	RCH_DATA _L							
R/W	RCH_DATA_H							

The R channel conversion result is written into RCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has being accessed until the high byte data has been read.

GCH_DATA

0x1E 0x1F	**GCH_DATA, G channel output data.**							
BIT	7	6	5	4	3	2	1	0
R/W	GCH_DATA_L							
R/W	GCH_DATA_H							

The G channel sensor result is written into GCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has being accessed until the high byte data has been read.

BCH_DATA

0x20 0x21	BCH_DATA, B channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	BCH_DATA_L							
R/W	BCH_DATA_H							

The B channel sensor result is written into BCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has being accessed until the high byte data has been read.

WCH_DATA

0x22 0x23	WCH_DATA, W channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	WCH_DATA_L							
R/W	WCH_DATA_H							

The W channel sensor result is written into WCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has being accessed until the high byte data has been read.

IRCH_DATA

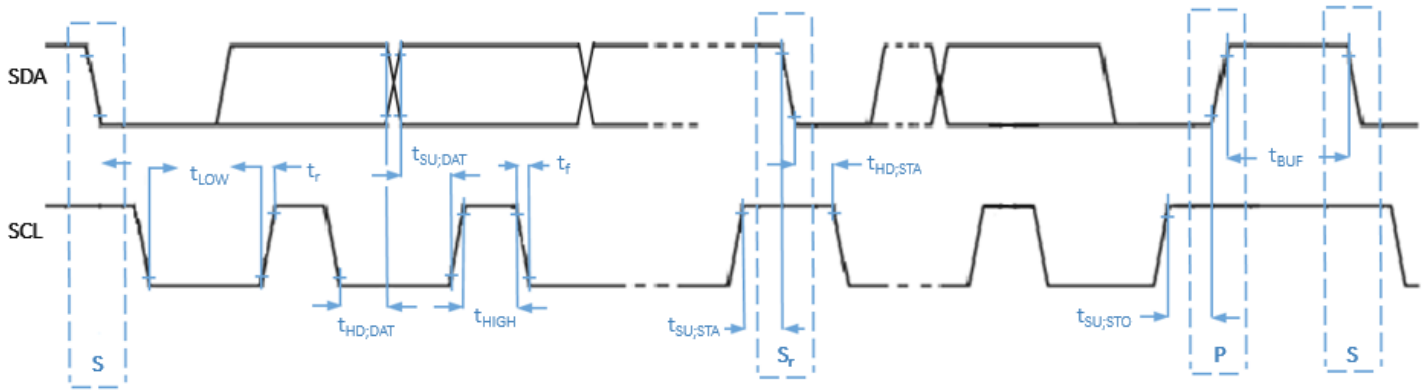
0x24 0x25	IRCH_DATA, IR channel output data.							
BIT	7	6	5	4	3	2	1	0
R/W	IRCH_DATA_L							
R/W	IRCH_DATA_H							

The IR channel sensor result is written into IRCH_DATA when CLS conversion is done.

For insuring the data in the register comes the same measurement, the high byte data will be latched when the low byte data has being accessed until the high byte data has been read.

I²C Interface Timing Characteristics

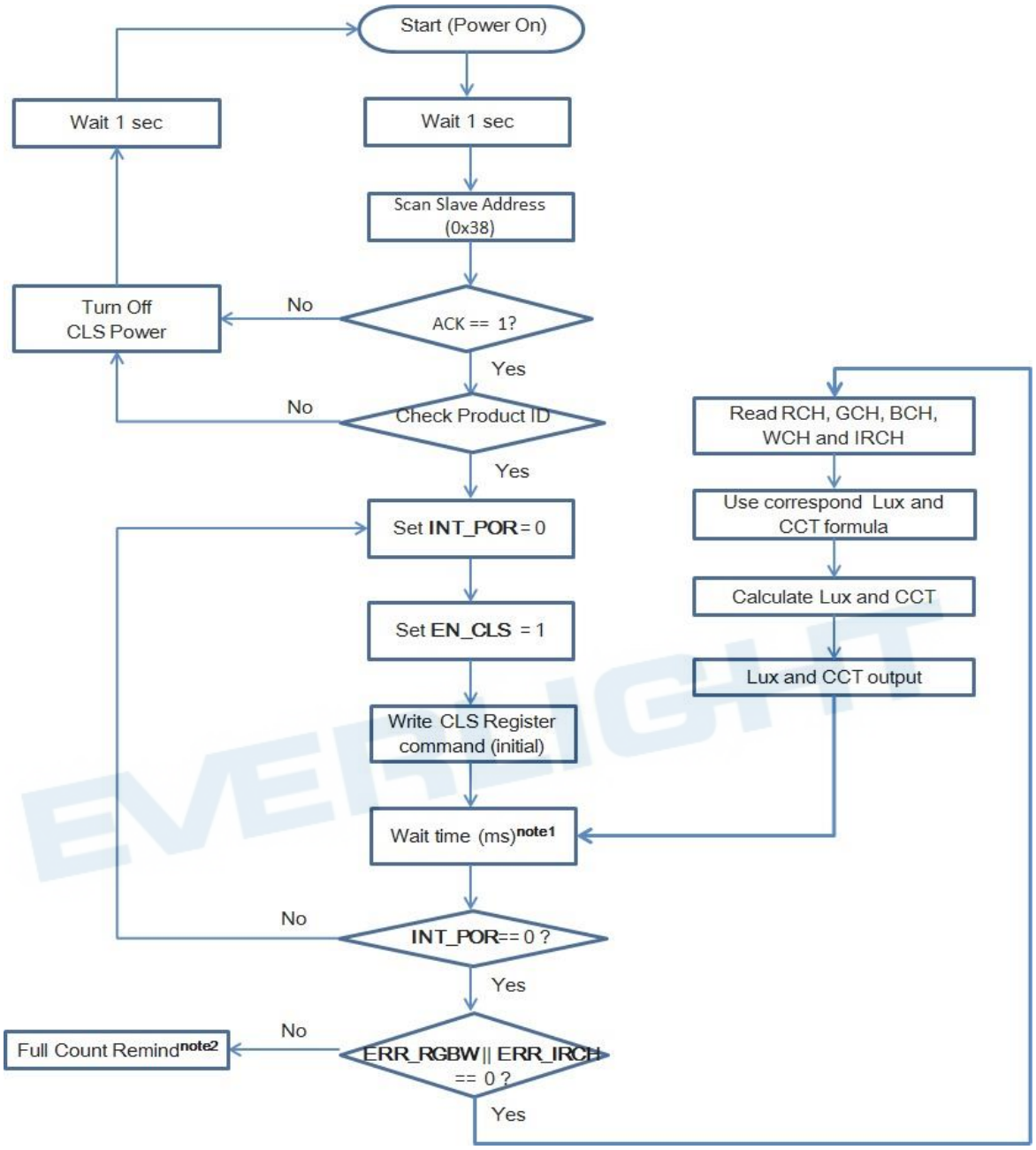
This section will describe the protocol of the I²C bus. For more details and timing diagrams please refer to the I²C specification.



Parameter (*)	Symbol	I²C Standard Mode		I²C Fast Mode		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition	$t_{HD;STA}$	4	--	0.6	--	μs
Set-up time (repeated) START condition	$t_{SU;STA}$	4.7	--	0.6	--	μs
LOW period of the SCL clock	t_{LOW}	4.7	--	1.3	--	μs
HIGH period of the SCL clock	t_{HIGH}	4	--	0.6	--	μs
Data hold time	$t_{HD;DAT}$	0	3.45	0	0.9	μs
Data set-up time	$t_{SU;DAT}$	250	--	100	--	ns
Rise time of both SDA and SCL signals	$t_{(r)}$	--	1000	20	300	ns
Fall time of both SDA and SCL signals	$t_{(f)}$	--	300	--	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4	--	0.6	--	μs
Bus free time between STOP condition and START condition	t_{BUF}	4.7	--	1.3	--	μs

(*) All specifications are at V_{Bus} = 3.3V, T_{ope}=25˚C, unless otherwise noted. Specified by design and characterization; not production tested.

Basic Operation Flow Chart



Notes:

1. The wait time need to be longer than WAIT_TIME + CLS_TIME (ms).
2. ERR_RCH || ERR_GCH || ERR_BCH || ERR_WCH || ERR_IRCH ==1 means CLS data is outside of measurable range.

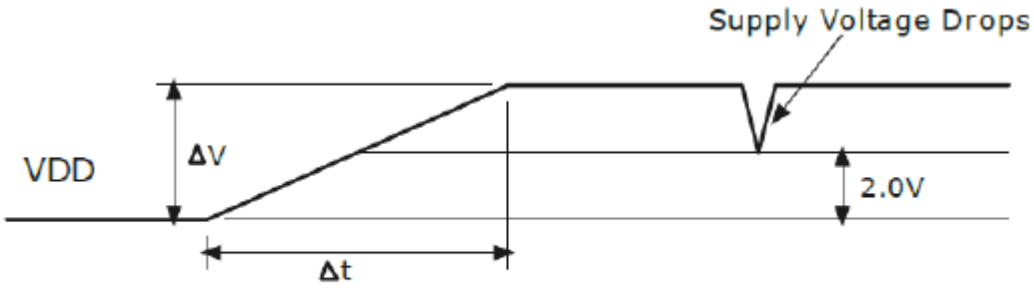
Next steps can be decided by costumer, such as:

- ●Ignore the reminder and continue reading RCH、GCH、BCH、WCH & IRCH.
- ●Send an error message to MCU and wait for next command.
- ●Other error handling actions.

Supply Voltage Drops

Upon power-up, a slew rate of VDD greater than 1.0 V/ms must be ensured.

The supply voltage shall NOT drop below 2.0V after power up. If the voltage dropped below 2V after power up, the supply voltage must be turned off for at least one second before powering up the device again.



$$\text{Slew Rate} = \frac{\Delta V}{\Delta t} > 1.0\,V/\,mS$$

Note:

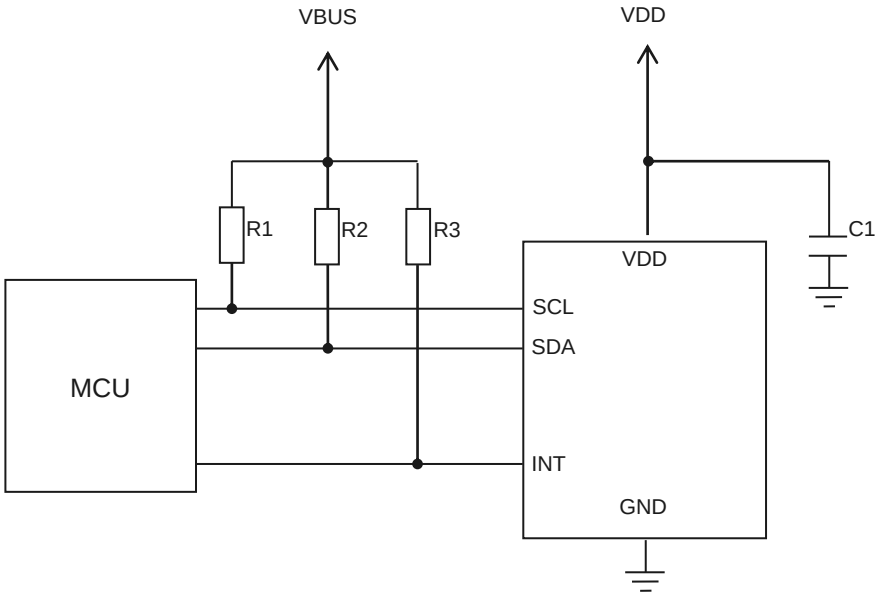
I²CBus Clear

In the unlikely event where the clock (SCL) is stuck LOW, the preferential procedure is to reset the bus using the HW reset signal if your I2C devices have HW reset inputs. If the I2C devices do not have HW reset inputs, cycle power to the devices to activate the mandatory Internal Power-On Reset (POR) circuit.
If the data line (SDA) is stuck LOW, the master should send nine clock pulses. The device that held the bus LOW should release it within those nine clock cycles.

I²C General Call Software Reset

Following a General Call, (0000 0000), sending 0000 0110 (06h) as the second byte causes software reset. This feature is optional and not all devices will respond to this command. On receiving this 2-byte sequence, all devices designed to respond to the general call address will reset and take in the programmable part of their address.
Precautions have to be taken to ensure that a device is not pulling down the SDA or SCL line after applying the supply voltage, since these low levels would block the bus.

Typical Application Circuit



CLS-16D24-44-DF8/TR8

The capacitor C1 is required for sensor power supply. The capacitor should be placed as close as possible to the VDD pin. The high frequency AC noises can be shunted to the ground by the capacitors. The transient current caused by digital circuit switching also can be handled by the capacitors. A typical value of 0.1μF can be used. The capacitor must be a ceramic capacitor. When choosing the capacitor temperature effects and capacitance change over voltage must be considered.

The pull-up resistors (R1, R2) are required for I²C communication. At fast speed mode (400kHz/s) and VBUS = 3V, the resistor values must not be lower than 1kΩ. Higher values can be used, but might cause too slow rise/fall times in case of high parasitic capacitances of the I2C bus. The pull-up resistor (R3) is also required for the interrupt, a typical value between 10kΩ and 100kΩ can be used.

Electrical and Optical Characteristics (T_a=25℃)

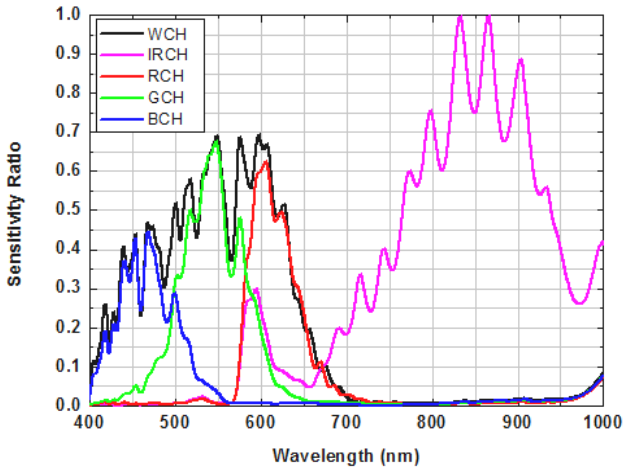


Fig.1 Spectral vs. Wavelength

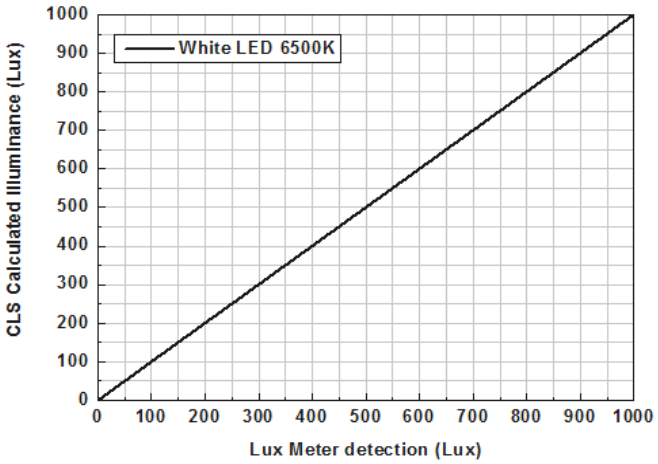


Fig.2 CLS sensor Lux vs. Meter Lux (White LED)

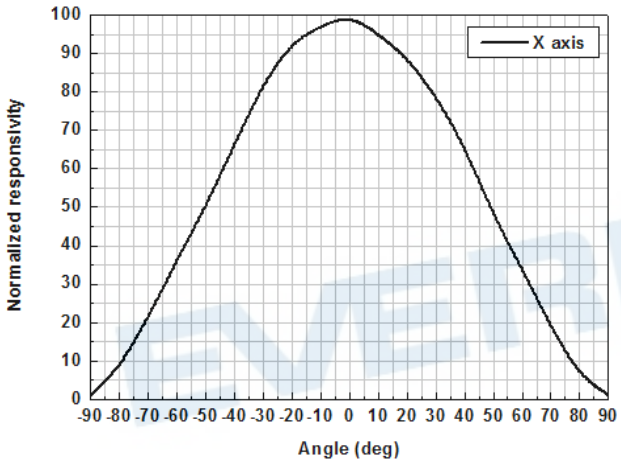


Fig.3 CLS angular sensitivity for X axis

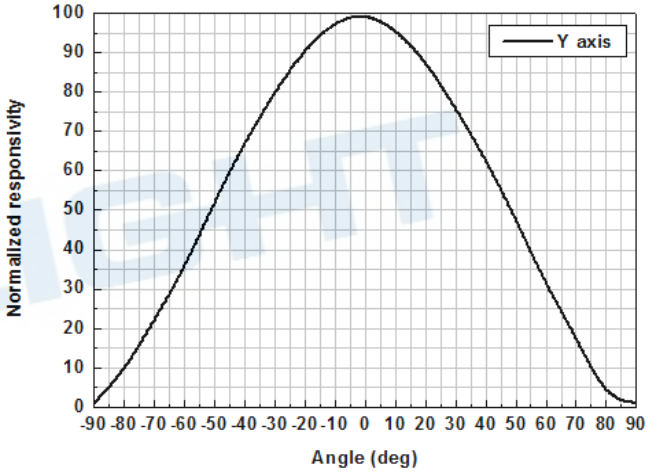


Fig.4 CLS angular sensitivity for Y axis

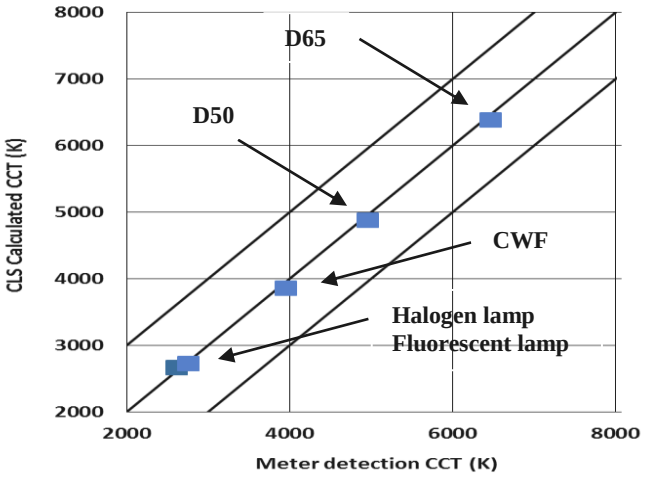
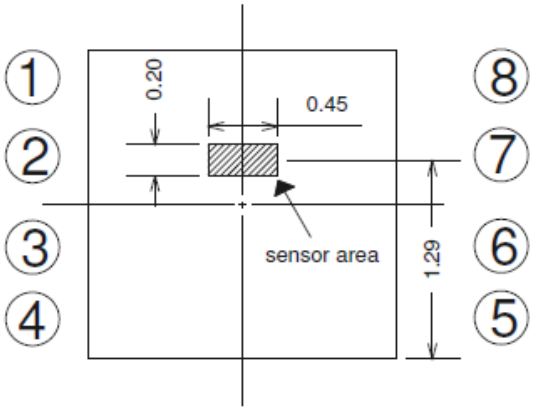


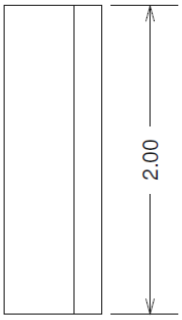
Fig.5 CLS sensor CCT vs. Meter CCT

Package Dimensions and recommended solder pad layout

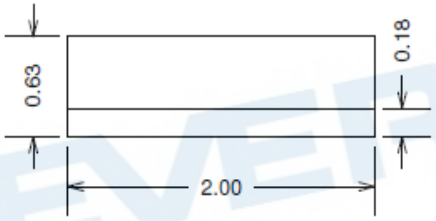
Top view



Side View

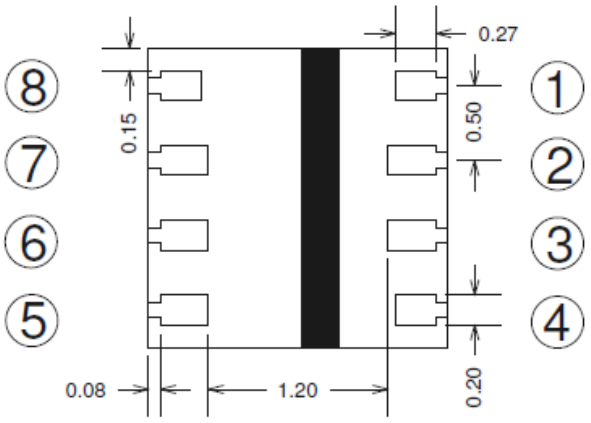


Side View

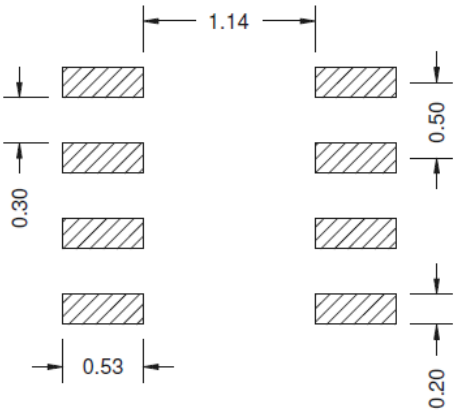


Pad Number	Pad Name
1	NC
2	VDD
3	GND
4	NC
5	SCL
6	SDA
7	INT
8	NC

Bottom View



Recommend Soldering Pad

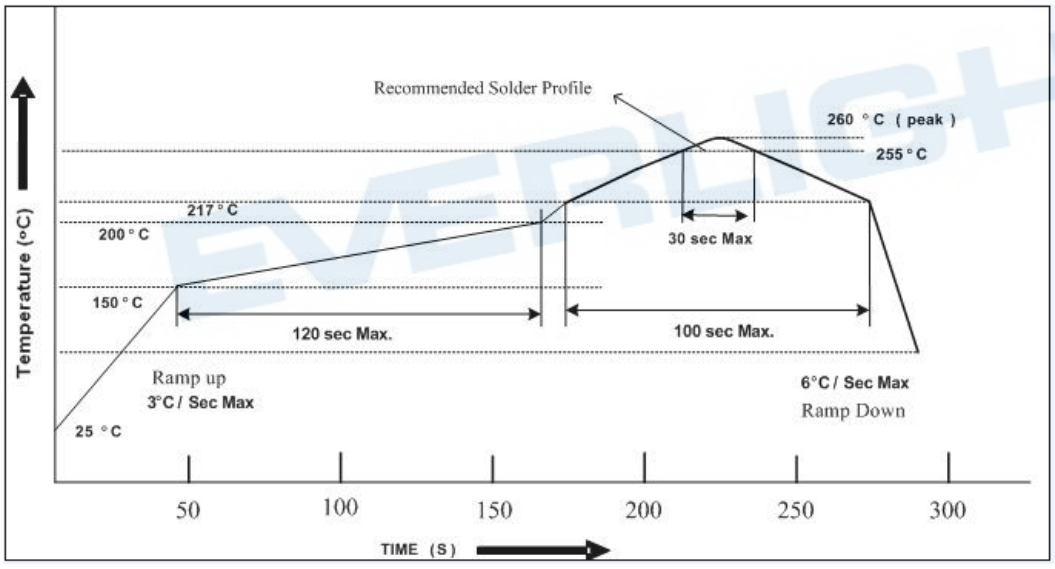


Unit: mm
Tolerances: ± 0.1mm

Recommended method of storage

1. Do not open moisture proof bag before devices are ready to use.
2. Shelf life in sealed bag from the bag seal date: 18 months at 10°C~30°C and < 90% RH.
3. After opening the package, the devices must be stored at 10°C~30°C and ≤ 60%RH, and used within 168 hours (floor life).
4. If the moisture absorbent material (desiccant material) has faded or unopened bag has exceeded the shelf life or devices (out of bag) have exceeded the floor life, baking treatment is required.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure or recommend the following conditions:
   192 hours at 40°C +5/–0°C and < 5 % RH (reeled/tubed/loose units) or
   96 hours at 60°C ± 5°C and < 5 % RH (reeled/tubed/loose units) or
   24 hours at 125°C ± 5°C, not suitable for reel or tubes.

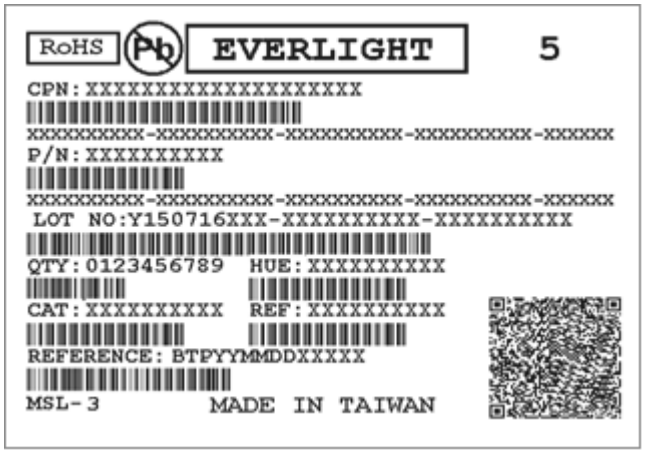
Recommended Solder Profile



Notice:

1. Reflow soldering should not be done more than two times.
2. When soldering, do not put stress on the devices during heating.
3. After soldering, do not warp the circuit board.
4. Reference: IPC/JEDEC J-STD-020D

Label Explanation

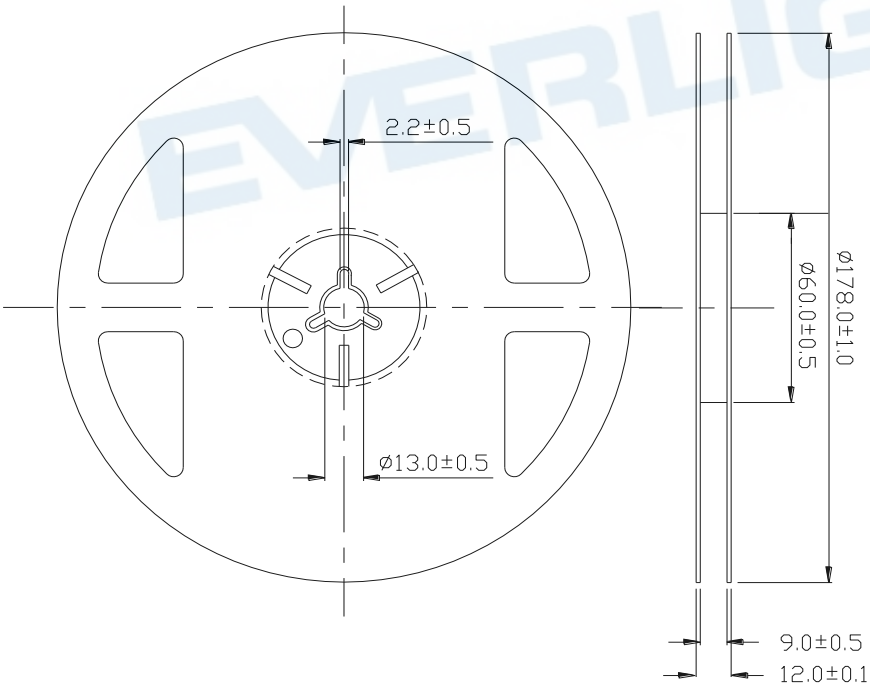


·CPN: Customer's Product Number
·P/N: Product Number
·QTY: Packing Quantity
·CAT: Luminous Intensity Rank
·HUE: Dom. Wavelength Rank
·REF: Forward Voltage Rank
·LOT No: Lot Number
·MADE IN TAIWAN: Production Place

Packing Quantity Specification

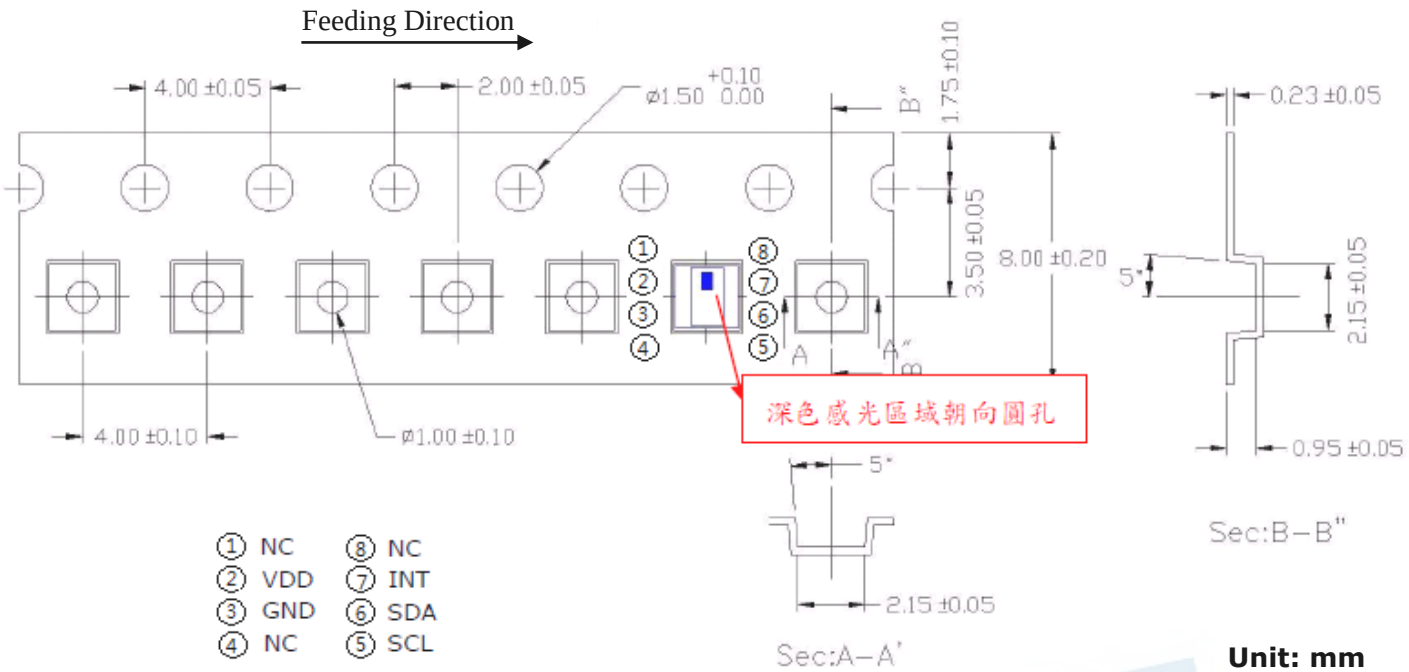
2000 PCS/ 1 Reel

Reel Dimensions



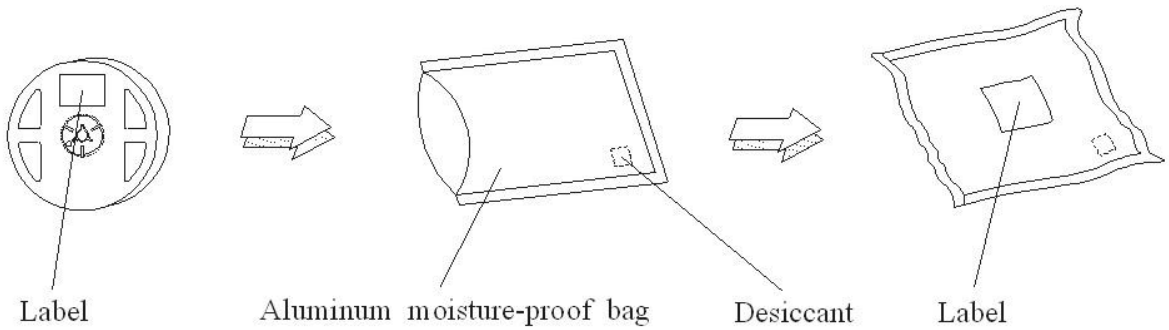
Unit: mm

Tape Dimensions



Unit: mm

Moisture Resistant Packing Process



DISCLAIMER

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2. The product meets EVERLIGHT published specification for a period of twelve (12) months from date of shipment.
3. The graphs shown in this datasheet are representing typical data only and do not show guaranteed values.
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