CMOS Static RAM
1 Meg (128K x 8-Bit)
Revolutionary Pinout

Features

- **128K x 8 advanced high-speed CMOS static RAM**
- **JEDEC revolutionary pinout (center power/GND) for reduced noise.**
- **Equal access and cycle times**
  - *Commercial: 12/15/20ns*
  - *Industrial: 15/20ns*
- **One Chip Select plus one Output Enable pin**
- **Bidirectional inputs and outputs directly TTL-compatible**
- **Low power consumption via chip deselect**
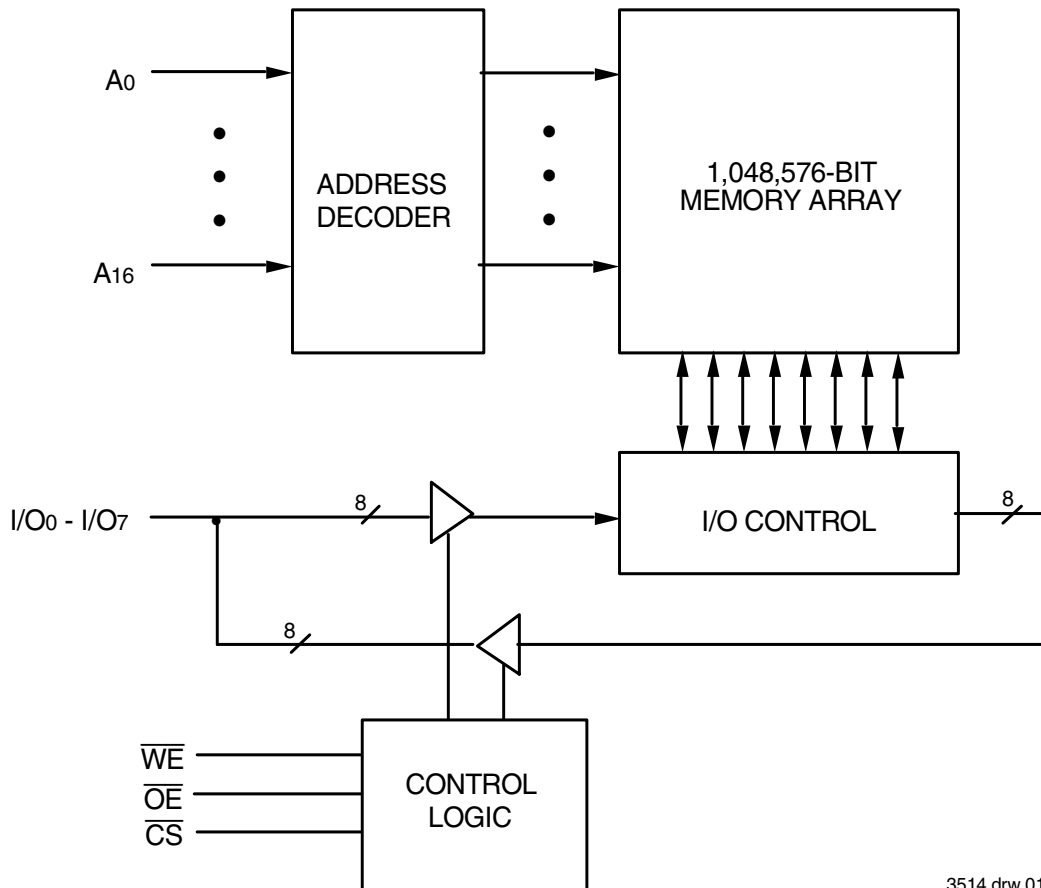- **Available in a 32-pin 400 mil Plastic SOJ.**

Description

The IDT71124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center power/GND pinout reduces noise generation and improves system performance.

The IDT71124 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71124 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.
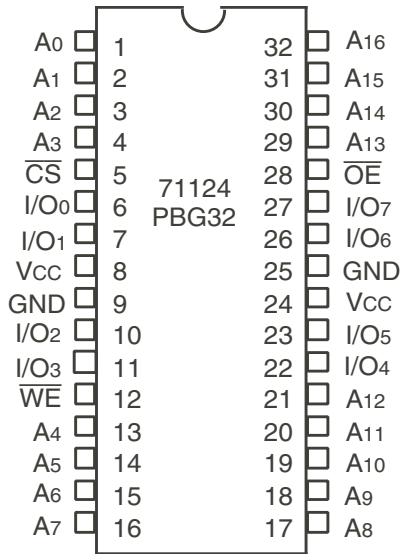
The IDT71124 is packaged in a 32-pin 400 mil Plastic SOJ.

Functional Block Diagram

3514 drw 01

Pin Configuration


```
    A0  ▯ 1          32 ▯  A16
    A1  ▯ 2          31 ▯  A15
    A2  ▯ 3          30 ▯  A14
    A3  ▯ 4          29 ▯  A13
    CS̄  ▯ 5          28 ▯  ŌĒ
  I/O0  ▯ 6   71124  27 ▯  I/O7
  I/O1  ▯ 7   PBG32  26 ▯  I/O6
   Vcc  ▯ 8          25 ▯  GND
   GND  ▯ 9          24 ▯  Vcc
  I/O2  ▯ 10         23 ▯  I/O5
  I/O3  ▯ 11         22 ▯  I/O4
    WĒ  ▯ 12         21 ▯  A12
    A4  ▯ 13         20 ▯  A11
    A5  ▯ 14         19 ▯  A10
    A6  ▯ 15         18 ▯  A9
    A7  ▯ 16         17 ▯  A8
```

3514 drw 02

SOJ
Top View

Truth Table[1,2]

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	DATA$_{OUT}$	Read Data
L	X	L	DATA$_{IN}$	Write Data
L	H	H	High-Z	Output Disabled
H	X	X	High-Z	Deselected - Standby (I_{SB})
V$_{HC}$[3]	X	X	High-Z	Deselected - Standby (I_{SB1})

3514 tbl 01

NOTES:
1. H = V$_{IH}$, L = V$_{IL}$, x = Don't care.
2. VLC = 0.2V, VHC = VCC -0.2V.
3. Other inputs ≥ VHC or ≤ VLC.

Absolute Maximum Ratings[1]

Symbol	Rating	Value	Unit
V$_{TERM}$[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0[2]	V
T$_A$	Operating Temperature	0 to +70	ºC
T$_{BIAS}$	Temperature Under Bias	-55 to +125	ºC
T$_{STG}$	Storage Temperature	-55 to +125	ºC
P$_T$	Power Dissipation	1.25	W
I$_{OUT}$	DC Output Current	50	mA

3514 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V$_{TERM}$ must not exceed Vcc + 0.5V.

Capacitance
(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 3dV	8	pF
C$_{I/O}$	I/O Capacitance	V$_{OUT}$ = 3dV	8	pF

3514 tbl 03

NOTE:
1. This parameter is guaranteed by device characterization, but is not production tested.

Recommended Operating Temperature and Supply Voltage

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	−40°C to +85°C	0V	5.0V ± 10%

3514 tbl 04

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V$_{CC}$	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V$_{IH}$	Input High Voltage	2.2	—	V$_{CC}$ +0.5	V
V$_{IL}$	Input Low Voltage	-0.5[1]	—	0.8	V

3514 tbl 05

NOTE:
1. V$_{IL}$ (min.) = –1.5V for pulse width less than 10ns, once per cycle.

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DC Electrical Characteristics
(V$_{CC}$ = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
|I$_{LI}$|	Input Leakage Current	V$_{CC}$ = Max., V$_{IN}$ = GND to V$_{CC}$	—	5	µA
|I$_{LO}$|	Output Leakage Current	V$_{CC}$ = Max., $\overline{CS}$ = V$_{IH}$, V$_{OUT}$ = GND to V$_{CC}$	—	5	µA
V$_{OL}$	Output Low Voltage	I$_{OL}$ = 8mA, V$_{CC}$ = Min.	—	0.4	V
V$_{OH}$	Output High Voltage	I$_{OH}$ = –4mA, V$_{CC}$ = Min.	2.4	—	V

3514 tbl 06

DC Electrical Characteristics[1]
(V$_{CC}$ = 5.0V ± 10%, V$_{LC}$ = 0.2V, V$_{HC}$ = V$_{CC}$ – 0.2V)

Symbol	Parameter	71124S12	71124S15		71124S20		Unit
		Com'l.	Com'l.	Ind.	Com'l.	Ind.	
I$_{CC}$	Dynamic Operating Current $\overline{CS}$ ≤ V$_{IL}$, Outputs Open, V$_{CC}$ = Max., f = f$_{MAX}$[2]	160	155	155	140	140	mA
I$_{SB}$	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V$_{IH}$, Outputs Open, V$_{CC}$ = Max., f = f$_{MAX}$[2]	40	40	40	40	40	mA
I$_{SB1}$	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V$_{HC}$, Outputs Open, V$_{CC}$ = Max., f = 0[2] V$_{IN}$ ≤ V$_{LC}$ or V$_{IN}$ ≥ V$_{HC}$	10	10	10	10	10	mA

3514 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f$_{MAX}$ = 1/t$_{RC}$ (all address inputs are cycling at f$_{MAX}$); f = 0 means no address input lines are changing.

AC Test Conditions

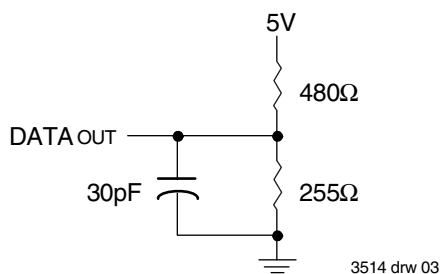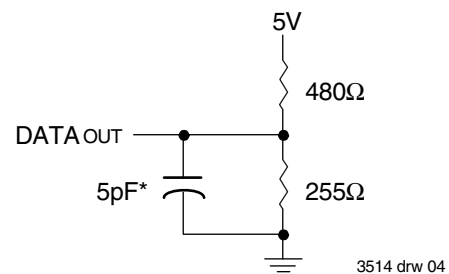|	
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figure 1 and 2

3514 tbl 08

AC Test Loads

3514 drw 03

Figure 1. AC Test Load

3514 drw 04

*Including jig and scope capacitance.

Figure 2. AC Test Load
(for t$_{CLZ}$, t$_{OLZ}$, t$_{CHZ}$, t$_{OHZ}$, t$_{OW}$, and t$_{WHZ}$)

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AC Electrical Characteristics
(V_{CC} = 5.0V ± 10%, Commercial and Industrial Temperature Ranges)

| Symbol	Parameter	71124S12[2] Min.	Max.	71124S15 Min.	Max.	71124S20 Min.	Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	12	—	15	—	20	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	0	6	0	7	0	8	ns
t_{OE}	Output Enable to Output Valid	—	6	—	7	—	8	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	0	5	0	5	0	7	ns
t_{OH}	Output Hold from Address Change	4	—	4	—	4	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	12	—	15	—	20	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End of Write	8	—	12	—	15	—	ns
t_{CW}	Chip Select to End of Write	8	—	12	—	15	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	12	—	15	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	6	—	8	—	9	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{OW}[1]	Output active from End-of-Write	3	—	3	—	4	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	0	5	0	5	0	8	ns

3514 tbl 09

NOTES:
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
2. There is no industrial temperature offering for the 12ns speed grade.

Timing Waveform of Read Cycle No. 1[1]
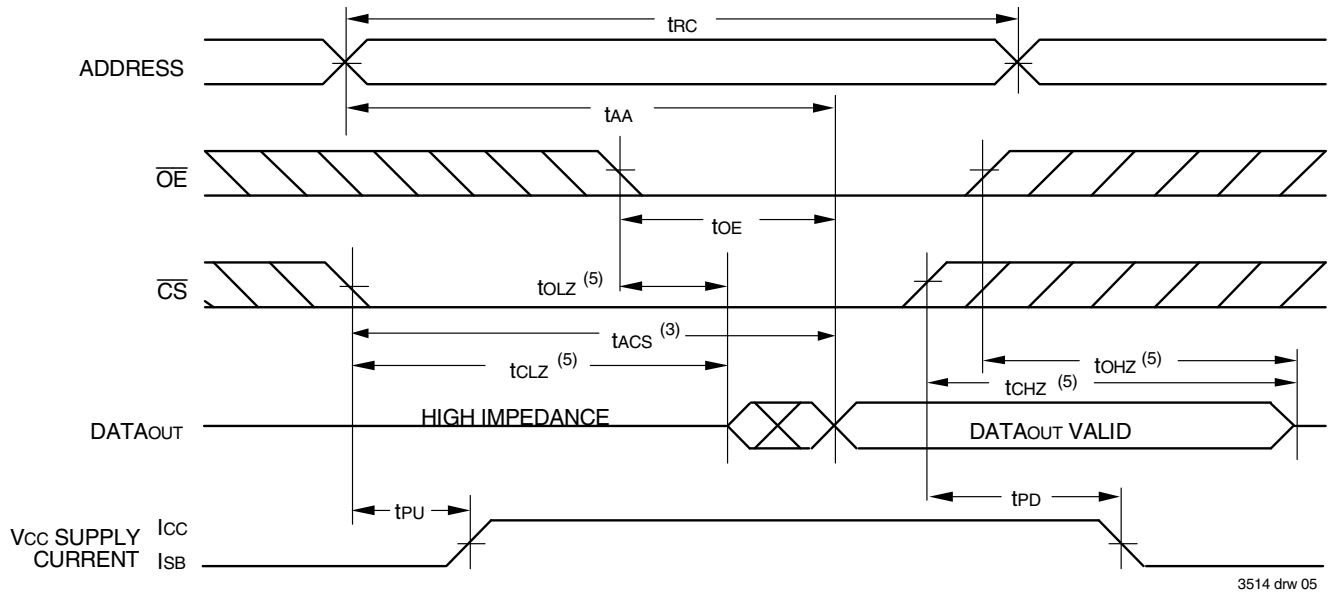
3514 drw 05

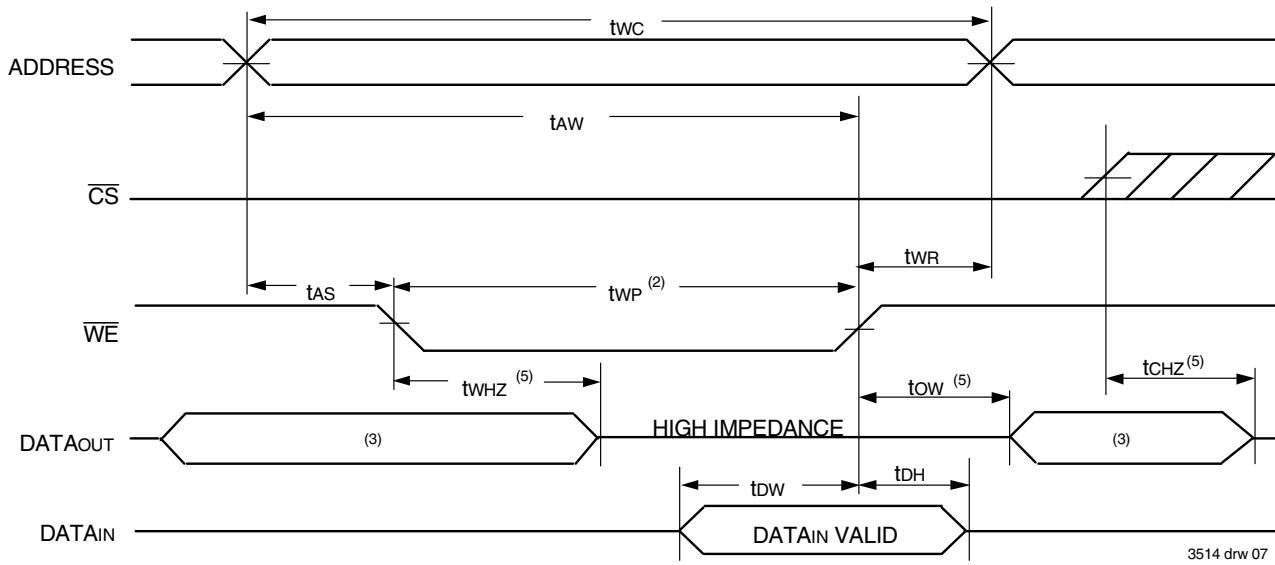## Timing Waveform of Read Cycle No. 2[1,2,4]
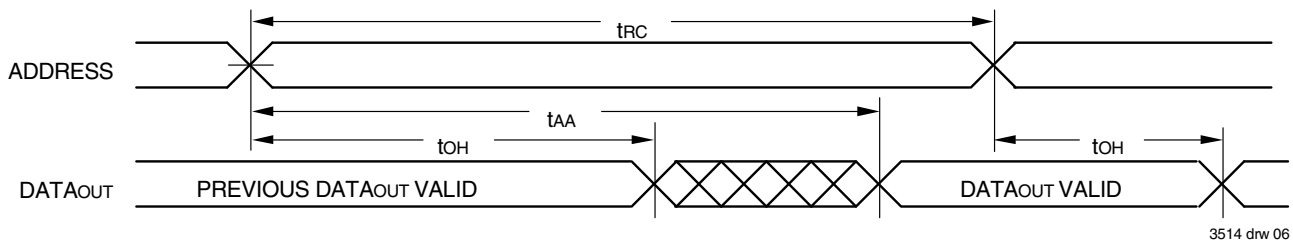
3514 drw 06

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

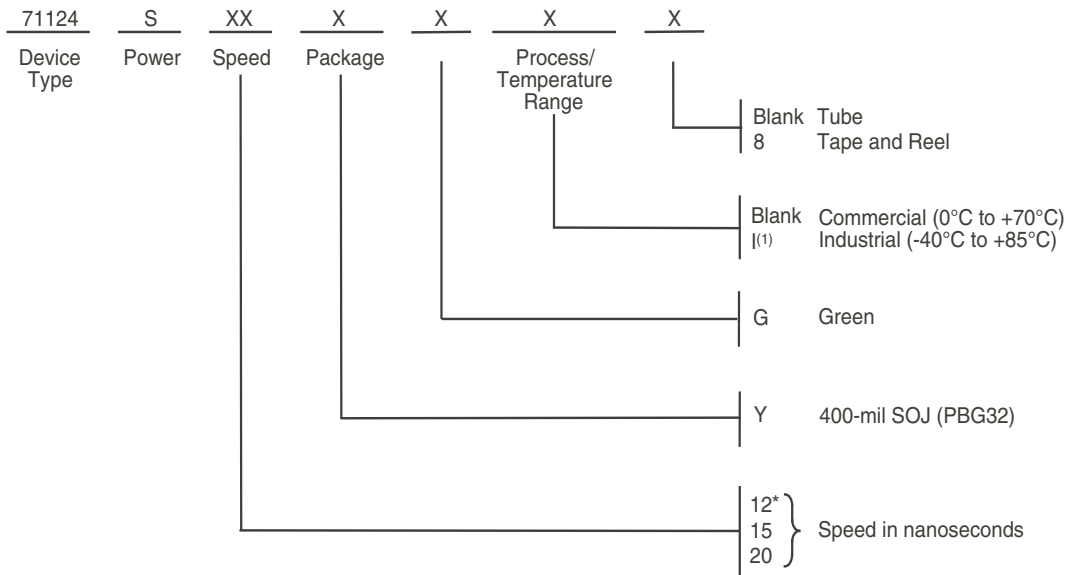## Timing Waveform of Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled Timing)[1,2,4]

3514 drw 07

Timing Waveform of Write Cycle No. 2 ($\overline{\text{CS}}$ Controlled Timing)[1,4]

3514 drw 08
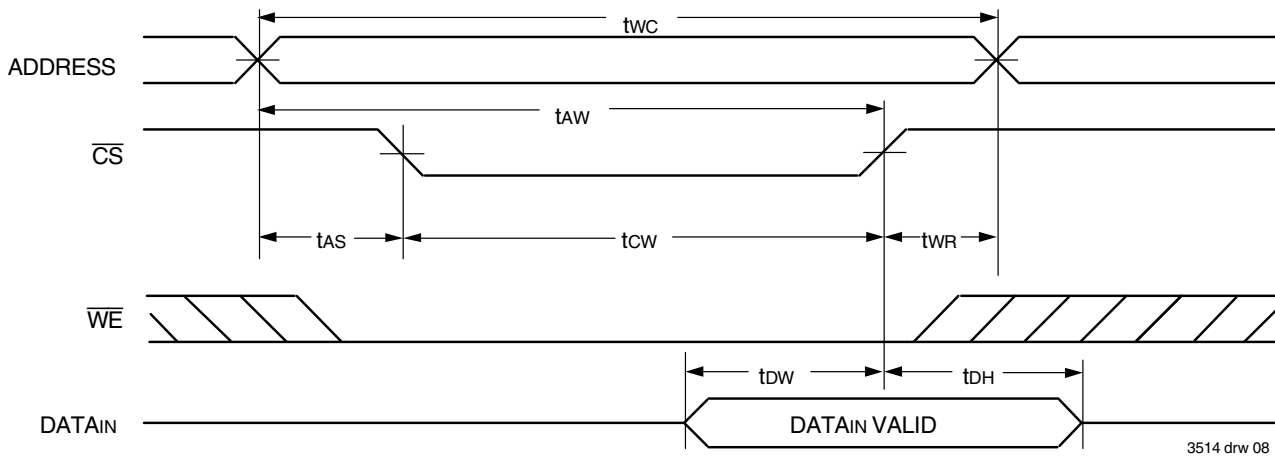
NOTES:
1. A write occurs during the overlap of a LOW $\overline{\text{CS}}$ and a LOW $\overline{\text{WE}}$.
2. $\overline{\text{OE}}$ is continuously HIGH. During a $\overline{\text{WE}}$ controlled write cycle with $\overline{\text{OE}}$ LOW, t_{WP} must be greater than or equal to t_{WHZ} + t_{DW} to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{\text{OE}}$ is HIGH during a $\overline{\text{WE}}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP}.
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the $\overline{\text{CS}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in a high impedance state. $\overline{\text{CS}}$ must be active during the t_{CW} write period.
5. Transition is measured ±200mV from steady state.

Feb.27.20 $\mathcal{R}$ENESAS

Ordering Information

```
71124      S      XX       X        X         X          X
Device   Power  Speed   Package           Process/
Type                                     Temperature
                                            Range
```

```
                                                          Blank   Tube
                                                          8       Tape and Reel

                                                          Blank   Commercial (0°C to +70°C)
                                                          I(1)    Industrial (-40°C to +85°C)

                                                          G       Green

                                                          Y       400-mil SOJ (PBG32)

                                                          12*  ⎫
                                                          15   ⎬  Speed in nanoseconds
                                                          20   ⎭
```

3514 drw 09

* No industrial temp on 12ns speed

NOTE:
1. Contact your local sales office for industrial temp range for other speeds, packages and powers.

Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
12	71124S12YG	PBG32	SOJ	C
	71124S12YG8	PBG32	SOJ	C
15	71124S15YG	PBG32	SOJ	C
	71124S15YG8	PBG32	SOJ	C
	71124S15YGI	PBG32	SOJ	I
	71124S15YGI8	PBG32	SOJ	I
20	71124S20YG	PBG32	SOJ	C
	71124S20YG8	PBG32	SOJ	C
	71124S20YGI	PBG32	SOJ	I
	71124S20YGI8	PBG32	SOJ	I

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Datasheet Document History

08/05/99:		Updated to new format
	Pg. 3	Removed military entries on DC table
	Pg. 4	Removed Note 1 and renumbered footnotes
	Pg. 6	Revised footnotes on Write Cycle No. 1 diagram
08/13/99:	Pg. 8	Added Datasheet Document History
09/30/99:	Pg. 1, 3, 4, 7	Added 12ns, 15ns, and 20ns industrial temperature speed grade offerings
02/18/00:	Pg. 3	Revise I_{SB} for Industrial Temperature offerings to meet commercial specifications
03/14/00:	Pg. 3	Revised I_{SB} to accommodate speed functionality
04/01/00:	Pg.4	Tightened tAW, tCW, tWP and tDW within the AC Electrical Characteristics
08/09/00:		Not recommended for new designs
02/01/01:		Removed "Not recommended for new designs"
10/23/08:	Pg.7	Removed "IDT" from the orderable part number
04/02/13:	Pg.1	Removed 12ns speed from the Industrial temp offering. Removed IDT in reference to fabrication
	Pg.3	Removed the industrial 12ns speed grade information from the DC Electrical Chars table 07
	Pg.4	Added footnote 2 to AC Electrical Chars table 09 to indicate that there is no industrial 12ns speed
	Pg.7	Added Tape & Reel and Green designators to the ordering information. Added a footnote to the ordering information to indicate that there is no industrial 12ns speed offering
02/27/20:	Pg. 1-9	Rebranded as Renesas datasheet
	Pg. 2-7	Updated package code
	Pg. 7	Added Industrial temp footnote to the Ordering Information
	Pg. 7	Added Orderable Part Information table

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