3.5A Peak Current 100V High Side Step-Down Converter

LA1812

Overview


SOP8L

LA1812 is a step down converter. It can be used to convert 100V input voltage to 2.5~30V output. LA1812 integrates 100V power MOS with super low R_{DSON}, to get low power loss. It applies variable off-time control mode and frequency jitter is added. EMI is easy to design. The startup current is designed to be as low as 5uA, make it easy to use in low power design. Built-in loop compensation, no need for extra compensation components. It can be worked both in CCM and DCM. With adjustable current limit. Innovated FB2 design, make the high side buck structure better. The transient and no load performance were improved a lot. And the size of the system can be decreased dramatically.

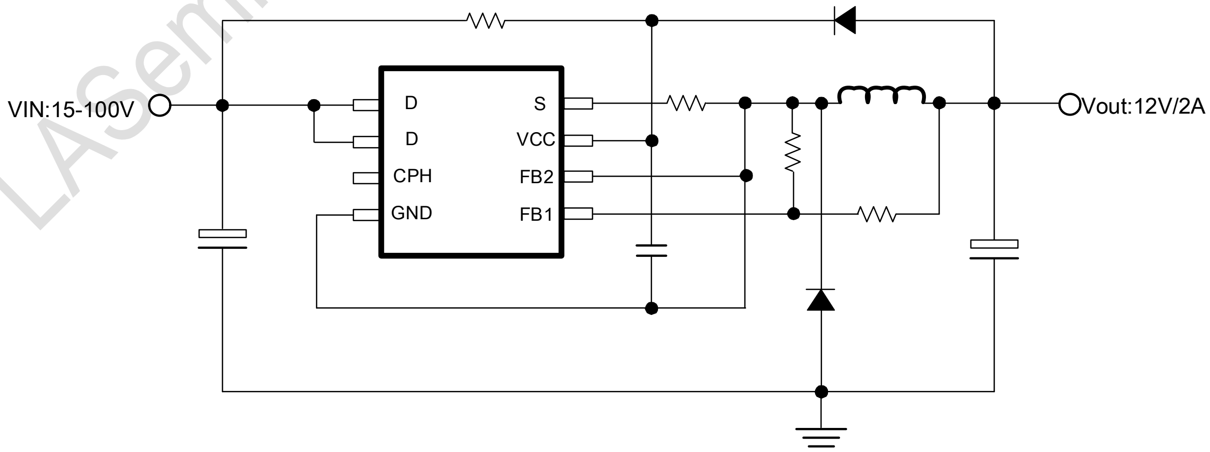
Features

- 15V to 100V Wide Input Range
- 3.5A Peak Current
- High-Side Buck Control
- Innovate FB2 Control for Fast Transient Response
- Wide VCC operating range
- 100V/0.23Ω power MOSFET
- Frequency Jittering
- Adjustable Peak Current Limit
- Low Standby Current
- Simple System Design Built-in Loop Compensation
- Low audible noise
- Full Protection OCP, SCP, OTP
- Available in SOP8 package

Application

- Motor Driver power supply
- E-bike
- Industry Control

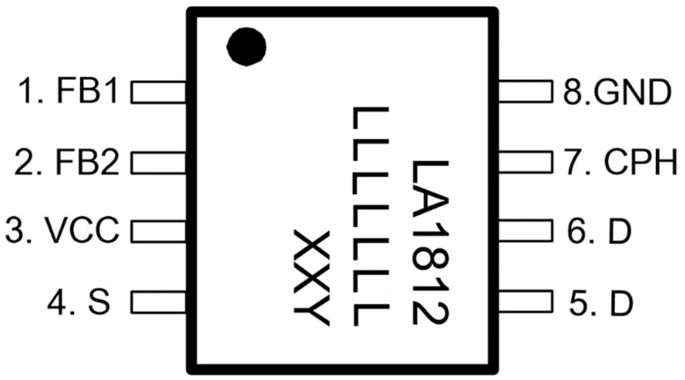
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1812	SOP8L	-40 to 125^{0}C	T/R 2500pcs/Roll	sales@latticeart.com

Pin Diagram

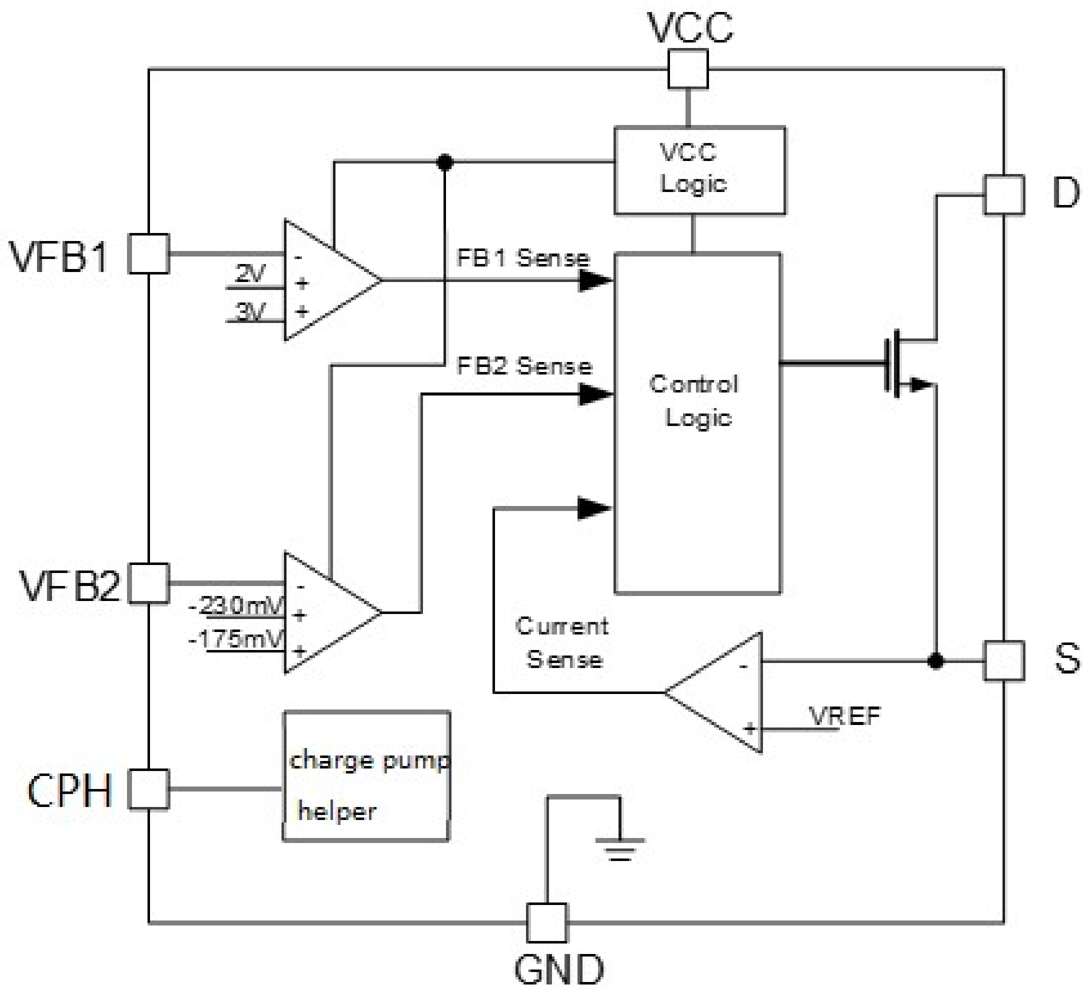


LA1812: Product code
LLLLLLL: IC Lot number
XX: Week number
Y: Year code

Pin Description

Pin No.	Symbol	Pin Description
1	FB1	**Feedback pin.** This pin will sense the voltage of the output when diode is conducting current. Connect a resistor divider between OUT and chip GND to set the output voltage.
2	FB2	**Feedback2.** FB2 will sense the output voltage at Hi-Z state. Connect a resistor divider between chip GND and output GND to sense the output voltage. Short to chip GND to disable the FB2 detection.
3	VCC	IC internal logic circuitry power supply.
4	S	**Source of the power MOS**. Also served as the current sense pin.
5,6	D	**Drain node of the power MOS.** In buck configuration, connect this pin to VIN of the system.
7	CPH	**Charge pump helper.** Use CPH pin when output voltage is in the range of 2.5 to 4.5V. Float if not used
8	GND	**IC ground.** In buck configuration, it serves as the switching load of the system.

Block Diagram



Absolute Maximum Ratings (note 1)

T_A=25°C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
D	Power MOSFET input voltage, D to S	-0.3~105	V
I_{load}	Output load current	2	A
VCC	Power supply for IC, VCC to GND	-0.5~32	V
FB1	Output feedback signal, FB1 to GND	-0.5~4.5	V
FB2	FB2 to IC GND, FB2 to GND	-0.5~0	V
S	Power MOSFET source, S to GND	-0.3~4.5	V
T_{STG}	Storage temperature	-55 to150	°C
T_j	Junction temperature	-40 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
VCC	Power supply pin for low side	2.5 to 30	V
D	Power MOSFET input voltage	≤100	V
Tj	Junction temperature	-40 ~ 125	°C

Thermal Resistance (note 2)

Symbol	Definition	Ratings	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	90	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	45	°C/W

Note 2: Measured on JESD51-7, 4-Layer PCB, and the PCB has no copper for thermal dissipation. Normal PCB with copper thermal resistance will be smaller.

Electrical Characteristics

T_A=25^{0}C, VCC=12V, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VCC						
V_{CC_clamp}	VCC clamped voltage	I_{CC}=2mA		20		V
V_{CC_OVP}	VCC Over Voltage protection threshold		28.6	30	31.4	V
V_{CC_start}	VCC startup threshold	VCC rises up	9.2	9.7	10.3	V
V_{CC_stop}	VCC shutdown voltage	VCC ramps down	4	4.15	4.3	V
I_{st}	VCC startup current	Vcc=Vcc_start -1V T_J= -40° ~ +125°C		2.5	10	uA
I_{op}	VCC quiescent operation current	VFB=2.2V, Vcc=19V		63		uA
FB1						
V_{FB1_REF}	FB1 regulation reference voltage		1.99	2.05	2.11	V
T_{Sample_BLK}(3)	FB1 sample blanking time after power MOS off			1.4		us
T_{ONMAX}	Maximum turn on time			30		us
T_{OffMAX_ECO}	Maximum turn off time during standby mode			20		ms
FB2						
V_{FB2ACT}	FB2 active threshold			-30		mV
V_{HOLD}	FB2 over voltage threshold		-244	-233	-221	mV
V_{WAKEUP}	FB2 standby mode Wakeup threshold		-191	-179	-167	mV
T_{SAMPLE_BLK}(3)	FB2 sample blanking time	After ZC is detected	6			us
T_{SAMPLE_BLKMAX}	MAX FB2 sample blanking time	After power MOS off.		83		us

Electrical Characteristics

T_A=25^{0}C, VCC=12V, unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Current Sense						
$V_{CS\_PK\_MAX}$	Max Current limit voltage		300	312	324	mV
$V_{CS\_PK\_MIN}$	Min current limit voltage at low load state			0.4		$V_{CS\_PK\_MAX}$
T_{LEB}	Leading edge blanking time			250		ns
Internal Power MOSFET						
R_{DSON}	Drain-source Turn-On Resistance			0.23		ohm
Frequency &Timing Part						
T_{MINOFF}	Minimum off time		6.2	6.8	7.5	us
Over Temperature Protection (OTP)						
T_{OTP}(4)	Over temperature threshold			150		℃

Note 3: Guaranteed by Design

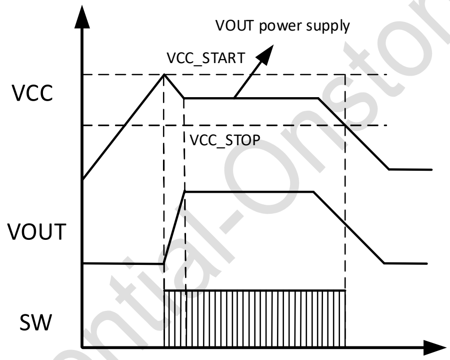
Note 4: Not tested in production and derived from bench characterization.

Function Descriptions

LA1812 is peak current mode control green mode operation regulator. The power MOSFET ON time is controlled by the peak current limit. IC controls the OFF time to regulate the output voltage. LA1812 switching frequency will decrease with load decreasing. As a result, LA1812 can achieve excellent light load efficiency. LA1812 can work in continuous current mode (CCM) and discontinuous current mode (DCM) based on the load current condition. Built-in loop compensation, no need for extra compensation components and simple the design.

Startup and Input Under Voltage Lockout

Before IC starts switching, LA1812 VCC start current is as low as 2.5μA typ. VCC can be charged by the pull resistor from VIN. IC remains low start current consumption until VCC charged above (V_{CC_START}) 9.7V. After VCC charged above V_{CC_START}, IC starts switching, output will go up and supply the VCC via the external diode. The VCC supply voltage needs to be higher than (V_{CC_STOP}) 4.15V.
When VCC voltage falls below the V_{CC_STOP}, LA1812 will stops switching to avoid abnormal operation. VCC need to be recharged to V_{CC_START} to restart the IC. Proper pull-up resistor needs to be designed to achieve short circuit or over temperature protection.



Startup Timing

Output Voltage Regulation

LA1812 can regulate the output voltage under different load and input voltage condition. Whenever High-side (HS) power MOSFET is off, FB1 will become the sensor of the output voltage. After a Tsenseblk blanking time when the HS power MOSFET is off, VOUT will be sensed via FB1 and sent to internal error amplifier. The output of the error amplifier will control the timing of next on pulse, also it controls the peak current. To keep the VOUT stable at different load condition: it adjust the switching frequency and I_{PK} to regulate the output voltage.
LA1812 will enter Eco mode under extremely light load or no-load condition to avoid IC cannot monitor FB1 for a long time. In Eco mode, the maximum off time is 20ms typical.

Output Under Voltage Protection and Over Voltage Protection

LA1812 has innovated FB2 to improve the load transient performance of High-side buck structure design. When HS power MOSFET is off, the inductor current will drop to 0A and then IC enters Hi-Z state. FB2 monitors the VOUT via the shunt resistor from VOUT+ to VOUT-. At this period IC GND connect to VOUT+ via the inductor. VOUT- is negative VOUT voltage to the IC. In normal operation, FB2 is designed in the range between -179mV and -233mV. If the voltage of FB2 is higher than -179mV in Hi-Z state, IC will consider it to be VOUT under voltage which might be caused by load transient. Then it will start a new pulse immediately to avoid VOUT drops lower. On the other hand, if FB2's voltage is lower than -233mV in the Hi-Z state, then IC will consider it to be VOUT over voltage. No pulse will be allowed any more to avoid VOUT overshoot higher even if the off time is longer than the MAX off time 20ms.

Connect the FB2 pin to chip GND will disable the FB2 detection.

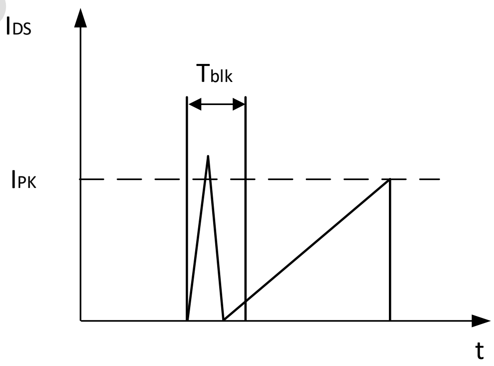
Feedback Open Output Over Voltage Protection

LA1812 can achieve VOUT over voltage protection in feedback open condition via VCC pin. LA1812 VCC working range is from 4.15V to 30V. Because VCC voltage is bias by VOUT through the external diode, VCC voltage will increase with VOUT. When VCC voltage goes above 30V, the VCC over voltage protection will be triggered. IC will be shut down and stop switching. VCC will be discharged by an internal 6mA current source. IC will stops switching until VCC drops to V_{CC_STOP}. Then the internal 6mA current source will be disconnected and VCC will be recharged up by the external pull up resistor. IC restart when VCC voltage rise above V_{CC_START}. LA1812 repeats this operation cycle until the VCC over-voltage condition disappears and the output voltage rise smoothly back the regulation level.

Current Sense

The LA1812 sensed the current in HS power MOSFET through the external Rcs resistor. When the sense voltage Vcs_pk is triggered, IC will shut down the power MOSFET. The peak current determined by the Rcs resistor. The maximum I_{PK} can be set by V_{CS_PK}/R_{CS}. The peak current will decrease with the load decreasing and the minimum I_{PK_MIN} is $V_{CS\_MIN}/R_{CS} = V_{CS\_PK\_MAX}/(2.5*R_{CS})$. To avoid V_{CS_PK} triggered by the spike current caused by the parasitic capacitance and reverse recovery current of the freewheeling diode and result in HS power MOSFET falsely off, LA1812 has implemented a blanking time (Tblk) after HS power MOSFET turns on. During the blanking time, the current limit comparator will be disabled.

LA1812 I_{PK} can be programmed by the external Rcs resistor. Recommend not to set I_{PK} higher than 3.5A.



Current Sense Blanking

Over Current and Short-Circuit Protection

The LA1812 max output current is limited by minimum off time and peak current limit. Increases the load current, the IC switching frequency will increase until reaches the DCM to CCM critical condition. If keep increasing the load, the frequency cannot be increased due to inductor current peak and value limitation, so VOUT starts to drop. Due to VCC is biased by VOUT via the diode, VCC will drop followed the VOUT. When VCC voltage drops below the V_{CC_STOP}, IC stops switching enter hiccup protection. Then VCC voltage will be recharged up by the pull resistor from VIN to VCC. IC will restart after VCC is charged to V_{CC_START}. LA1812 repeats this operation cycle until the over-current condition disappears, and the output voltage rises smoothly back to the regulation level.

Switching Frequency and Audible Noise Reduction

LA1812 is peak current control mode. IC switching frequency will decrease with load decreasing to achieve excellent light load efficiency. When LA1812 switching frequency is much higher than 20k, the switching frequency can be estimated by below two formulas:

$$F_{SW} = \frac{2(V_{IN} - V_O)}{L * I_{PK}^2} * \frac{V_O * I_O}{V_{IN}}, \text{ DCM}$$

$$F_{SW} = \frac{(V_{IN} - V_O)}{2L * (I_{PK} - I_O)} * \frac{V_O}{V_{IN}}, \text{ CCM}$$

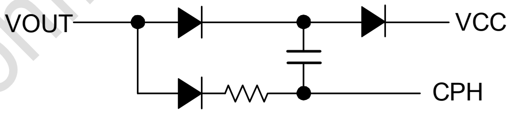
The LA1812 will gradually reduce the peak current to minimum, which is 0.4 times of the max peak current set by sense resistor when switching frequency drops to 20KHz. The inductor current can be greatly reduced in this condition and the load range of enter the audible noise will become smaller. After system frequency enter the audible noise range, the smaller inductor energy will reduce the noise caused by the inductor vibration.

Green Mode Operation

LA1812 switching frequency will decrease with load decreasing. As a result, LA1812 can achieve excellent light load efficiency. Different with traditional burst mode, the LA1812 switching cycle can automatically decrease to 20ms maximum. As a result, the light load ripple voltage and voltage overshoot has optimized.

Low Output Voltage Operation

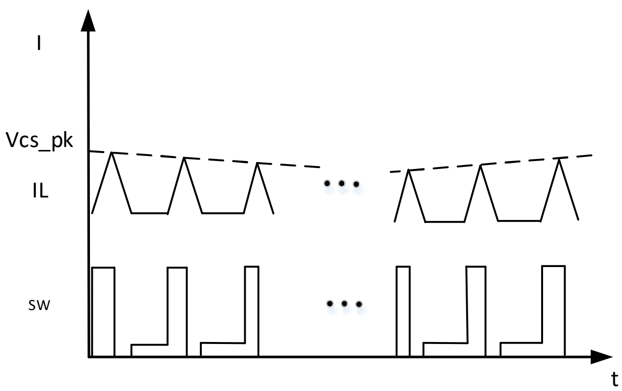
When output is set in the range of 2.5V to 4.5V, the VCC voltage will be too low to drive the internal MOSFET. CPH pin can be used to charge pump the VCC voltage to two times of the output voltage with below circuit.



External Charge Pump Circuit for 2.5V to 4.5V Output

EMI Reduction

LA1812 achieves the switching frequency jitter by modulate the V_{CS_PK}. By doing this, EMI noise peak caused by the switching frequency noise will be greatly reduced, simplify the EMI design and reduce the solution cost.

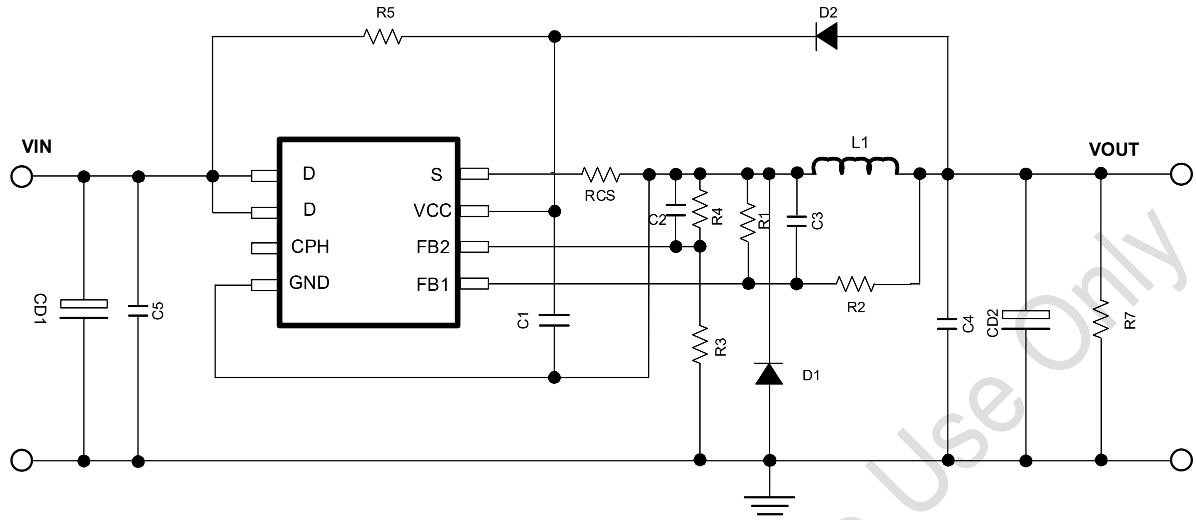


Frequency Spread Spectrum

Over Temperature Protection

LA1812 has built-in accurate over temperature protection. It monitors the MOSFET temperature and improves the system reliability. Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the MOSFET temperature exceeds 150°C, the entire chip shuts down. When MOSFET temperature drops below 150°C, system will discharge and recharge VCC cap to achieve the thermal restart delay and restart the IC.

Application Information



Setting the FB1 Resistor

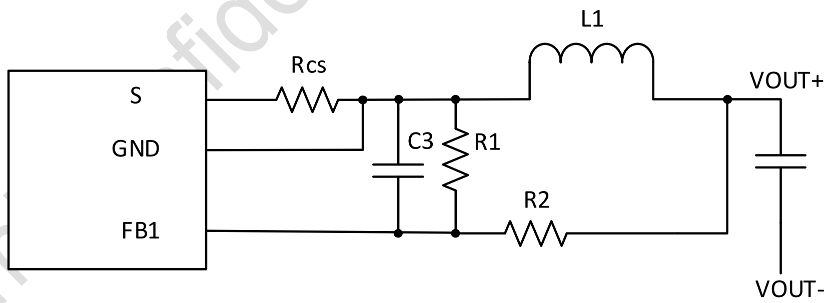
LA1812 output voltage can be set by the external resistor dividers on FB1 pin. Equation as below:

$$V_{OUT} = 2.05 * \left(1 + \frac{R_2}{R_1}\right) - 0.7$$

While 0.7V is the forward voltage drop of the freewheeling diode.

Normally use a value around 10K for R1 resistor. To avoid the noise to the FB1 pin, recommend to use a 10pF/50V capacitor in parallel with R1 resistor. For 5V Output example, choose 22K for R1,40K for R2. Then the operating output voltage is:

$$V_O = 2.05 * \left(1 + \frac{40K}{22K}\right) - 0.7 = 5.07V$$

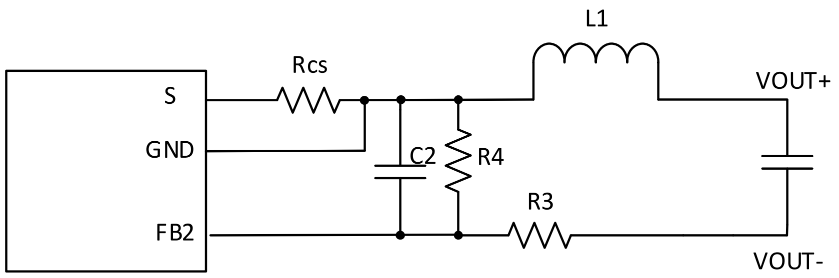


FB1 Feedback Network

Setting the FB2 Resistor

FB2 can be used to set the wake-up voltage under no-load condition. Connect the FB2 to chip GND will disable the FB2 detection. If FB2 wake-up threshold is not triggered within Toff max 20ms, then IC will work under 20ms typical switching cycle. If FB2 wake-up threshold is triggered within 20ms, LA1812 will wake up and start normal operating immediately to achieve fast loop response. If FB2 voltage is lower than -0.233V, no pulse will be allowed any more to avoid VOUT overshoot higher even if the off time is longer than the MAX off time 20ms. So in no-load output voltage max value is determined by below formula:

$$V_{O\_MAX} = 0.233 * (1 + \frac{R_3}{R_4})$$



FB2 Feedback Network

Wake-up voltage is set by FB2. When FB2 below 0.179V IC will wake-up. Wake up voltage can be set by below formula:

$$V_O = 0.179 * \left(1 + \frac{R_3}{R_4}\right)$$

Setting the Max Output Current

If IC works in CCM mode, so the max output current will be determined by below formula:

$$I_{O-\max} = I_{PK} - \frac{V_{IN} - V_O}{2.L.F_{SW}} * \frac{V_O}{V_{IN}}$$

If IC in DCM to CCM critical mode under max output condition. So the max output current will be determined by below formula:

$$I_O = \frac{I_{PK}}{2}$$

While I_{PK} is the inductor peak current. I_{PK} is determined by Rcs with below formula:

$$I_{PK} = \frac{V_{CS\_PK}}{R_{CS}}$$

Note: need to choose 1% accuracy with good temperature coefficient resistor for Rcs to achieve good production and over temperature consistency.

Selecting the Inductor and Set the Switching Frequency

In this case the switching frequency can be estimated by below formulas:

$$F_{SW} = \frac{2(V_{IN} - V_O)}{L * I_{PK}^2} * \frac{V_O * I_O}{V_{IN}}, \text{ DCM}$$

$$F_{SW} = \frac{(V_{IN} - V_O)}{2L * (I_{PK} - I_O)} * \frac{V_O}{V_{IN}}, \text{ CCM}$$

Consider the EMI performance and PCB solution size. Recommend to set the switching frequency below 100KHz. Too high switching frequency will result in thermal and EMI issue. Too low switching frequency will increase the solution size and increase the inductor and capacitor value.

Selecting the Startup Resistor and VCC Capacitor

LA1812 VCC start current is as small as 2.5uA typical. Choose a pull-up resistor with higher than 10μA will be enough. When design to achieve low no-load power consumption, choose a large pull-up resistor to reduce the input current. When design to achieve fast startup, choose a small pull-up resistor. Recommend not to choose Schottky diode due to the Schottky diode will have large leakage current at high temperature. If must use

Schottky diode need choose smaller pull-up resistor to avoid startup failure at high temperature. Normally choose a value between100K to 1MΩ for the pull-up resistor.

Choose 1μF to 4.7μF capacitor for VCC cap. Due to after IC starts switching VCC will consume more current and pull-up resistor may not be able to supply. VCC need to be supplied by the VOUT via the external diode. If output capacitor is too big, need to choose a larger VCC cap to avoid VCC drop below V_{CC_STOP} before VOUT ramp up.

Selecting the Output Capacitor

Output capacitor is used to maintain the output voltage. The steady state ripple voltage can be calculated with below formula:

$$V_{OUT\_ripple} = \frac{I_{PK}}{8F_{SW} * C_{OUT}} + I_{PK} * R_{ESR}$$

Recommend to choose low ESR Aluminum electrolytic capacitor to reduce the output ripple voltage.

Due to the FB2 design, LA1812 has good transient performance. Doesn't need to use too large output capacitor to achieve the transient requirement. The output capacitance can be reduced if the full load condition reduced.

Startup

Before startup, LA1812 only takes very low current from VCC. The startup current through the startup resistor will charge VCC. Till VCC reaches 9.7V.

When VCC voltage reaches 9.7V, LA1812 will start work. VOUT will get high, then the diode between VOUT and VCC will keep VCC voltage higher than 4.15V. Or if VOUT is abnormal, VCC cannot be hold higher than 4.15V, then the system will protect and restart. At start up, a current loop will work to prevent the inductor current to be out of control.

Output voltage regulation

LA1812 will sense the output voltage 1.4us after the power MOS is off, and send it to internal error amplifier.

The output of the error amplifier will control the timing of next on pulse, also it controls the peak current. To keep the output voltage stable at different load condition: it adjust the switching frequency and I_{PEAK} to fulfill the output load.

After the inductor current drops to 0, or 70us after the power MOS is off. LA1812 will begin to sense the output voltage through FB2. and react if the FB2 is over or under voltage.

Firstly, to active the FB2 sense function, the voltage on this pin should lower than -30mV. If this pin is short to GND, then the part will disable the FB2 sense function.

Then if the voltage of FB2 is in the range between -170mV and -230mV, it consider to be normal, and the part will do nothing.

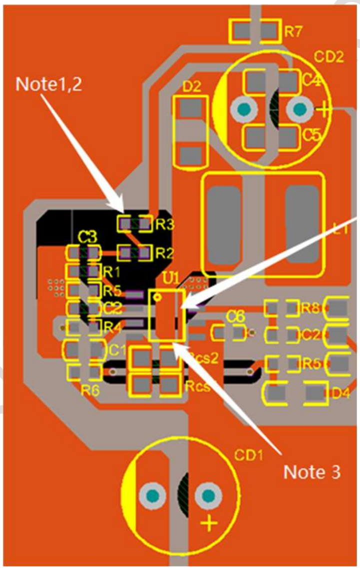
If the voltage of FB2 is higher than -179mV, then the part will consider this situation as Vout undervoltage, which might be caused by load transient. Then it will start a new pulse at once, to prevent Vout from dropping anymore.

On the other hand, if FB2's voltage is lower than -233mV, then the part will consider this situation as Vout OV. No pulse will be allowed any more, even if the off time is longer than the MAX off time, 20ms.

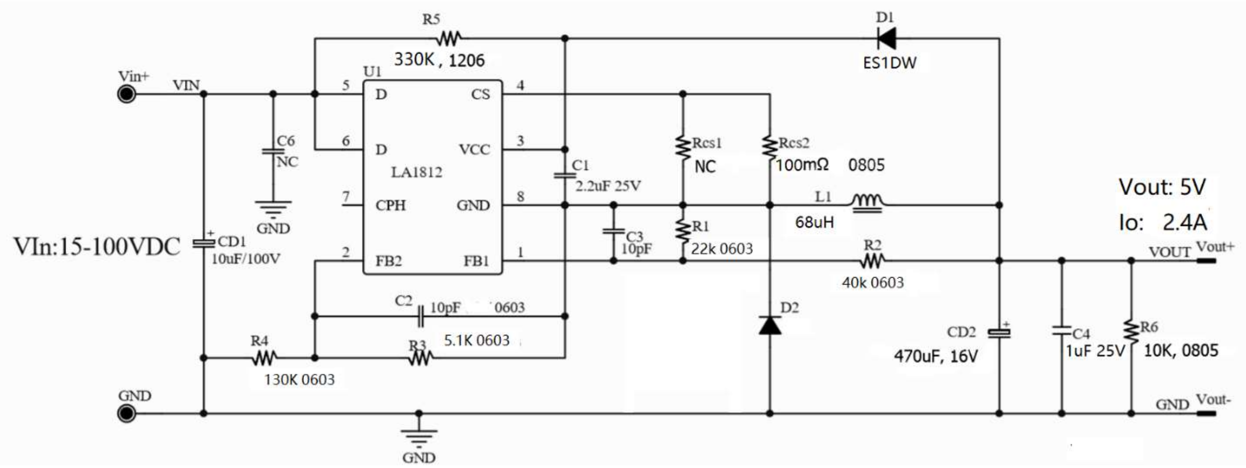
PCB layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below.

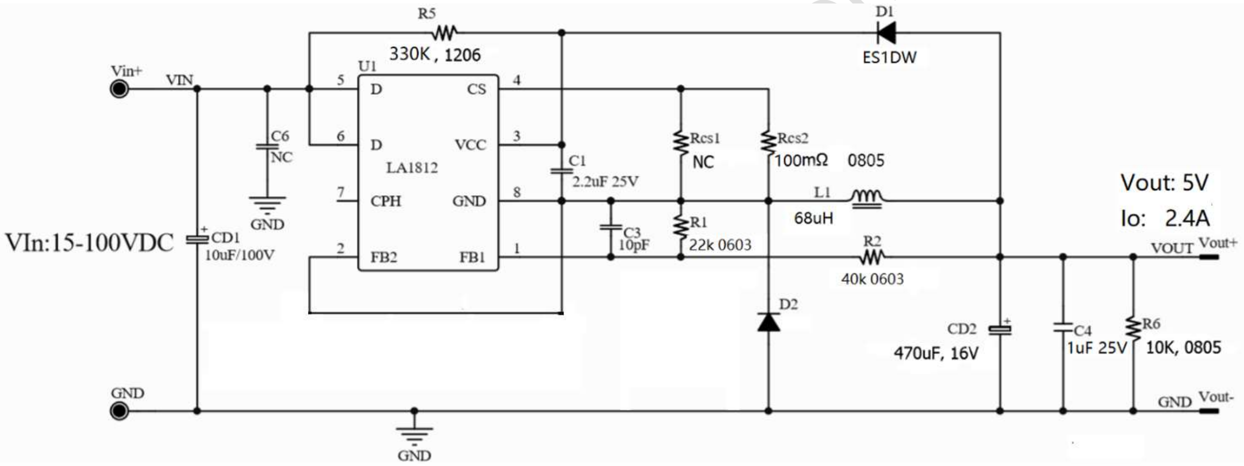
- Minimize the power loop area formed by the input capacitor, IC, freewheeling diode, inductor and output capacitor.
- Don't put the heat sourcing device close to each other on the PCB to achieve good thermal performance. The heat sourcing device are: Rectifier bridge, LA1812, inductor, freewheeling diode.
- Keep the current sense resister as close as possible to the part.
- Kelvin connect the part's GND to the Neg node of the sense resistor.
- For double-sided PCB don't do cross line on the power trace to achieve good EMI.
- Place the external feedback resistors as close to FB1 and FB2 as possible. The FB1 and FB2 resistor need to be placed always from the Drain node of LA1812.
- Use large copper area on LA1812 Drain to achieve good heat dissipation.



Typical Application Circuit



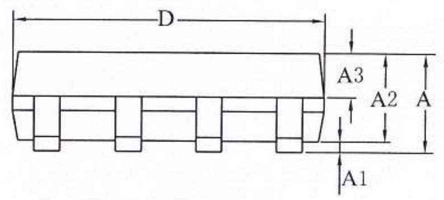
VOUT=5V/2.4A with FB2 Wakeup

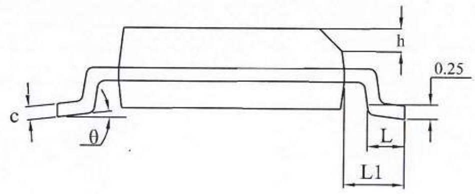


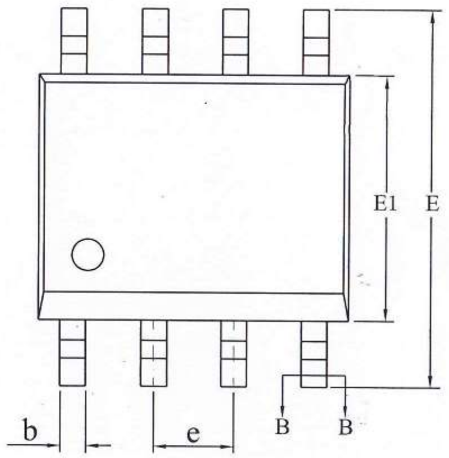
VOUT=5V/2.4A without FB2 Wakeup

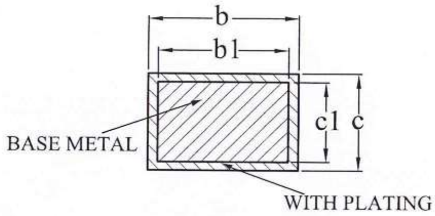
Detail Package Outline Drawing

Package type: SOP8L









SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°