

● General Description

The AGM30P25MBQ combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

● Features

- Advance high cell density Trench technology
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance
- 100% Avalanche tested
- 100% DVDS tested

● Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
AGM30P25MB	AGM30P25MBQ	WQFN3.3*3.3	330mm	12mm	5000

Table 1. Absolute Maximum Ratings (Tc=25°C)

Symbol	Parameter	Value	Unit
VDS	Drain-Source Voltage (VGS=0V)	-30	V
VGS	Gate-Source Voltage (VDS=0V)	±20	V
ID	Drain Current-Continuous(Tc=25°C) (Note 1)	-8	A
	Drain Current-Continuous(Tc=100°C)	-4.8	A
IDM (pluse)	Drain Current-Continuous@ Current-Pulsed (Note 2)	-32	A
PD	Maximum Power Dissipation(Tc=25°C)	28	w
	Maximum Power Dissipation(Tc=100°C)	11	w
EAS	Avalanche energy (Note 3)	65	mJ
TJ,TSTG	Operating Junction and Storage Temperature Range	-55 To 150	°C

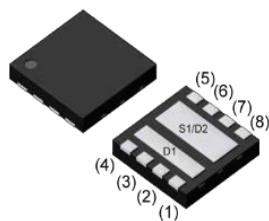
Table 2. Thermal Characteristic

Symbol	Parameter	Typ	Max	Unit
RθJA	Thermal Resistance Junction-ambient (Steady State) ¹	---	50	°C/W
RθJC	Thermal Resistance Junction-Case ¹	---	4.4	°C/W

Product Summary

BVDSS	RDSON	ID
-30V	20mΩ	-8A

WQFN3*3 Pin Configuration



- (1) Tr1 Gate
- (2) Tr1 Drain
- (3) Tr1 Drain
- (4) Tr1 Drain
- (5) Tr2 Source
- (6) Tr2 Source
- (7) Tr2 Source
- (8) Tr2 Gate

*1 Body Diode

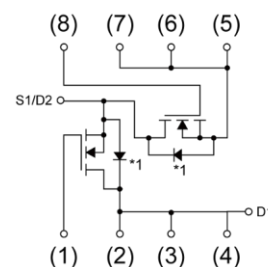


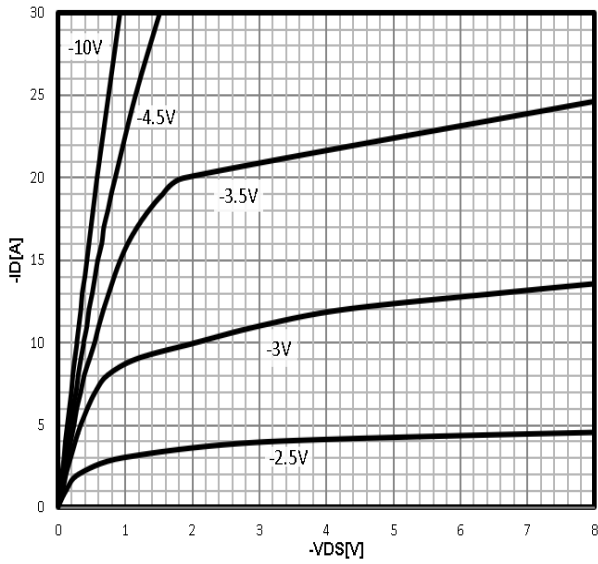
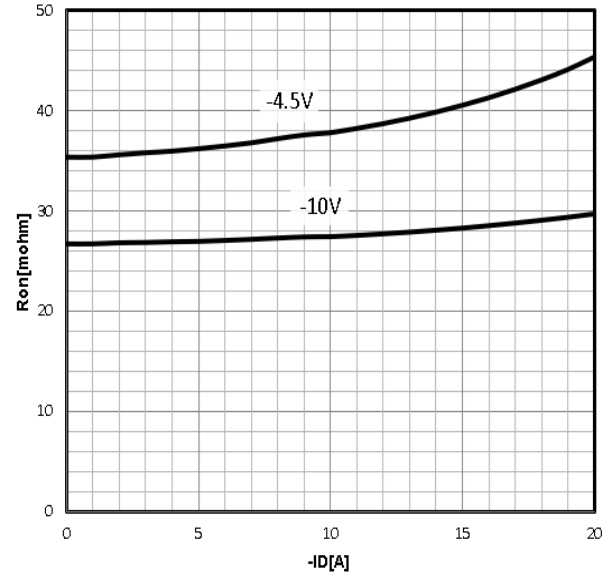
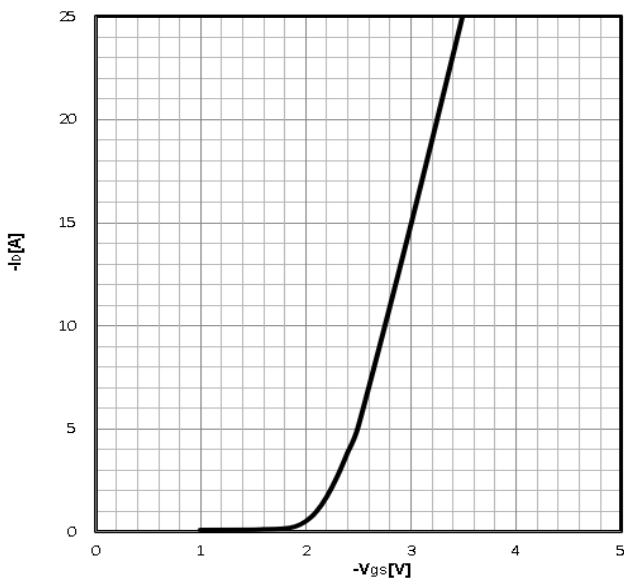
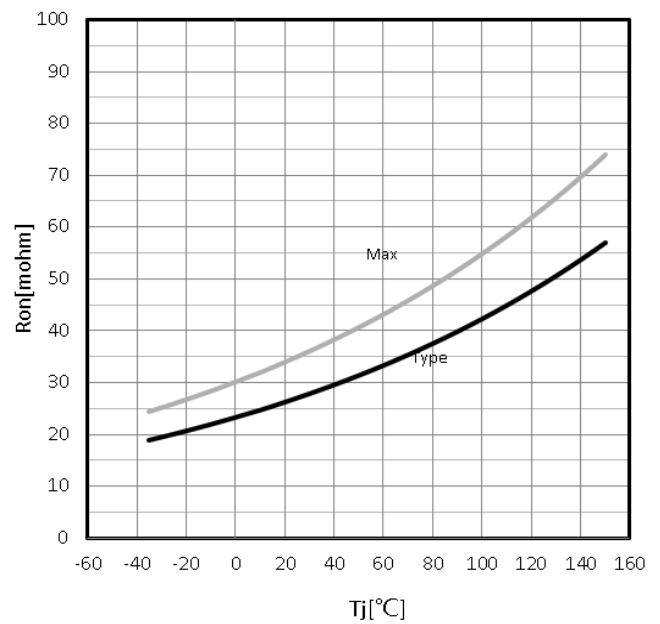
Table 2. P-Channel Electrical Characteristics (Tc=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On/Off States						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V ID=-250μA	-30	--	--	V
IDSS	Zero Gate Voltage Drain Current	VDS=-30V,VGS=0V	--	--	-1	μA
IGSS	Gate-Body Leakage Current	VGS=±20V,VDS=0V	--	--	±100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS,ID=-250μA	-1.2	-1.5	-2.5	V
gFS	Forward Transconductance	VDS=-10V,ID=-4A	--	6	--	S
RDS(on)	Drain-Source On-State Resistance	VGS=-10V, ID=-5A	--	20	24	mΩ
		VGS=-4.5V, ID=-4A	--	29	34	mΩ
Dynamic Characteristics						
Ciss	Input Capacitance	VDS=-15V,VGS=0V, F=1MHZ	--	652	--	pF
Coss	Output Capacitance		--	95	--	pF
Crss	Reverse Transfer Capacitance		--	85.7	--	pF
Switching Times						
td(on)	Turn-on Delay Time	VGS=-10V,VDS=-15V, ID=-4A,RGEN=3Ω, RL=3.6Ω	--	8	--	nS
tr	Turn-on Rise Time		--	4	--	nS
td(off)	Turn-Off Delay Time		--	26	--	nS
tf	Turn-Off Fall Time		--	12.5	--	nS
Qg	Total Gate Charge	VGS=-10V, VDS=-15V, ID=-1A	--	14	--	nC
Qgs	Gate-Source Charge		--	1.34	--	nC
Qgd	Gate-Drain Charge		--	2.99	--	nC
Source-Drain Diode Characteristics						
ISD	Source-Drain Current(Body Diode)		--	--	-8	A
VSD	Forward on Voltage	VGS=0V,IS=-5A	--	--	-1.2	V
trr	Reverse Recovery Time	IF=-5A , dI/dt=100A/μs , TJ=25°C	--	--	--	ns
Qrr	Reverse Recovery Charge		--	--	--	nc

Notes 1.The maximum current rating is package limited.

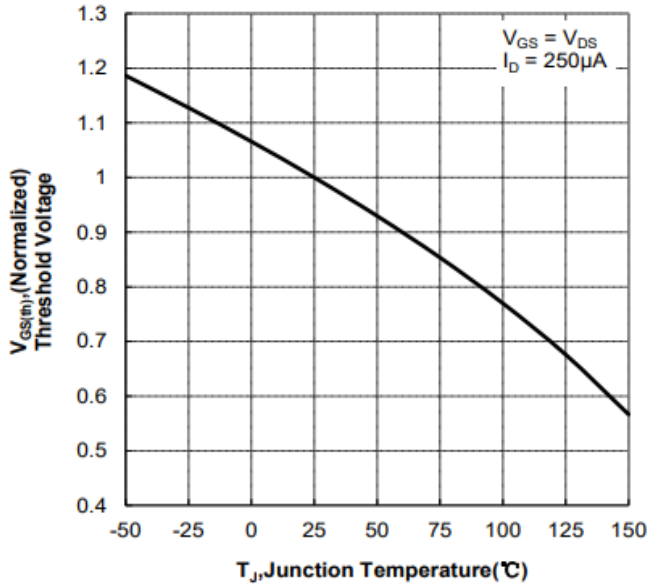
Notes2.Repetitive Rating: Pulse width limited by maximum junction temperature Notes

3.EAS condition: TJ=25°C

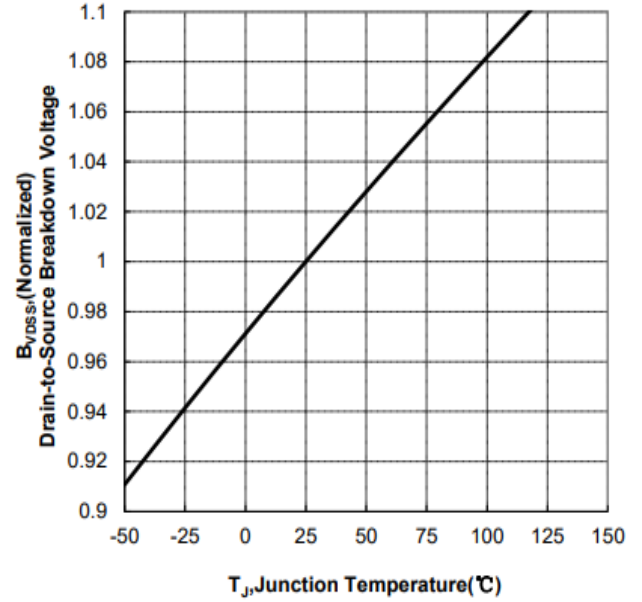
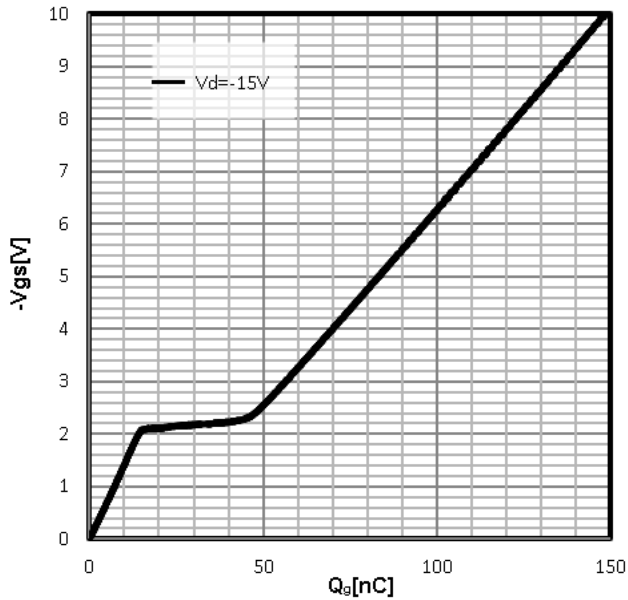
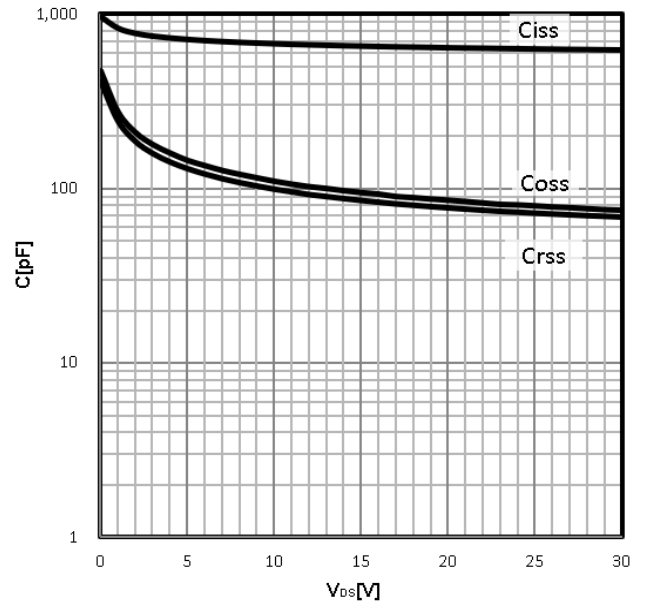
Characteristics Curve:
Typ. output characteristics
 $I_D = f(V_{DS})$

Typ. drain-source on resistance
 $R_{DS(on)} = f(I_D)$

Typ. transfer characteristics
 $I_D = f(V_{GS})$

Drain-source on-state resistance
 $R_{DS(on)} = f(T_j); I_D = -5A; V_{GS} = -10V$


Gate Threshold Voltage

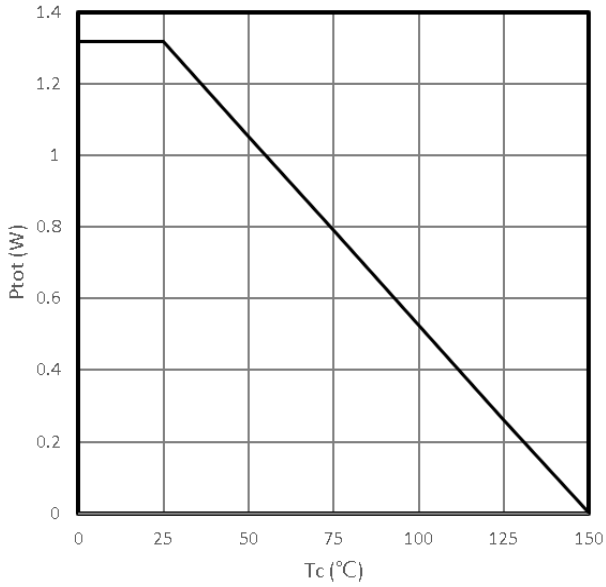
$$-V_{TH} = f(T_j); I_D = -250\mu A$$


Drain-source breakdown voltage

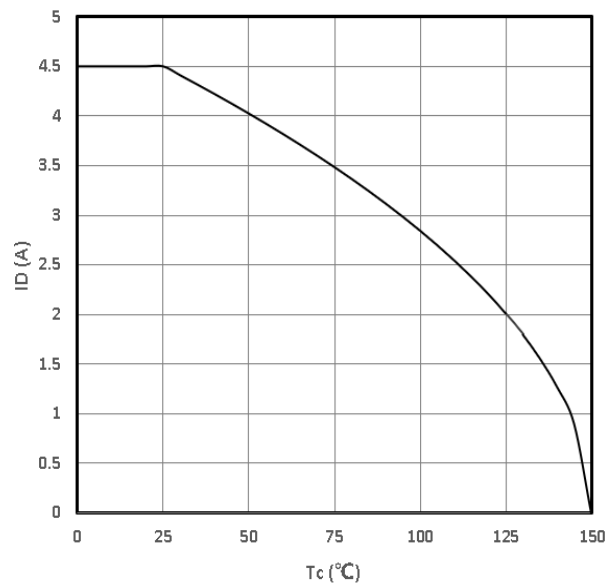
$$V_{BR(DSS)} = f(T_j); I_D = -250\mu A$$


Typ. gate charge
 $V_{GS} = f(Q_{gate}); I_D = -1A$

Typ. capacitances
 $C = f(V_{DS}); V_{GS} = 0V; f = 1MHz$


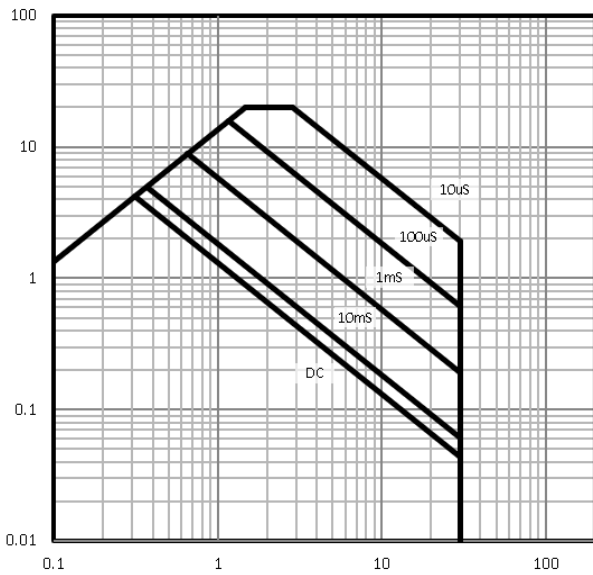
Power Dissipation
 $P_{tot}=f(T_C)$



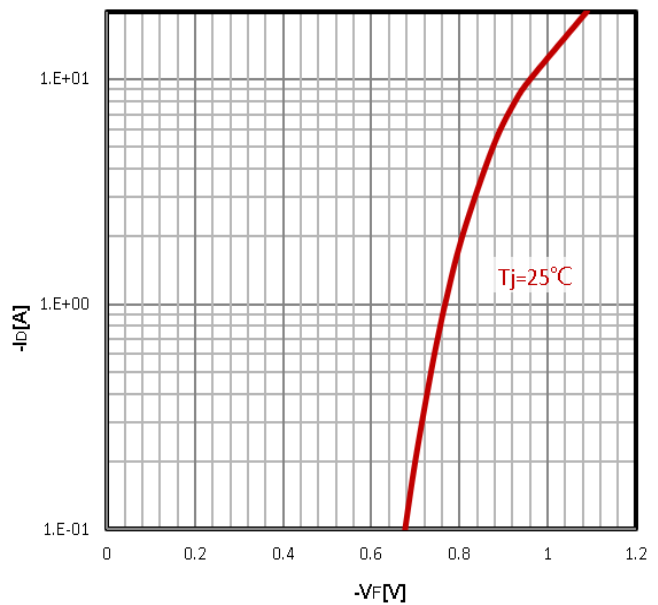
Maximum Drain Current
 $-I_D=f(T_C)$



Safe operating area
 $-I_D=f(-V_{DS})$

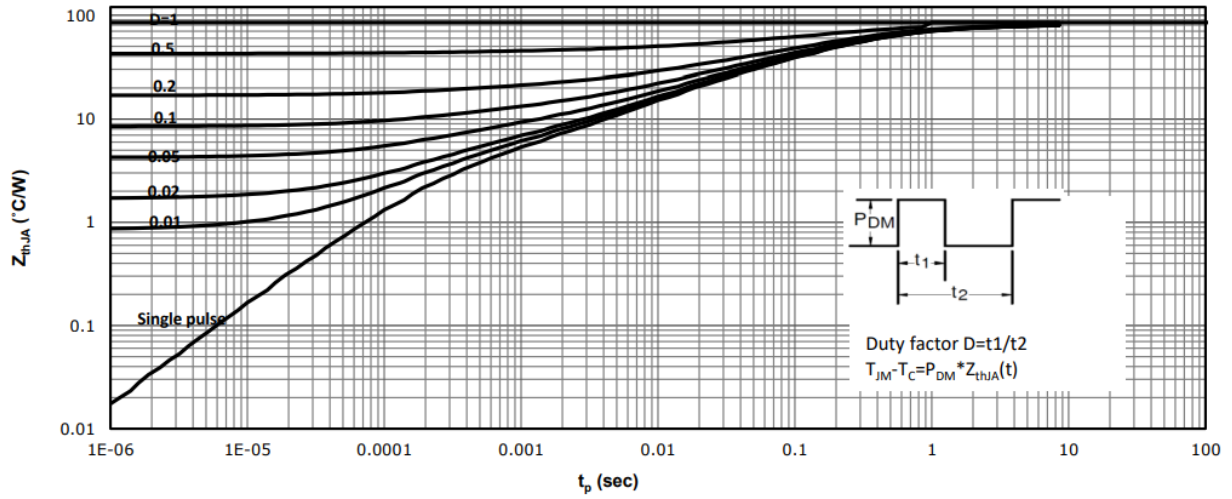


Body Diode Forward Voltage Variation
 $-I_F=f(-V_{DS})$

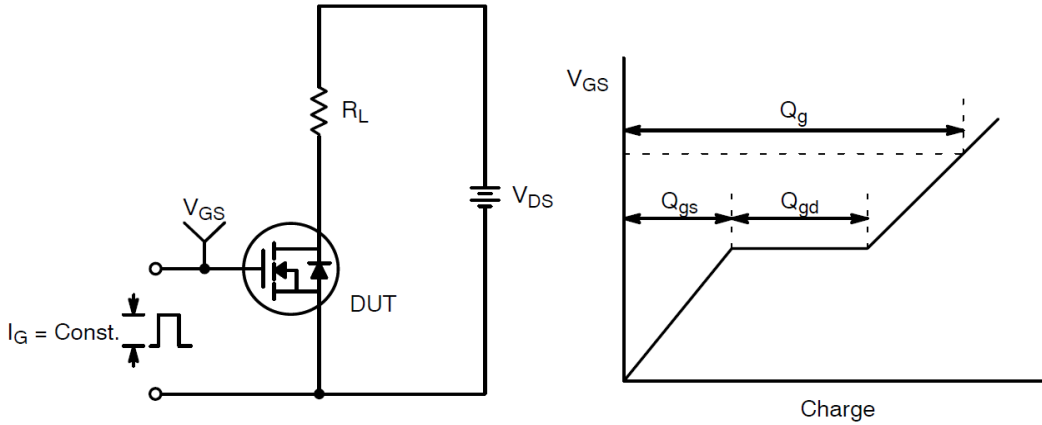


Max. transient thermal impedance

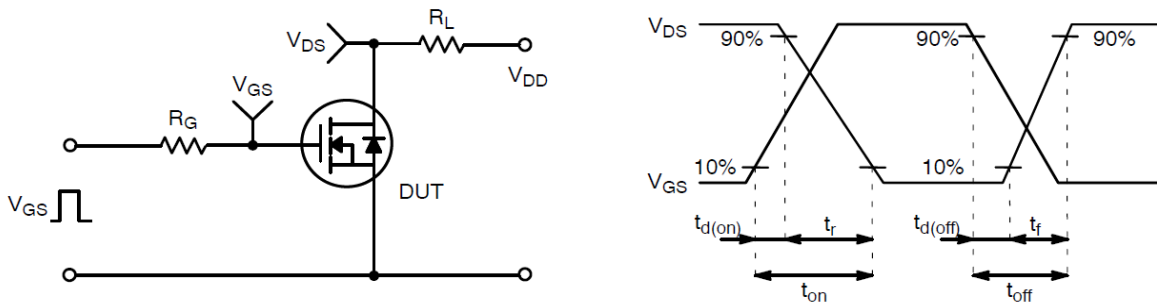
$$Z_{thJC} = f(t_p)$$



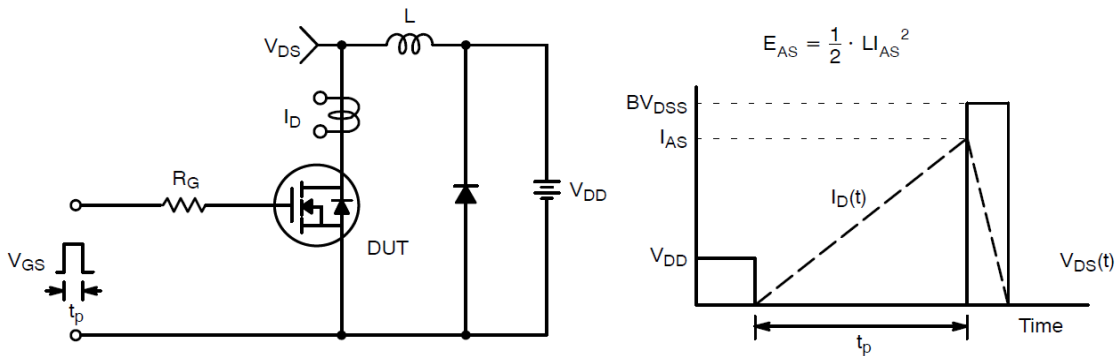
Test Circuit and Waveform:



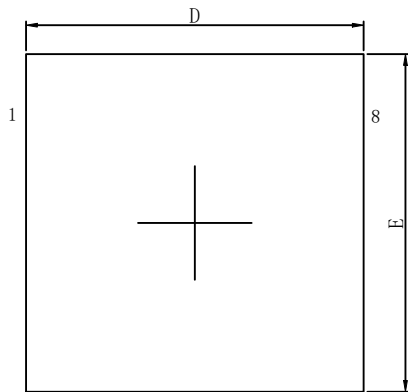
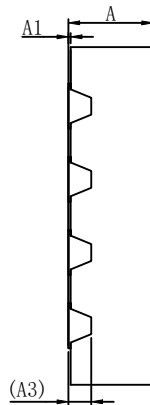
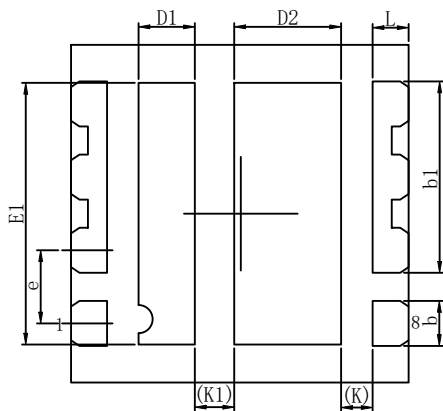
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

•Dimensions (WQFN3.3*3.3)

 TOP VIEW
 [顶视图]

 SIDE VIEW
 [侧视图]

 BOTTOM VIEW
 [背视图]

SYMBOL	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	0.000	0.020	0.050
A3	0.203 REF		
b	0.350	0.400	0.450
b1	1.600	1.700	1.800
D	2.900	3.000	3.100
E	2.900	3.000	3.100
e	0.650 BSC		
D1	0.400	0.500	0.600
D2	0.850	0.950	1.050
E1	2.225	2.325	2.425
L	0.220	0.320	0.420
K	0.280 REF		
K1	0.350 REF		


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