High Performance Current Mode Controllers

The HT3842B, HT3843B series are high performance fixed frequency current mode controllers. They are specifically designed for Off−Line and DC−DC converter applications offering the designer a cost−effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

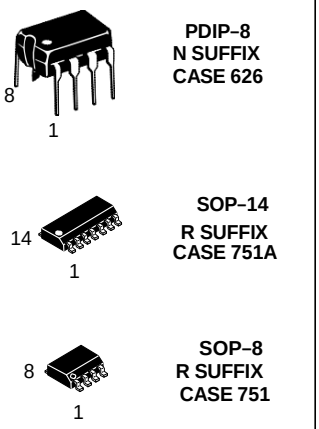
Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle−by−cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

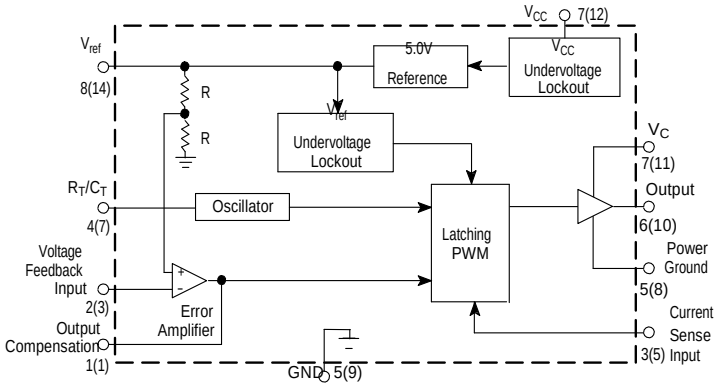
These devices are available in an 8−pin dual−in−line and surface mount (SOIC−8) plastic package as well as the 14−pin plastic surface mount (SOIC−14). The SOIC−14 package has separate power and ground pins for the totem pole output stage.

The HTX842B has UVLO thresholds of 16 V (on) and 10 V (off), ideally suited for off−line converters. The HTX843B is tailored for lower voltage applications having UVLO thresholds of 8.5 V (on) and 7.6 V (off).

Features

- Trimmed Oscillator for Precise Frequency Control
- Oscillator Frequency Guaranteed at 250 kHz
- Current Mode Operation to 500 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle−By−Cycle Current Limiting
- Internally Trimmed Reference with Undervoltage Lockout
- High Current Totem Pole Output
- Undervoltage Lockout with Hysteresis
- Low Startup and Operating Current
- This is a Pb−Free and Halide−Free Device

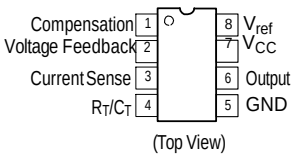




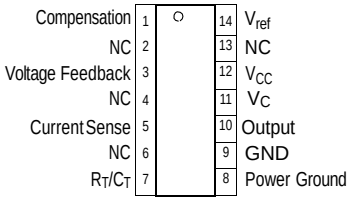
Pin numbers in parenthesis are for the D suffix SOIC−14 package.

Figure 1. Simplified Block Diagram

PIN CONNECTIONS



(Top View)



(Top View)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bias and Driver Voltages (Zero Series Impedance, see also Total Device spec)	V_{CC}, V_C	30	V
Total Power Supply and Zener Current	(I_{CC} + I_Z)	30	mA
Output Current, Source or Sink	I_O	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense, Voltage Feedback, V_{ref} and Rt/Ct Inputs	V_{in}	− 0.3 to + 5.5	V
Compensation	V_{comp}	− 0.3 to + 7.2	V
Output	V_o	− 0.3 to V_{CC} or V_C + 0.3	V
Error Amp Output Sink Current	I_O	10	mA
Power Dissipation and Thermal Characteristics			
D Suffix, Plastic Package, SOIC−14 Case 751A			
Maximum Power Dissipation @ T_A = 25°C	P_D	862	mW
Thermal Resistance, Junction−to−Air	R_{SJA}	145	°C/W
D1 Suffix, Plastic Package, SOIC−8 Case 751			
Maximum Power Dissipation @ T_A = 25°C	P_D	702	mW
Thermal Resistance, Junction−to−Air	R_{SJA}	178	°C/W
N Suffix, Plastic Package, Case 626			
Maximum Power Dissipation @ T_A = 25°C	P_D	1.25	W
Thermal Resistance, Junction−to−Air	R_{SJA}	100	°C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A		°C
HT3842B, HT3843B		0 to 70	
HT2842B, HT2843B		− 25 to + 85	
HT2843D		−40 to +85	
HT3842BV, HT3843BV		−40 to +105	
Storage Temperature Range	T_{stg}	− 65 to+150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 4000 V per JEDEC Standard JESD22-A114B
   Machine Model Method 200 V per JEDEC Standard JESD22-A115-A
2. This device contains latch-up protection and exceeds 100 mA per JEDEC Standard JESD78

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 3], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

Characteristics	Symbol	HT284XA, HT2843D			HT384XA, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Output Voltage (I_O = 1.0 mA, T_J = 25°C)	V_{ref}	4.95	5.0	5.05	4.9	5.0	5.1	V
Line Regulation (V_{CC} = 12 V to 25 V)	Reg_{line}	–	2.0	20	–	2.0	20	mV
Load Regulation (I_O = 1.0 mA to 20 mA)	Reg_{load}	–	3.0	25	–	3.0	25	mV
Temperature Stability	T_S	–	0.2	–	–	0.2	–	mV/°C
Total Output Variation over Line, Load, and Temperature HT284XA HT2843D	V_{ref}	 4.9 4.82	 – –	 5.1 5.18	 4.82	 –	 5.18	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = 25°C)	V_n	–	50	–	–	50	–	μV
Long Term Stability (T_A = 125°C for 1000 Hours)	S	–	5.0	–	–	5.0	–	mV
Output Short Circuit Current	I_{SC}	−30	−85	−180	−30	−85	−180	mA
OSCILLATOR SECTION								
Frequency T_J = 25°C T_A = T_{low} to T_{high} T_J = 25°C (R_T = 6.2 k, C_T = 1.0 nF)	f_{OSC}	 49 48 225	 52 – 250	 55 56 275	 49 48 225	 52 – 250	 55 56 275	kHz
Frequency Change with Voltage (V_{CC} = 12 V to 25 V)	血 f_{OSC}/血	–	0.2	1.0	–	0.2	1.0	%
Frequency Change with Temperature, T_A = T_{low} to T_{high}	血 f_{OSC}/血	–	1.0	–	–	0.5	–	%
Oscillator Voltage Swing (Peak−to−Peak)	V_{OSC}	–	1.6	–	–	1.6	–	V
Discharge Current (V_{OSC} = 2.0 V) T_J = 25°C, T_A = T_{low} to T_{high} HT284XA, HT384XA HT2843D, HT384XAV	I_{dischg}	 7.8 7.5 –	 8.3 – –	 8.8 8.8 –	 7.8 7.6 7.2	 8.3 – –	 8.8 8.8 8.8	mA
ERROR AMPLIFIER SECTION								
Voltage Feedback Input (V_O = 2.5 V) HT284XA HT2843D	V_{FB}	2.45 2.42	2.5 2.5	2.55 2.58	2.42	2.5	2.58	V
Input Bias Current (V_{FB} = 5.0 V)	I_{IB}	–	−0.1	−1.0	–	−0.1	−2.0	μA
Open Loop Voltage Gain (V_O = 2.0 V to 4.0 V)	A_{VOL}	65	90	–	65	90	–	dB
Unity Gain Bandwidth (T_J = 25°C)	BW	0.7	1.0	–	0.7	1.0	–	MHz
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V)	PSRR	60	70	–	60	70	–	dB
Output Current Sink (V_O = 1.1 V, V_{FB} = 2.7 V) Source (V_O = 5.0 V, V_{FB} = 2.3 V)	 I_{Sink} I_{Source}	 2.0 −0.5	 12 −1.0	 – –	 2.0 −0.5	 12 −1.0	 – –	mA
Output Voltage Swing High State (R_L = 15 k to ground, V_{FB} = 2.3 V) Low State (R_L = 15 k to V_{ref}, V_{FB} = 2.7 V) HT284XA, HT384XA HT2843D, HT384XAV	 V_{OH} V_{OL}	 5.0 – –	 6.2 0.8 –	 – 1.1 –	 5.0 – –	 6.2 0.8 0.8	 – 1.1 1.2	V

3. Adjust V_{CC} above the Startup threshold before setting to 15 V.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible. T_{low} = 0°C for HT3842B, HT3843B; −25°C for HT2842B, HT2843B; −40°C for HT3842BV, HT3843BV, HT2843D T_{high} = +70°C for HT3842B, HT3843B; +85°C for HT2842B, HT2843B, HT2843D; +105°C for HT3842BV, HT3843BV

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V [Note 7], R_T = 10 k, C_T = 3.3 nF. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 8], unless otherwise noted.)

Characteristics	Symbol	HT284XA, HT2843D			HT384XA, XBV			Unit
		Min	Typ	Max	Min	Typ	Max	
CURRENT SENSE SECTION								
Current Sense Input Voltage Gain (Notes 5 and 6) HT2843D, HT284XA, HT384XA HT384XAV	A_V	2.85 –	3.0 –	3.15 –	2.85 2.85	3.0 3.0	3.15 3.25	V/V
Maximum Current Sense Input Threshold (Note 5) HT2843D, HT284XA, HT384XA HT384XAV	V_{th}	0.9 –	1.0 –	1.1 –	0.9 0.85	1.0 1.0	1.1 1.1	V
Power Supply Rejection Ratio (V_{CC} = 12 V to 25 V, Note 5)	PSRR	–	70	–	–	70	–	dB
Input Bias Current	I_{IB}	–	−2.0	−10	–	−2.0	−10	μA
Propagation Delay (Current Sense Input to Output)	$t_{PLH(In/Out)}$	–	150	300	–	150	300	ns
OUTPUT SECTION								
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) HT284XA, HT384XA HT384XAV, HT2843D High State (I_{Source} = 20 mA) HT284XA, HT384XA HT384XAV, HT2843D (I_{Source} = 200 mA)	V_{OL} V_{OH}	– – – 13 – 12	0.1 1.6 – 13.5 – 13.4	0.4 2.2 – – – –	– – – 13 12.9 12	0.1 1.6 1.6 13.5 13.5 13.4	0.4 2.2 2.3 – – –	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 1.0 mA)	$V_{OL(UVLO)}$	–	0.1	1.1	–	0.1	1.1	V
Output Voltage Rise Time (C_L = 1.0 nF, T_J = 25°C)	t_r	–	50	150	–	50	150	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = 25°C)	t_f	–	50	150	–	50	150	ns
UNDERVOLTAGE LOCKOUT SECTION								
Startup Threshold (V_{CC}) HTX842B, BV HTX843B, BV, D	V_{th}	15 7.8	16 8.4	17 9.0	14.5 7.8	16 8.4	17.5 9.0	V
Minimum Operating Voltage After Turn−On (V_{CC}) HTX842B, BV HTX843B, BV, D	$V_{CC(min)}$	9.0 7.0	10 7.6	11 8.2	8.5 7.0	10 7.6	11.5 8.2	V
PWM SECTION								
Duty Cycle Maximum HT284XA, HT384XA, HT2843D HT384XAV Minimum	$DC_{(max)}$ $DC_{(min)}$	94 – –	96 – –	– – 0	94 93 –	96 96 –	– – 0	%
TOTAL DEVICE								
Power Supply Current Startup (V_{CC} = 6.5 V for HTX843B, HT2843D V_{CC} 14 V for HTX842B, BV) (Note 7)	I_{CC} + I_C	– –	0.3 12	0.5 17	– –	0.3 12	0.5 17	mA
Power Supply Zener Voltage (I_{CC} = 25 mA)	V_Z	30	36	–	30	36	–	V

5. This parameter is measured at the latch trip point with V_{FB} = 0 V.
6. Comparator gain is defined as: $A_V \frac{\Delta V \text{ Output Compensation}}{\Delta V \text{ Current Sense Input}}$
7. Adjust V_{CC} above the Startup threshold before setting to 15 V.
8. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible. T_{low} = 0°C for HT3842B, HT3843B; −25°C for HT2842B, HT2843B; −40°C for HT3842BV, HT3843BV, HT2843D T_{high} = +70°C for HT3842B, HT3843B; +85°C for HT2842B, HT2843B, HT2843D; +105°C for HT3842BV, HT3843BV

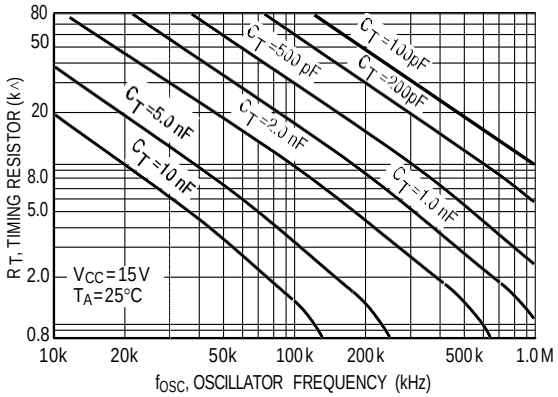


Figure 2. Timing Resistor versus Oscillator Frequency

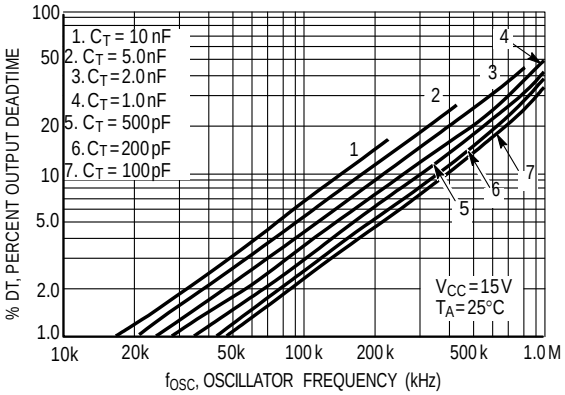


Figure 3. Output Deadtime versus Oscillator Frequency

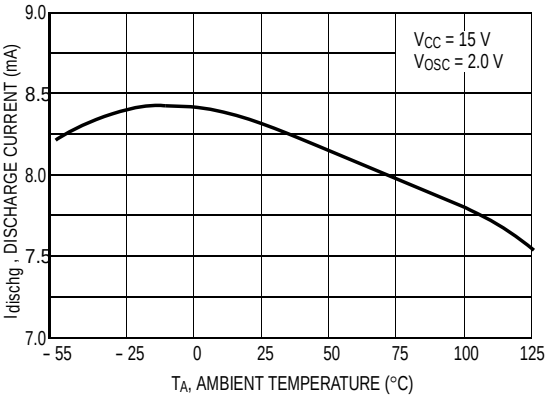


Figure 4. Oscillator Discharge Current versus Temperature

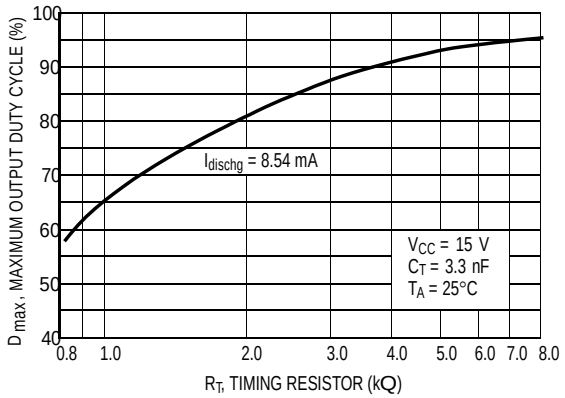


Figure 5. Maximum Output Duty Cycle versus Timing Resistor

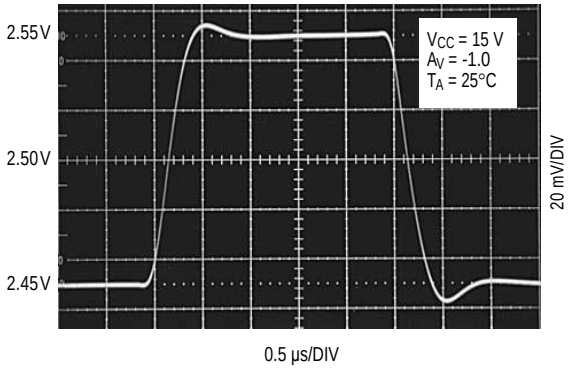


Figure 6. Error Amp Small Signal Transient Response

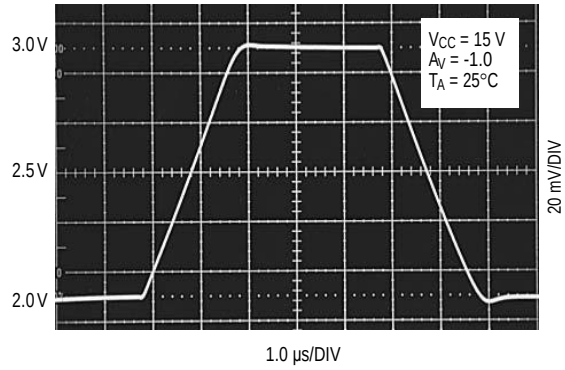


Figure 7. Error Amp Large Signal Transient Response

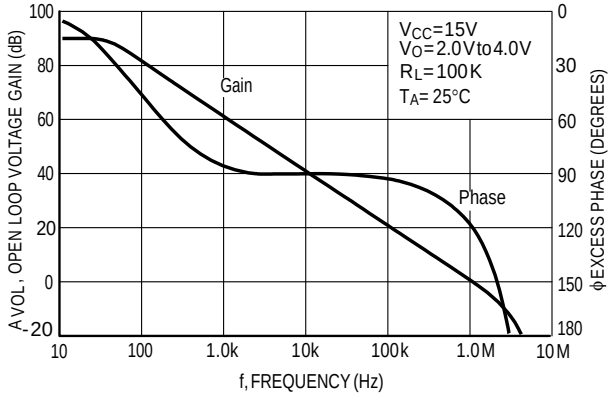


Figure 8. Error Amp Open Loop Gain and Phase versus Frequency

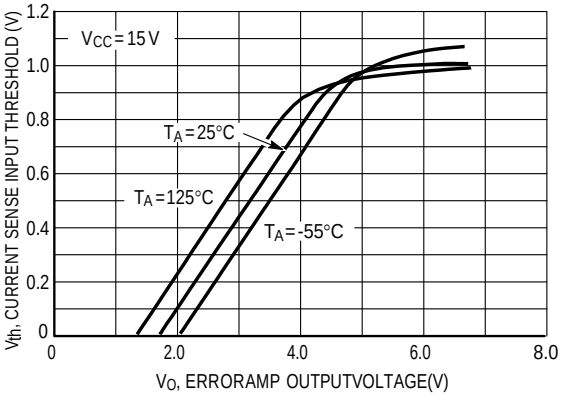


Figure 9. Current Sense Input Threshold versus Error Amp Output Voltage

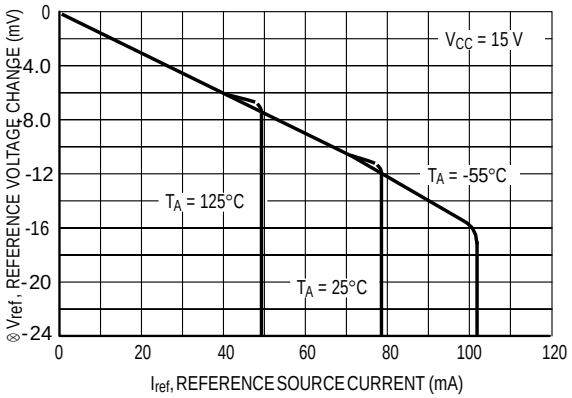


Figure 10. Reference Voltage Change versus Source Current

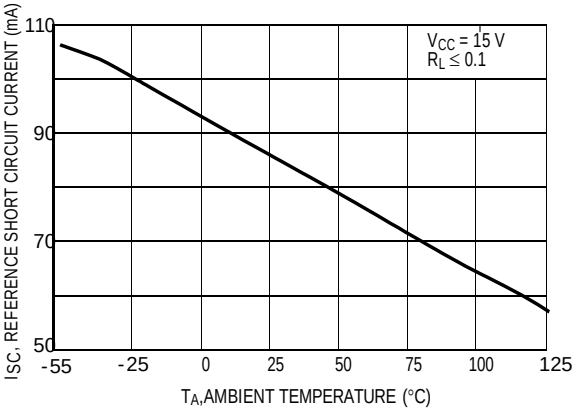


Figure 11. Reference Short Circuit Current versus Temperature

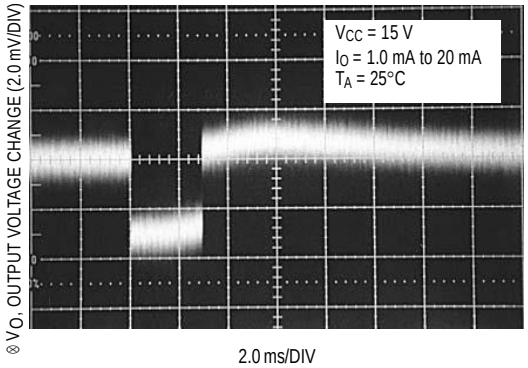


Figure 12. Reference Load Regulation

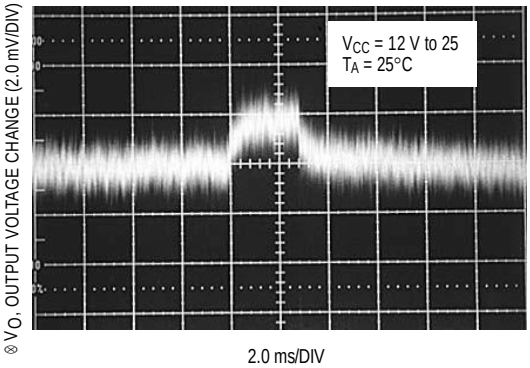


Figure 13. Reference Line Regulation

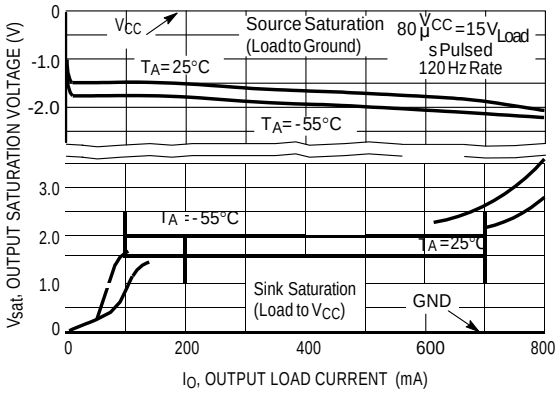


Figure 14. Output Saturation Voltage versus Load Current

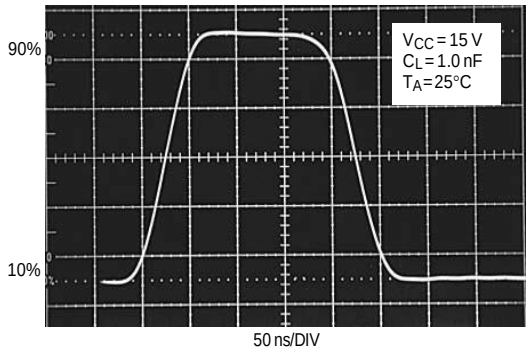


Figure 15. Output Waveform

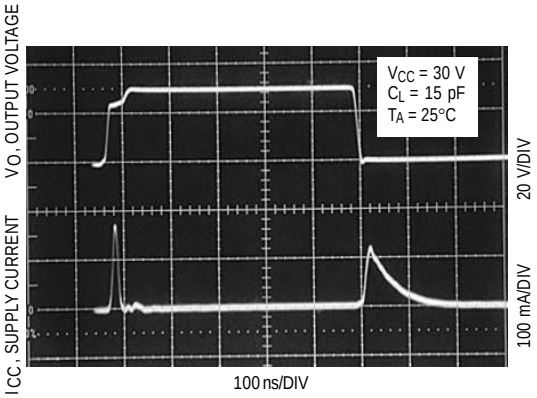


Figure 16. Output Cross Conduction

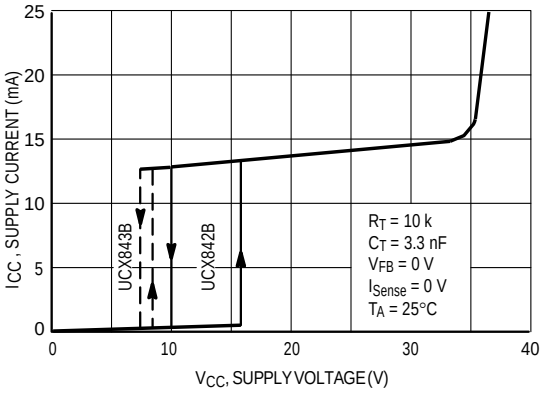


Figure 17. Supply Current versus Supply Voltage

PIN FUNCTION DESCRIPTION

8–Pin	14–Pin	Function	Description
1	1	Compensation	This pin is the Error Amplifier output and is made available for loop compensation.
2	3	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	5	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	7	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500 kHz is possible.
5		GND	This pin is the combined control circuitry and power ground.
6	10	Output	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	12	V_{CC}	This pin is the positive supply of the control IC.
8	14	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.
	8	Power Ground	This pin is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
	11	V_C	The Output high state (V_{OH}) is set by the voltage applied to this pin. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
	9	GND	This pin is the control circuitry ground return and is connected back to the power source ground.
	2,4,6,13	NC	No connection. These pins are not internally connected.

OPERATING DESCRIPTION

The HT3842B, HT3843B series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off−Line and DC−to−DC converter applications offering the designer a cost−effective solution with minimal external components. A representative block diagram is shown in Figure 19.

Oscillator

The oscillator frequency is programmed by the values chosen for the timing components R_T and C_T. It must also be noted that the value of R_T uniquely determines the maximum duty ratio of HT384xx. The oscillator configuration depicting the connection of the timing components to the R_T/C_T pin of the controller is shown in Figure 18. Capacitor C_T gets charged from the V_{ref} source, through resistor R_T to its peak threshold $V_{RT/CT(peak)}$, typically 2.8 V. Upon reaching this peak threshold volage, an internal 8.3 mA current source, I_{dischg}, is enabled and the voltage across C_T begins to decrease. Once the voltage across C_T reaches its valley threshold, $V_{RT/CT(valley)}$, typically 1.2 V, I_{dischg} turns off. This allows capacitor C_T to charge up again from V_{ref}. This entire cycle repeats, and the resulting waveform on the R_T/C_T pin has a sawtooth shape. Typical waveforms are shown in Figure 20.

The oscillator thresholds are temperature compensated to within ±6% at 50 kHz. Considering the general industry trend of operating switching controllers at higher frequencies, the HT384xx is guaranteed to operate within ±10% at 250 kHz. These internal circuit refinements minimize variations of oscillator frequency and maximum duty ratio.

The charging and discharging times of the timing capacitor C_T are calculated using Equations 1 and 2. These equations do not take into account the propagation delays of the internal comparator. Hence, at higher frequencies, the calculated value of the oscillator frequency differs from the actual value.

$$t_{RT/CT(chg)} = R_T C_T \ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}}\right) \quad \text{(eq. 1)}$$

$$t_{RT/CT(dischg)} = R_T C_T \ln\left(\frac{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(valley)} - V_{ref}}\right) \quad \text{(eq. 2)}$$

The maximum duty ratio, D_{max} is given by Equation 3.

$$D_{max} = \frac{t_{RT/CT(chg)}}{t_{RT/CT(chg)} + t_{RT/CT(dischg)}} \quad \text{(eq. 3)}$$

Substituting Equations 1 and 2 into Equation 3, and after algebraic simplification, weobtain

$$D_{max} = \frac{\ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}\right)}{\ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}}\right) \quad \ln\left(\frac{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(valley)} - V_{ref}}\right)} \quad \text{(eq. 4)}$$

Clearly, the maximum duty ratio is determined by the timing resistor R_T. Therefore, R_T is chosen such as to achieve a desired maximum duty ratio. Once R_T has been selected, C_T can now be chosen to obtain the desired switching frequency as per Equation 5.

$$f = \frac{1}{R_T C_T \ln\left(\frac{V_{RT/CT(valley)} - V_{ref}}{V_{RT/CT(peak)} - V_{ref}}\right) \quad \ln\left(\frac{R_T I_{dischg} + V_{RT/CT(peak)} - V_{ref}}{R_T I_{dischg} + V_{RT/CT(valley)} - V_{ref}}\right)} \quad \text{(eq. 5)}$$

Figure 2 shows the frequency and maximum duty ratio variation versus R_T for given values of C_T. Care should be taken to ensure that the absolute minimum value of R_T should not be less than 542 Q. However, considering a 10% tolerance for the timing resistor, the nearest available standard resistor of 680 Q is the absolute minimum that can be used to guarantee normal oscillator operation. If a timing resistor smaller than this value is used, then the charging current through the R_T, C_T path will exceed the pulldown (discharge) current and the oscillator will get permanently locked/latched to an undefined state.

In many noise-sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Figure 22. For reliable synchronization, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi-unit synchronization is shown in Figure 23. By tailoring the clock waveform, accurate Output duty ratio clamping can be achieved.

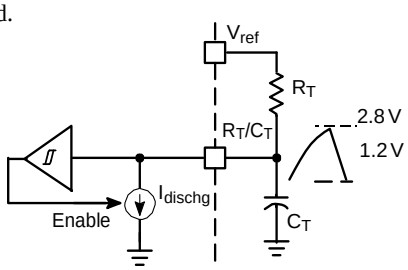


Figure 18. Oscillator Configuration

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical DC voltage gain of 90 dB, and a unity gain bandwidth of 1.0 MHz with 57 degrees of phase margin (Figure 8). The non−inverting input is internally biased at 2.5 V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is −2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output (Pin 1) is provided for external loop compensation (Figure 33). The output voltage is offset by two diode drops (≈1.4 V) and divided by three before it connects to the non−inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when pin 1 is at its lowest state (V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft−start interval (Figures 25, 26). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5 mA) and the required output voltage (V_{OH}) to reach the comparator's 1.0 V clamplevel:

$$R_{f(min)} \approx \frac{3.0\ (1.0\ V) + 1.4\ V}{0.5\ mA} = 8800\ \Omega$$

Current Sense Comparator and PWM Latch

The HT3842B, HT3843B operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation (Pin 1). Thus the error signal controls the peak inductor current on a cycle−by−cycle basis. The Current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground−referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared to a level derived from the Error Amp Output. The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{V_{(Pin\ 1)} - 1.4\ V}{3\ R_S}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0 V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{1.0\ V}{R_S}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Figure 24. The two external diodes are used to compensate the internal diodes, yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup canresult if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability (refer to Figure 28).

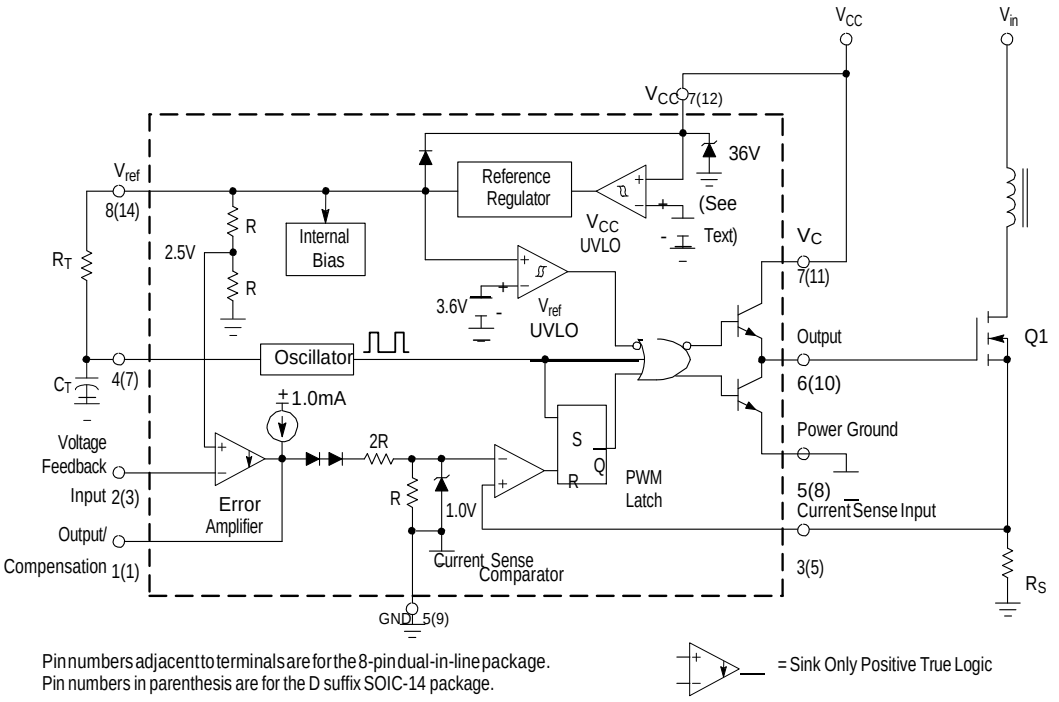


Figure 19. Representative Block Diagram

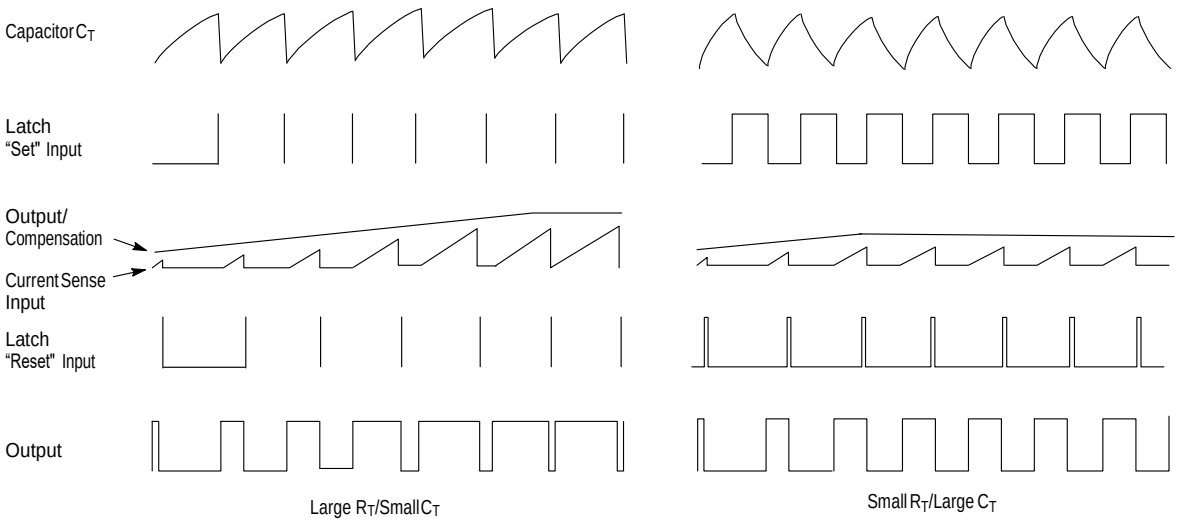


Figure 20. Timing Diagram

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built−in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16 V/10 V for the HTX842B, and 8.4 V/7.6 V for the HTX843B. The V_{ref} comparator upper and lower thresholds are 3.6 V/3.4 V. The large hysteresis and low startup current of the HTX842B makes it ideally suited in off−line converter applications where efficient bootstrap startup techniques are required (Figure 35). The HTX843B is intended for lower voltage DC−to−DC converter applications. A 36 V Zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage (V_{CC}) for the HTX842B is 11 V and 8.2 V for the HTX843B.

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It is capable of up to ±1.0 A peak drive current and has a typical rise and fall time of 50 ns with a 1.0 nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an undervoltage lockout is active. This characteristic eliminates the need for an external pull−down resistor.

The SOIC−14 surface mount package provides separate pins for V_C (output supply) and Power Ground. Proper implementation will significantly reduce the level of switching transient noise imposed on the control circuitry. This becomes particularly useful when reducing the $I_{pk(max)}$ clamp level. The separate V_C supply input allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}. A Zener clamp is typically connected to this input when driving power MOSFETs in systems where V_{CC} is greater than 20 V. Figure 27 shows proper power and control ground connections in a current−sensing power MOSFET application.

Reference

The 5.0 V bandgap reference is trimmed to ±1.0% tolerance at T_J = 25°C on the HT284XA, and ±2.0% on the HT384XA. Its primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short−circuit protection and is capable of providing in excess of 20 mA for powering additional control systemcircuitry.

Design Considerations

Do not attempt to construct the converter on wire−wrap or plug−in prototype boards. High frequency circuit layout techniques are imperative to prevent pulse−width jitter. This is usually caused by excessive noise pick−up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low−current signal and high−current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise−generatingcomponents.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulator's closed loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Figure 21A shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2, until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting in a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn−on (t_2) is increased by $\Delta I + \Delta I\, m_2/m_1$. The minimum current at the next cycle (t_3) decreases to ($\Delta I + \Delta I\, m_2/m_1$) ($m_2/m_1$). This perturbation is multiplied by m_2/m_1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn−on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Figure 21B shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensating ramp (m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage, yielding true current mode operation. The compensating ramp can be derived from the oscillator and added to either the Voltage Feedback or Current Sense inputs (Figure 34).

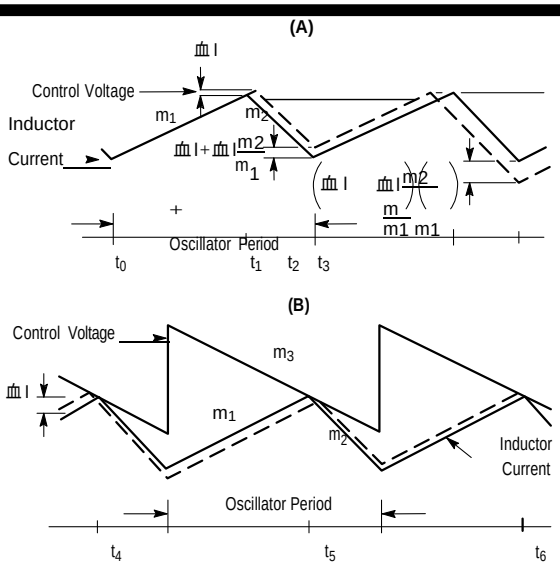


Figure 21. Continuous Current Waveforms

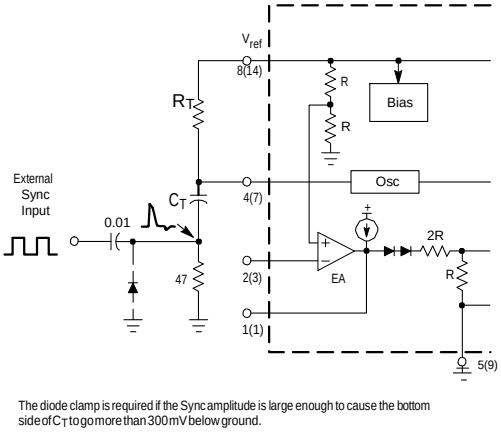


Figure 22. External Clock Synchronization

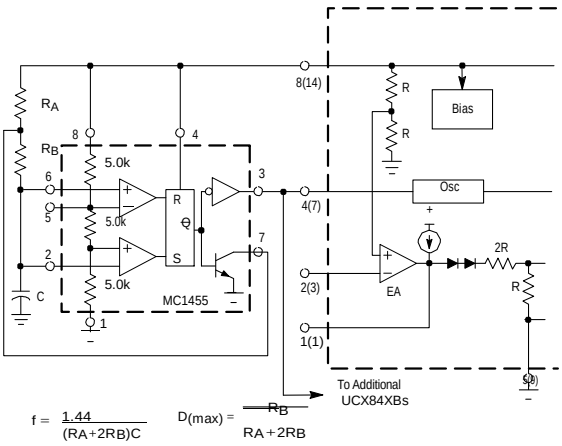


Figure 23. External Duty Cycle Clamp and Multi–Unit Synchronization

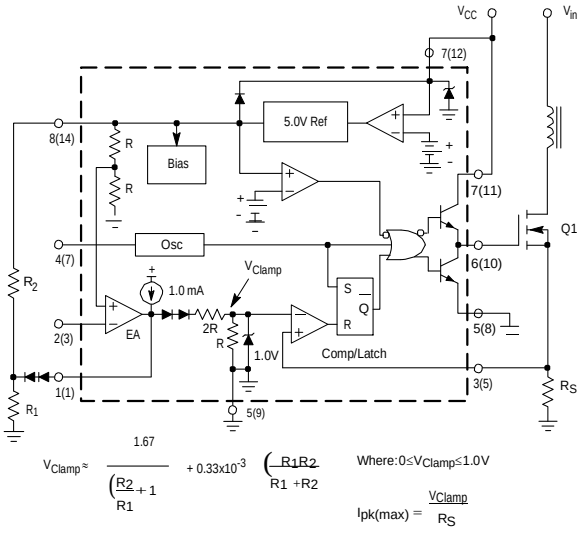


Figure 24. Adjustable Reduction of Clamp Level

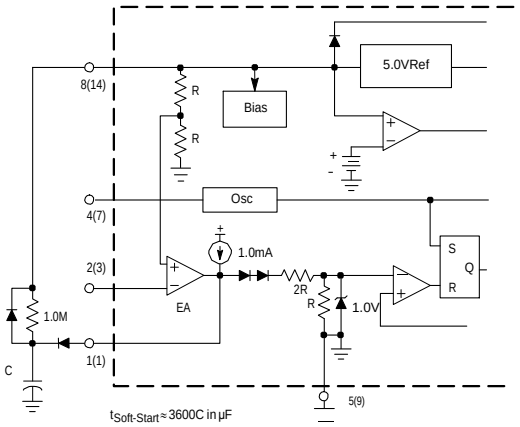


Figure 25. Soft−Start Circuit

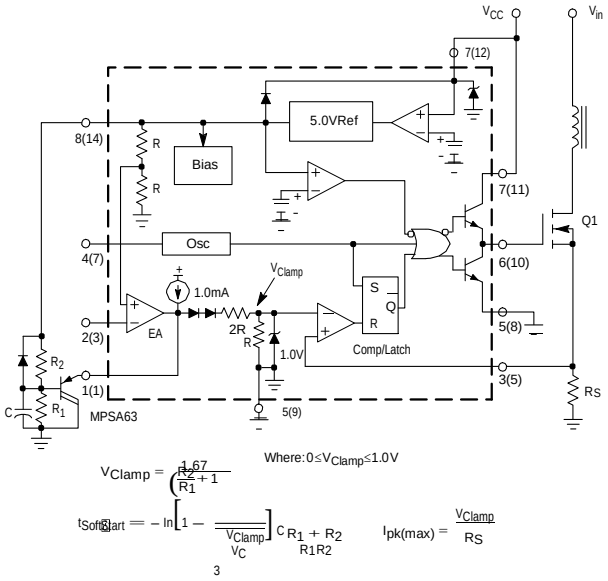
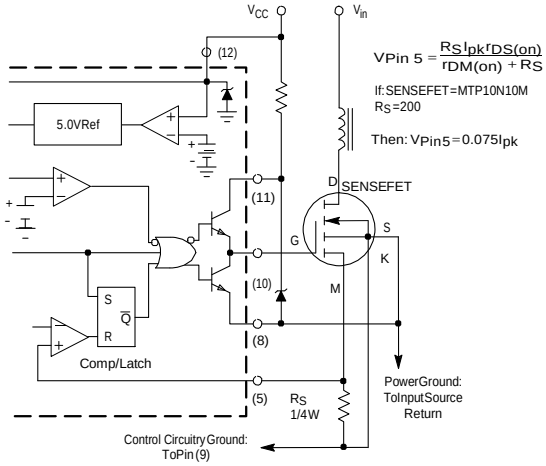
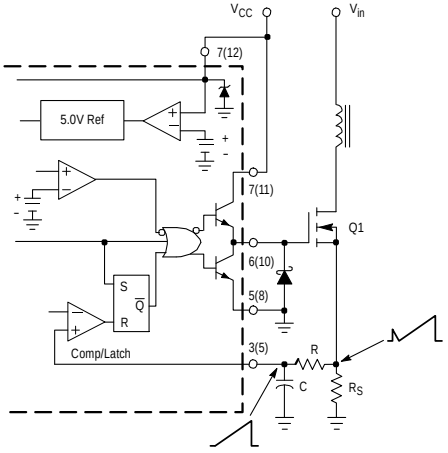


Figure 26. Adjustable Buffered Reductionof Clamp Level with Soft−Start



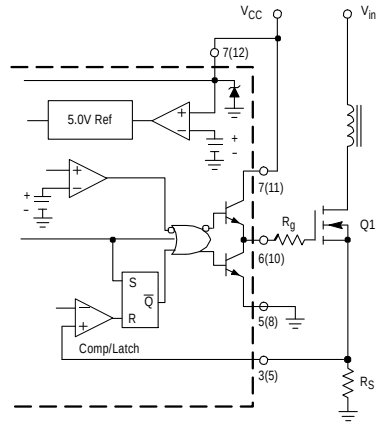
Virtually lossless current sensing can be achieved with the implementation of a SENSEFET power switch. For proper operation during over-current conditions, a reduction of the $I_{pk(max)}$ clamp level must be implemented. Refer to Figures 24 and 26.

Figure 27. Current Sensing Power MOSFET



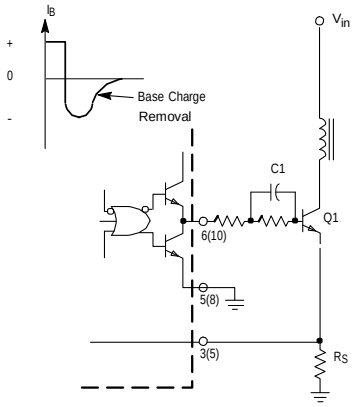
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Figure 28. Current Waveform Spike Suppression



Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Figure 29. MOSFET Parasitic Oscillations



The totem pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C_1.

Figure 30. Bipolar Transistor Drive

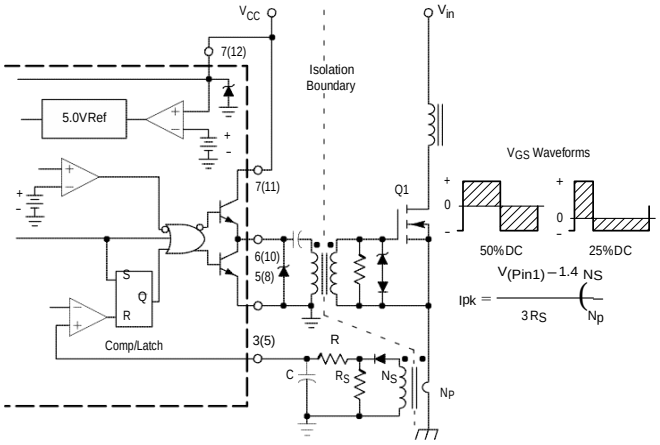
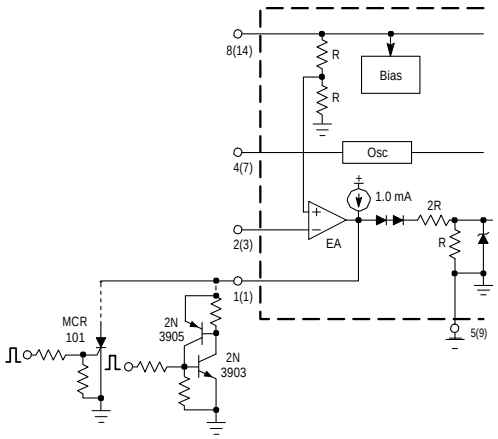
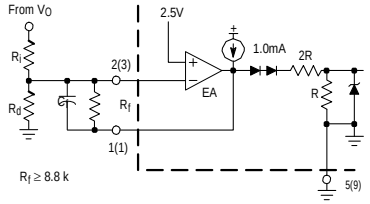


Figure 31. Isolated MOSFET Drive

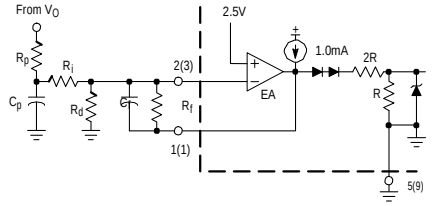


The MCR101 SCR must be selected for a holding of < 0.5 mA @ $T_{A(min)}$. The simple two transistor circuit can be used in place of the SCR as shown. All resistors are 10 k.

Figure 32. Latched Shutdown

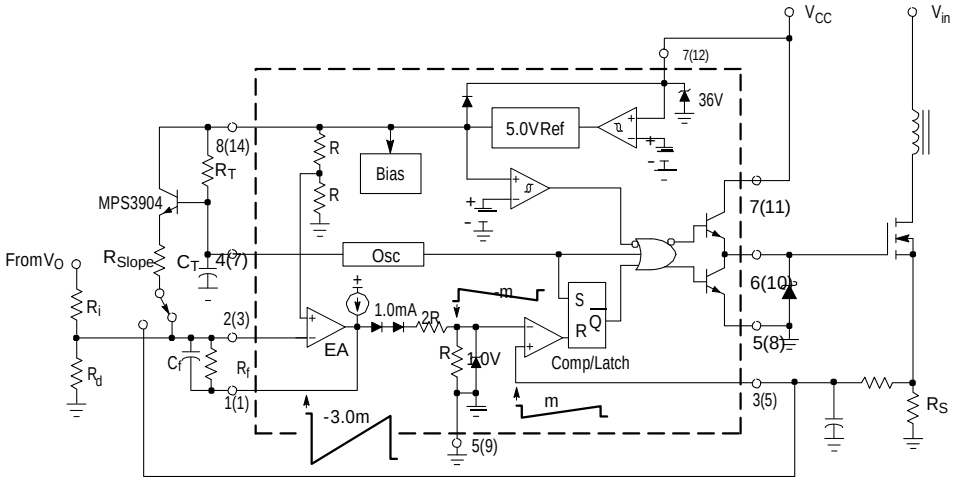


Error Amp compensation circuit for stabilizing any current mode topology except for boost and flyback converters operating with continuous inductor current.



Error Amp compensation circuit for stabilizing current mode boost and flyback topologies operating with continuous inductor current.

Figure 33. Error Amplifier Compensation



The buffered oscillator ramp can be resistively summed with either the voltage feedback or current sense inputs to provide slope compensation.

Figure 34. Slope Compensation

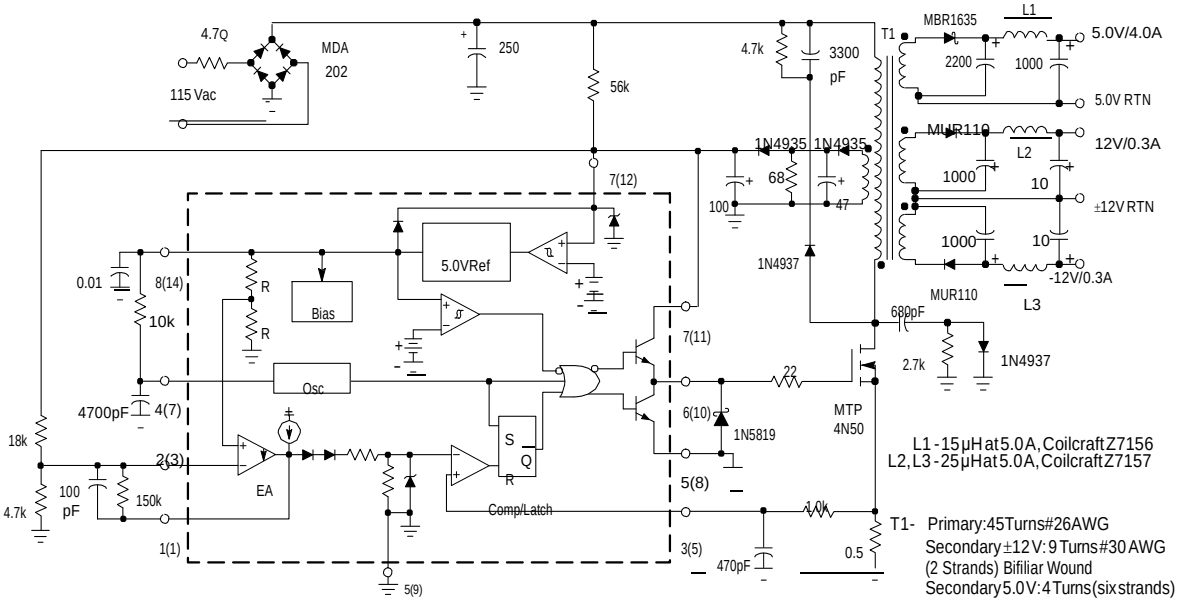


Figure 35. 27 W Off−Line Flyback Regulator

Test	Conditions	Results
Line Regulation: 5.0 V ±12V	V_{in} = 95 to 130 Vac	凾 = 50 mV or ± 0.5% 凾 = 24 mV or ± 0.1%
Load Regulation: 5.0 V ±12V	V_{in} = 115 Vac, I_{out} = 1.0 A to 4.0 A V_{in} = 115 Vac, I_{out} = 100 mA to 300 mA	凾 = 300 mV or ± 3.0% 凾 = 60 mV or ± 0.25%
Output Ripple: 5.0 V ±12V	V_{in} = 115 Vac	40 mV_{pp} 80 mV_{pp}
Efficiency	V_{in} = 115 Vac	70%

All outputs are at nominal load currents, unless otherwise noted