**MOSFET Silicon N-Channel MOS**

## 1. Applications

Synchronous rectification in SMPS,
Hard switching and High speed circuit
DC/DC in telecoms and industrial

## 2. Features

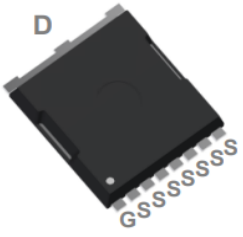
Low drain-source on-resistance:
TO220&TO263 RDS(on) = 2.8mΩ (typ.)
TOLL-8L RDS(on) = 2.4mΩ (typ.)
High speed power switching
Enhanced body diode dv/dt capability
Enhanced avalanche ruggedness

**Table 1 Key Performance Parameters**

| Parameter | Value | Unit |
|---|---|---|
| $V_{DS}$ @ $T_{j,max}$ | 100 | V |
| $R_{DS(on),max}$ TO220&TO263 | 3.4 | mΩ |
| $R_{DS(on),max}$ TOLL | 3.0 | mΩ |
| $Q_{g,typ}$ | 138 | nC |
| $I_{D,pulse}$ | 856 | A |

## 3. Packaging and Internal Circuit

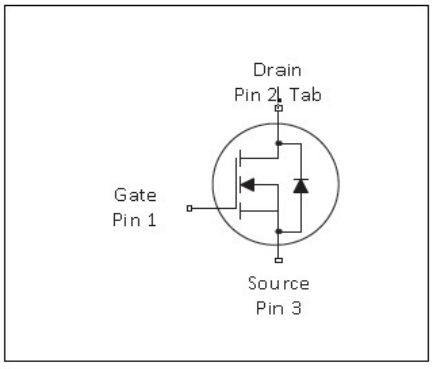
| Part Name | Package | Marking |
|---|---|---|
| AUP034N10 | TO220 | AUP034N10 |
| AUB034N10 | TO263 | AUB034N10 |
| AUR030N10 | TOLL | AUR030N10 |

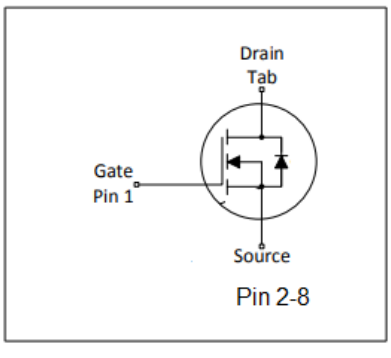
| TO263 | TO220 | TOLL |
|---|---|---|
|  |  |  |









# 1 Maximum ratings

At $T_j$= 25°C, unless otherwise specified

## Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current at sikicon[1)] | $I_D$ | | - | 214 | A | $T_C$=25°C |
| Continuous drain current at package[1)] | $I_D$ | | - | 195 | A | $T_C$=25°C |
| Continuous drain current at silicon[1)] | $I_D$ | | | 151 | A | $T_C$=100°C |
| Pulsed drain current[2)] | $I_{D,pulse}$ | - | | 856 | A | $T_C$=25°C |
| Avalanche energy, single pulse | $E_{AS}$ | - | - | 512 | mJ | Tc=25°C,VDD=40V,Vgs=10V, L=1mH, RG=25Ω |
| Avalanche current, single pulse | $I_{AR}$ | - | - | 32 | A | Tc=25°C, VDD=40V, L=1mH, RG=25Ω |
| Gate source voltage (static) | $V_{GS}$ | -20 | - | 20 | V | static; |
| Power dissipation | $P_{tot}$ | - | - | 330 | W | $T_C$=25°C |
| Storage temperature | $T_{stg}$ | -55 | - | 175 | °C | |
| Operating junction temperature | $T_j$ | -55 | - | 175 | °C | |
| Soldering Temperature<br>Distance of 1.6mm from case for 10s | $T_L$ | | | 300 | °C | |

[1)] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2)] Pulse width $t_p$ limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical $R_G$

## 2 Thermal characteristics

**Table Thermal characteristics(TO263&TO252)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 0.46 | °C/W | - |
| Thermal resistance, junction - ambient | $R_{thJA}$ | - | - | 63 | °C/W | device on PCB, minimal footprint |

**Table Thermal characteristics(TOLL)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case | $R_{thJC}$ | - | - | 0.28 | °C/W | - |
| Thermal resistance, junction - ambient | $R_{thJA}$ | - | - | 48 | °C/W | device on PCB, minimal footprint |

# 3 Electrical characteristics

at$T_j$=25°C, unless otherwise specified

## Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 100 | - | - | V | $V_{GS}$=0V, $I_D$=250uA |
| Gate threshold voltage | $V_{(GS)th}$ | 2 | | 4 | V | $V_{DS}$=$V_{GS}$, $I_D$=250uA |
| Zero gate voltage drain current | $I_{DSS}$ | - | - | 1 | uA | $V_{DS}$=100V, $V_{GS}$=0V, $T_j$=25°C |
| Gate-source leakage current | $I_{GSS}$ | - | - | +/-100 | nA | $V_{GS}$=+/-20V, $V_{DS}$=0V |
| Drain-source on-state resistance (TO220&TO263) | $R_{DS(on)}$ | - | 2.8 | 3.4 | mΩ | $V_{GS}$=10V, $I_D$=20A, $T_j$=25°C |
| Drain-source on-state resistance (TOLL) | $R_{DS(on)}$ | - | 2.4 | 3.0 | mΩ | $V_{GS}$=10V, $I_D$=20A, $T_j$=25°C |
| Gate resistance (Intrinsic) | $R_G$ | - | 2.6 | - | Ω | $f$=1MHz, open drain |
| Transconductance | *Gfs* | | 197.2 | | S | $V_{DS}$=*5V*, $I_D$=90A |

## Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Input capacitance | $C_{iss}$ | - | 10000 | - | pF | $V_{GS}$=0V, $V_{DS}$=25V, $f$=1MHz |
| Output capacitance | $C_{oss}$ | - | 2900 | - | pF | $V_{GS}$=0V, $V_{DS}$=25V, $f$=1MHz |
| Reverse transfer capacitance | $C_{rss}$ | - | 280 | - | pF | $V_{GS}$=0V, $V_{DS}$=25V, $f$=1MHz |
| Turn-on delay time | $t_{d(on)}$ | - | 38 | - | ns | $V_{DD}$=50V,$V_{GS}$=10V,$I_D$=80A, $R_G$=2.5Ω |
| Rise time | $t_r$ | - | 50 | - | ns | $V_{DD}$=50V,$V_{GS}$=10V,$I_D$=80A, $R_G$=2.5Ω |
| Turn-off delay time | $t_{d(off)}$ | - | 69 | - | ns | $V_{DD}$=50V,$V_{GS}$=10V,$I_D$=80A, $R_G$=2.5Ω |
| Fall time | $t_f$ | - | 33 | - | ns | $V_{DD}$=50V,$V_{GS}$=10V,$I_D$=80A, $R_G$=2.5Ω |

## Table 6 Gate charge characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | $Q_{gs}$ | - | 58 | - | nC | $V_{DD}$=50V, $I_D$=80A, $V_{GS}$=10V |
| Gate to drain charge | $Q_{gd}$ | - | 44 | - | nC | $V_{DD}$=50V, $I_D$=80A, $V_{GS}$=10V |
| Gate charge total | $Q_g$ | - | 138 | - | nC | $V_{DD}$=50V, $I_D$=80A, $V_{GS}$=10V |

## Table 7 Reverse diode characteristics

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Continuous Source Current at silicon | $I_{SD}$ | - | - | 214 | A | *Maximum Ratings* |
| Diode forward voltage | $V_{SD}$ | - | - | 1.2 | V | $V_{GS}$=0V, $I_S$=80A, $T_j$=25°C |
| Reverse recovery time | $t_{rr}$ | - | 95 | - | ns | *Vgs=0V*, $I_F$=80A, d$i_F$/d$t$=100A/µs |
| Reverse recovery charge | $Q_{rr}$ | - | 143 | - | nC | *Vgs=0V*, $I_F$=80A, d$i_F$/d$t$=100A/µs |

## 4 Electrical characteristics diagram

**Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case**

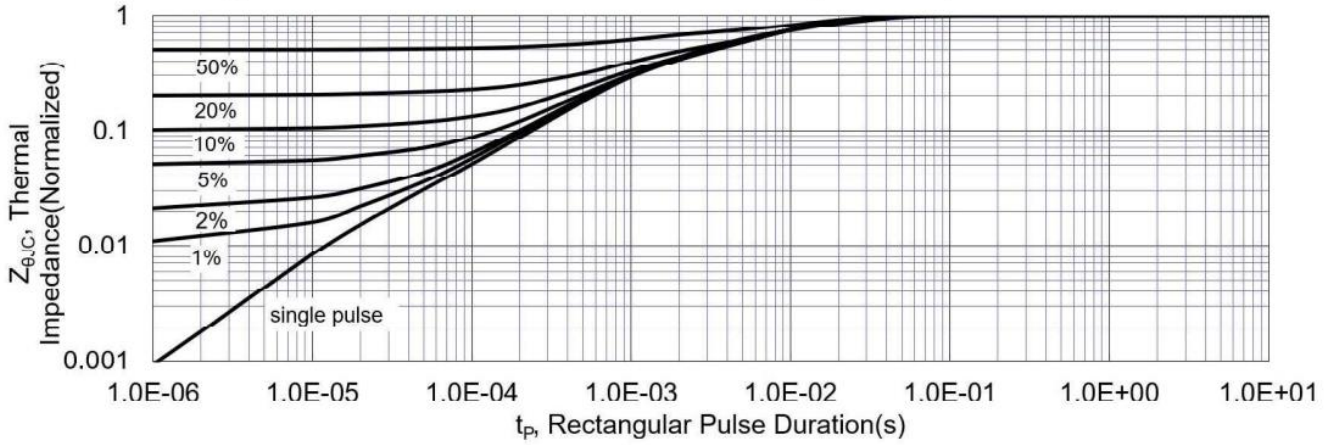



**Figure 2. Maximum Power Dissipation vs. Case Temperature**

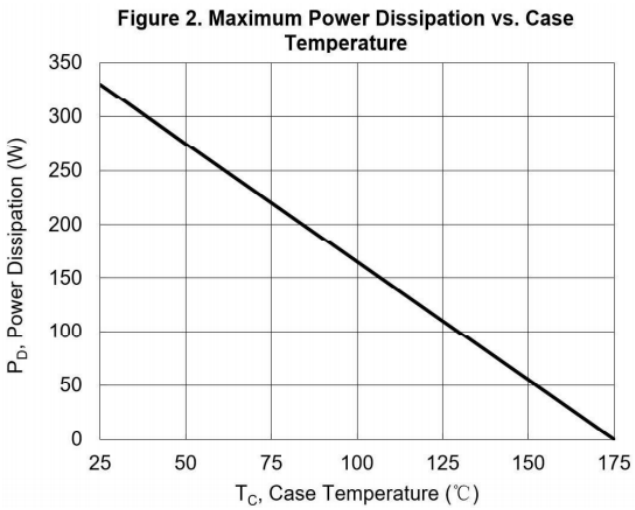



**Figure 3. Maximum Continuous Drain Current vs Case Temperature**

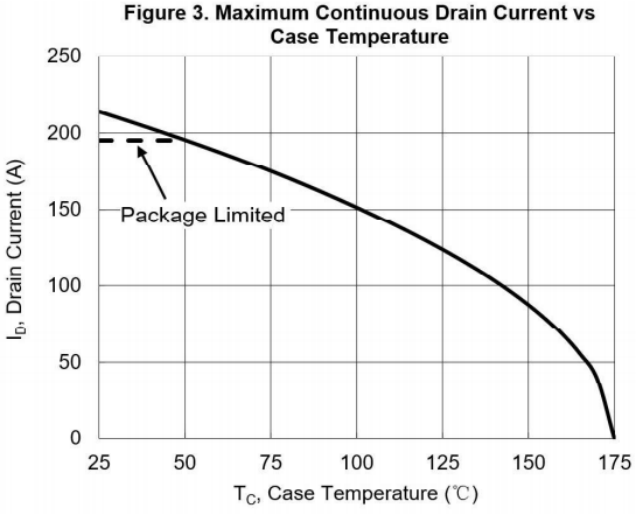



**Figure 4. Typical Output Characteristics**

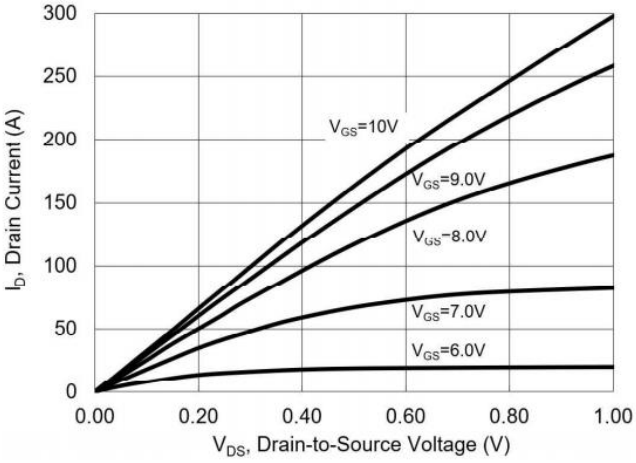



**Figure 5. Unclamped Inductive Switching Capability**

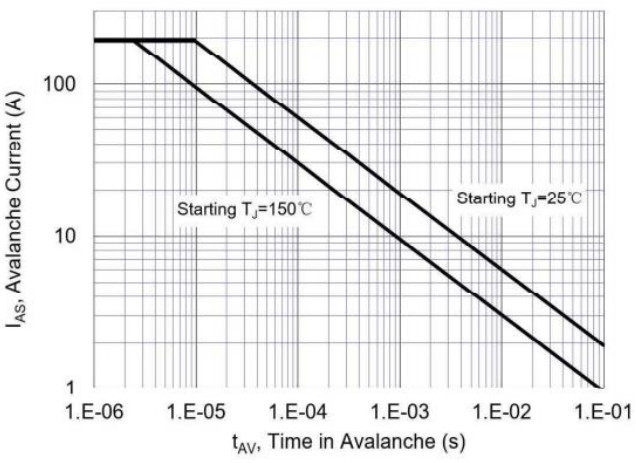


**Figure 6. Maximum Peak Current Capability**

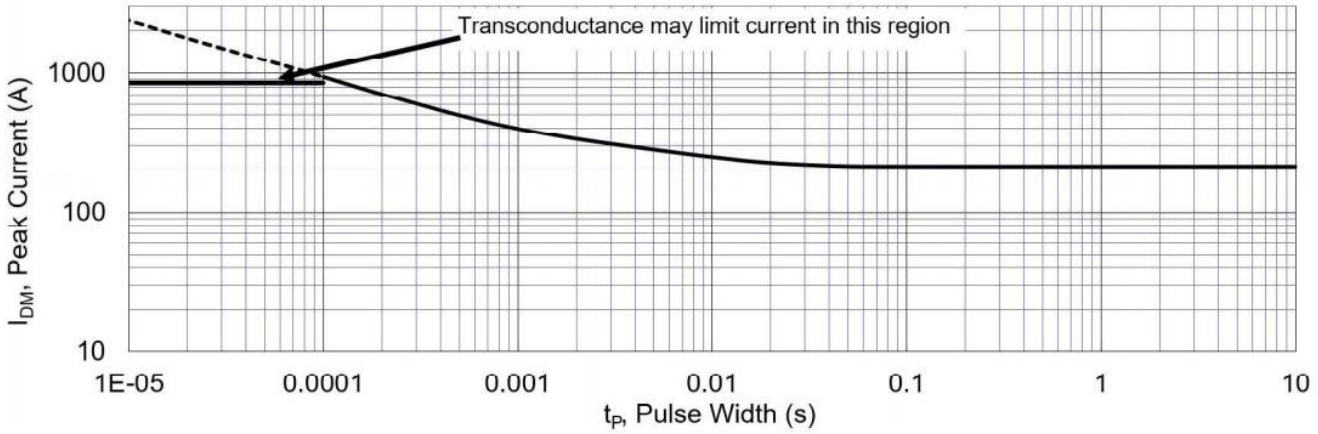



**Figure 7. Maximum Forward Safe Operation Area**

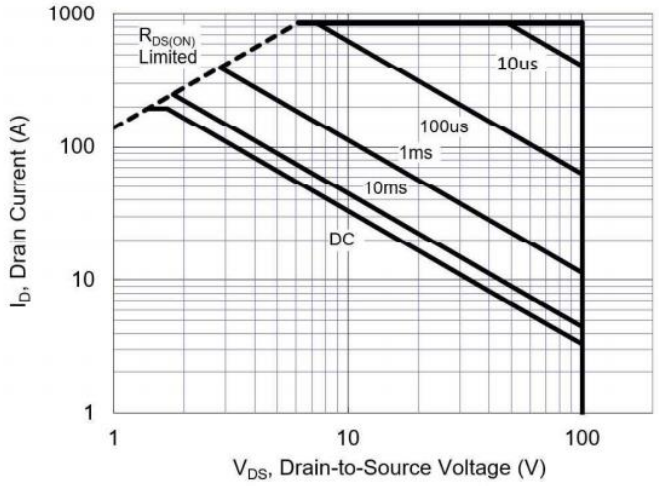



**Figure 8. Typical Capacitance vs. Drain-to-Source Voltage**

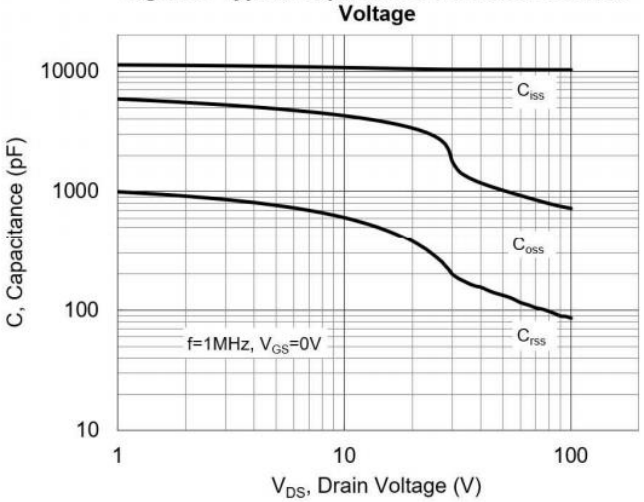
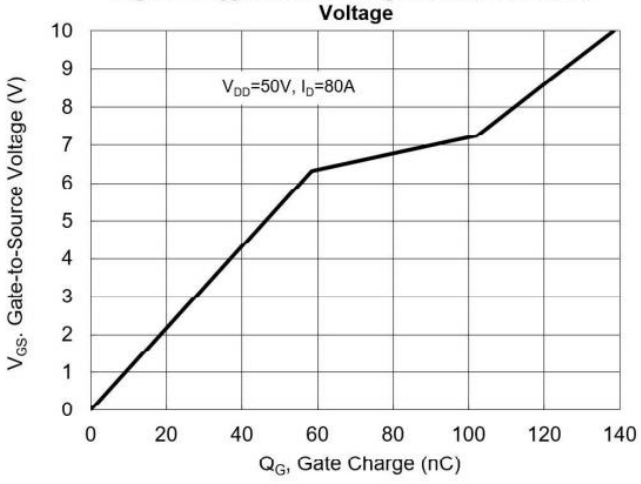
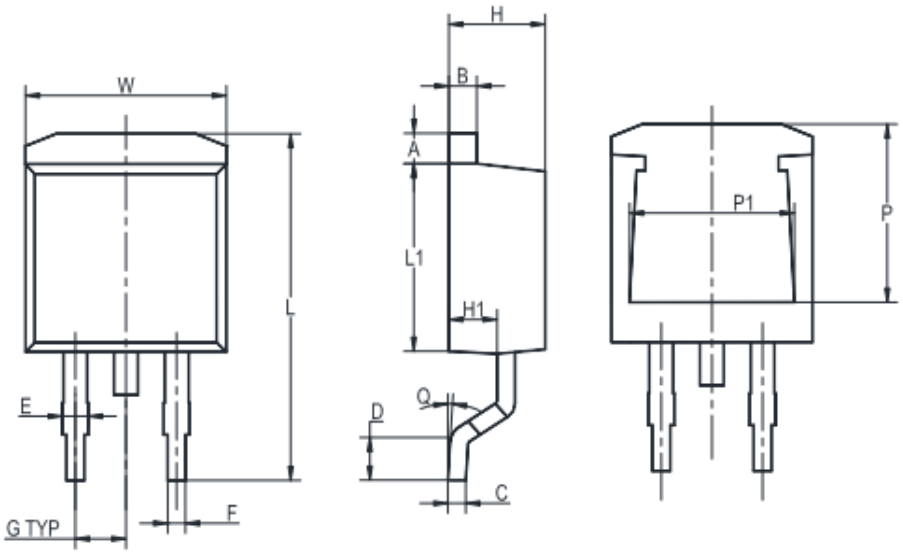



**Figure 9. Typical Gate Charge vs. Gate-to-Source Voltage**



## 5. Package Outlines




| UNIT | A | B | C | D | E | F | G | W | H | H1 | L | L1 | Q | P | P1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.5 | 1.5 | 0.5 | 2.60 | 1.6 | 0.94 | 2.54 | 10.5 | 4.8 | 2.9 | 16.5 | 8.7 | 8° | 7.6 | 8.2 |
| | 1.1 | 1.1 | 0.3 | 2.15 | 1.1 | 0.68 | TYP | 9.6 | 4.4 | 2.5 | 14.5 | 8.2 | MAX | 7.1 | 7.4 |

Figure1：Outline PG-TO263(HC)

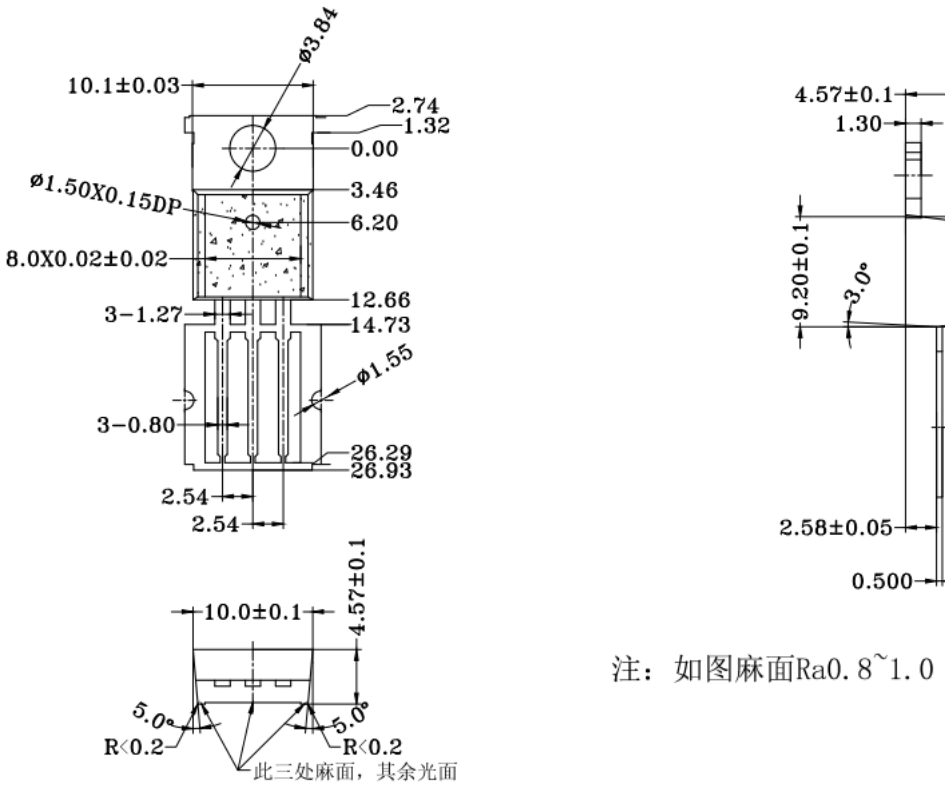
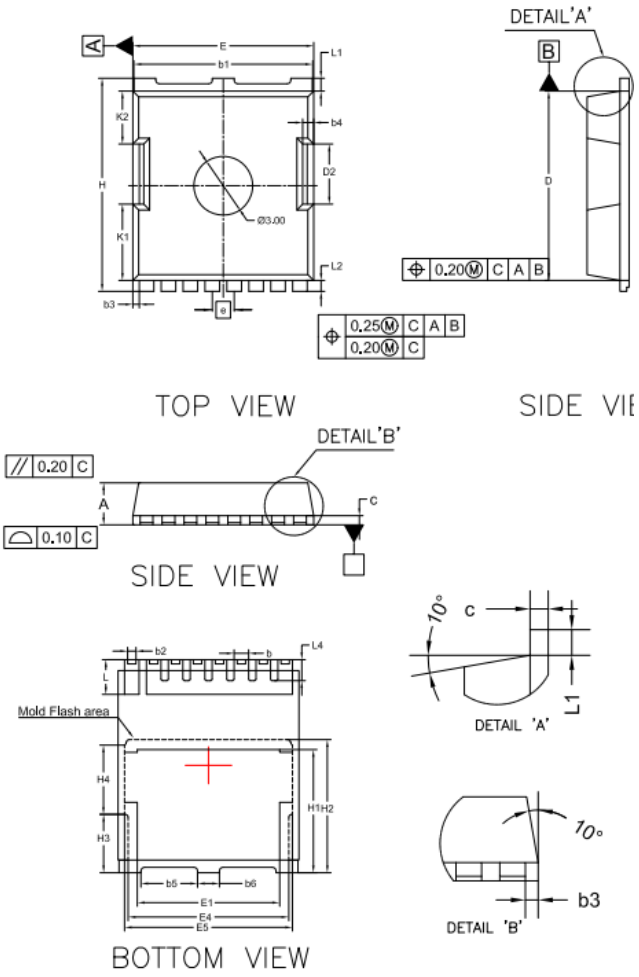



Figure2：Outline PG-TO220(HT)




| SYMBOLS | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| * A | 2.200 | 2.300 | 2.400 |
| c | 0.492 | 0.500 | 0.508 |
| * D | 10.280 | 10.380 | 10.480 |
| * E | 9.800 | 9.900 | 10.000 |
| e | | 1.20 BSC | |
| * H | 11.580 | 11.680 | 11.780 |
| H1 | 6.650 | 6.750 | 6.850 |
| H2 | | 7.300 | |
| H3 | | 3.200 | |
| H4 | | 3.800 | |
| K1 | | 4.180 | |
| K2 | | 2.900 | |
| * D2 | | 3.300 | |
| b | 0.700 | 0.800 | 0.900 |
| b1 | 9.700 | 9.800 | 9.900 |
| b2 | 0.420 | 0.460 | 0.500 |
| b3 | | 0.350 | |
| b4 | | 0.600 | |
| b5 | | 3.100 | |
| b6 | | 1.200 | |
| L | 1.700 | 1.900 | 2.100 |
| L1 | | 0.700 | |
| L2 | | 0.600 | |
| L4 | 1.050 | 1.150 | 1.250 |
| L5 | 0.500 | 0.600 | 0.700 |
| E1 | | 7.800 | |
| E4 | | 8.800 | |
| E5 | | 9.200 | |

Figure3：Outline PG-TOLL(JJW)

## Revision History

| Revision | Date | Subjects (major changes since last revision) |
|---|---|---|
| 1.0 | 2022-04-15 | Preliminary version |
| 1.1 | 2022-09-01 | Add TOLL package |