

Product Specification

Multiprotocol 80Km, 10Gb/s DWDM XFP Optical Transceiver

FTLX3815M3xx

PRODUCT FEATURES

- Supports 8.5Gb/s to 11.35Gb/s
- Hot-pluggable XFP footprint
- RoHS-6 Compliant (lead-free)
- 100GHz ITU Grid, C-Band
- Duplex LC connector
- Power dissipation <3.5W
- Built-in digital diagnostic functions
- Temperature range: 0°C to 70°C
- Point-to-Point & OSNR optimized versions
- Reference Clock Not Required



APPLICATIONS

- ITU G.698.1, DW100S-2Dx compliant DWDM 10G SONET/SDH
- ITU G.698.2, DW100C-2Ax compliant DWDM 10G SONET/SDH
- DWDM, IEEE 10GBASE-ZR based Ethernet
- 10GFC (SM-1200-LL-L) & 8GFC (SM-800-LC-L) compliant
- ITU G.709 / OTN FEC applications

Finisar's FTLX3815M3xx Small Form Factor 10Gb/s (XFP) transceiver complies with the XFP Multi-Source Agreement (MSA) Specification¹. It supports amplified DWDM 10Gb/s SONET/SDH, 10 Gigabit Ethernet, and 10 Gigabit Fibre Channel applications over 80km of fiber without dispersion compensation. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA. The transceiver is RoHS compliant and lead free per Directive 2002/95/EC³, and Finisar Application Note AN-2038⁴.

PRODUCT SELECTION

FTLX3815M3xx

xx: 100GHz ITU-T channel

1174161	Rev.: A04	Page 1 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

I. Pin Descriptions**II.**

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – Not used	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; Finisar defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply – Not used	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply – Not used	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not Required	
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not Required	
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.

1174161	Rev.: A04	Page 2 of 23
Finisar	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

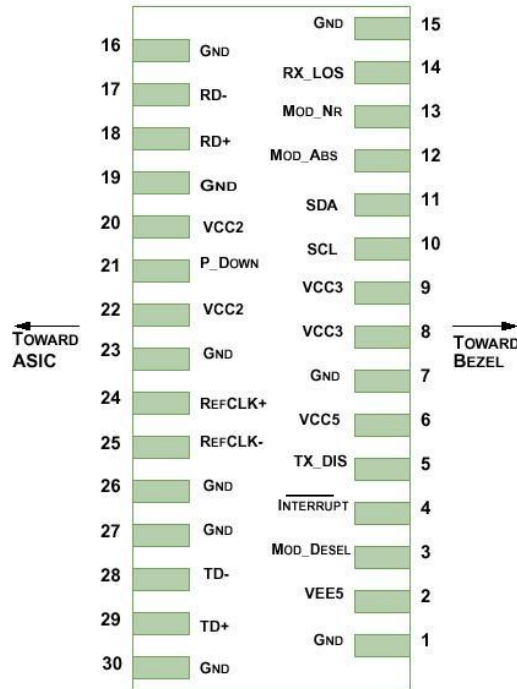


Diagram of Host Board Connector Block Pin Numbers and Names

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage #1	V _{cc3}	-0.5		4.0	V	
Maximum Supply Voltage #2	V _{cc2}	-0.5		6.0	V	
Storage Temperature	T _S	-40		85	°C	
Case Operating Temperature	T _{OP}	0		70	°C	
Receiver Damage Threshold	P _{Rdmg}	+5			dBm	

III. Electrical Characteristics (T_{OP} = -5 to 70 °C, V_{CC5} = 4.75 to 5.25 Volts)

FTLX3815M3xx							
Parameter	Symbol	Min	Typ	Max	Unit	Ref.	
Supply Voltage #1	V _{CC3}	3.13		3.46	V		
Supply Voltage #2	V _{CC5}	4.75		5.25	V		
Supply Current – V _{CC5} supply	I _{CC5}			450	mA		
Supply Current – V _{CC3} supply	I _{CC3}			750	mA		
Module total power dissipation	P			3.5	W	1	
Transmitter							
Input differential impedance	R _{in}		100		Ω	2	
Differential data input swing	V _{in,pp}	120		820	mV		
Transmit Disable Voltage	V _D	2.0		V _{CC}	V	3	
Transmit Enable Voltage	V _{EN}	GND		GND+ 0.8	V		
Receiver							
Differential data output swing	V _{out,pp}		500	850	mV	4	
Data output rise time	t _r			40	ps	5	
Data output fall time	t _f			40	ps	5	
LOS Fault	V _{LOS_fault}	V _{CC} – 0.5		V _{CC_HOST}	V	6	
LOS Normal	V _{LOS_norm}	GND		GND+0.5	V	6	
Power Supply Rejection	PSR	See Note 7 below					7
Reference Clock (AC-Coupled)							
Single-ended peak to peak voltage swing	V _{SEPP}	200		450	mV		
Single-ended resistance	R _L	40	50	60			
Frequency clock tolerance	Δf	-100		+100	ppm		
Duty cycle	-	40		60	%		

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. After internal AC coupling.
3. Or open circuit.
4. Into 100 ohms differential termination.
5. 20 – 80 %
6. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
7. Per Section 2.7.1. in the XFP MSA Specification¹.

1174161	Rev.: A04	Page 4 of 23
Finisar	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

XII. Optical Characteristics (EOL, T_{OP} = -5 to 70°C, V_{CC5} = 4.75 to 5.25 Volts)

Transmitter						
Parameter	Symbol	Min	Typ	Max	Unit	Ref
Output Opt. Pwr: 9/125 SMF	P _{OUT}	-1		+3	dBm	
Optical Extinction Ratio	ER	8.2			dB	
Center Wavelength Spacing			100		GHz	1
Transmitter Center Wavelength – End Of Life	λ _c	X-100	X	X+100	pm	2
Transmitter Center Wavelength – Beginning Of Life	λ _c	X-25	X	X+25	pm	2
Sidemode Suppression ratio	SSR _{min}	35			dB	
Tx Jitter Generation (peak-to-peak)	T _{Xj}			0.1	UI	3
Tx Jitter Generation (RMS)	T _{XjRMS}			0.01	UI	4
Tx Locked Eye (Cold Start)				30	s	

Receiver						
Overload	P _{MAX}	-6			dBm	
Optical Center Wavelength	λ _c	1270		1615	nm	
Receiver Reflectance	R _{rx}			-27	dB	
LOS De-Assert	LOS _D			-30	dBm	
LOS Assert	LOS _A	-37			dBm	
LOS Hysteresis		0.5			dB	

FTLX3815M3xx					
Receiver Sensitivity⁵					5
Data rate (Gb/s)	BER	Dispersion (ps/nm)	Sensitivity back-to-back at OSNR>30dB (dBm)	Power Penalty at OSNR>30dB (dB)	Threshold Adjust Required
8.5	1e-12	-500 to 1450	-24	3	No
9.95	1e-12	-500 to 1450	-24	3	No
10.3	1e-12	-500 to 1450	-24	3	No
10.7	1e-4	-500 to 1450	-27	3	Yes
11.1	1e-4	-500 to 1450	-27	3	Yes
11.3	1e-4	-500 to 1450	-27	3	Yes

1174161	Rev.: A04	Page 5 of 23
Finisar	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

OSNR Performance ⁶				6
Data rate (Gb/s)	BER	Dispersion (ps/nm)	Max OSNR w/ dispersion at Power: -7 to -18dBm (dB)	Threshold Adjustm. Required
8.5	1e-12	-500 to 1450	28	No
9.95	1e-12	-500 to 1450	28	No
10.3	1e-12	-500 to 1450	28	No
10.7	1e-4	-500 to 1300	22	Yes
11.1	1e-4	-500 to 1300	22	Yes
11.3	1e-4	-500 to 1100	22	Yes

Notes:

1. Corresponds to approximately 0.8 nm.
2. X = Specified ITU Grid wavelength. Wavelength stability is achieved within 10 seconds of power up.
3. Measured with a host jitter of 50 mUI peak-to-peak.
4. Measured with a host jitter of 7 mUI RMS.
5. Measured at 1528-1600nm with worst ER; PRBS31.
6. All OSNR measurements are performed with 0.1nm resolution.

1174161	Rev.: A04	Page 6 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

Part Numbers for Amplified (OSNR) Applications:

Channel #	Product Code	Frequency (THz)	Center Wavelength (nm)
17	FTLX3815M317	191.7	1563.86
18	FTLX3815M318	191.8	1563.05
19	FTLX3815M319	191.9	1562.23
20	FTLX3815M320	192.0	1561.42
21	FTLX3815M321	192.1	1560.61
22	FTLX3815M322	192.2	1559.79
23	FTLX3815M323	192.3	1558.98
24	FTLX3815M324	192.4	1558.17
25	FTLX3815M325	192.5	1557.36
26	FTLX3815M326	192.6	1556.55
27	FTLX3815M327	192.7	1555.75
28	FTLX3815M328	192.8	1554.94
29	FTLX3815M329	192.9	1554.13
30	FTLX3815M330	193.0	1553.33
31	FTLX3815M331	193.1	1552.52
32	FTLX3815M332	193.2	1551.72
33	FTLX3815M333	193.3	1550.92
34	FTLX3815M334	193.4	1550.12
35	FTLX3815M335	193.5	1549.32
36	FTLX3815M336	193.6	1548.51
37	FTLX3815M337	193.7	1547.72
38	FTLX3815M338	193.8	1546.92
39	FTLX3815M339	193.9	1546.12
40	FTLX3815M340	194.0	1545.32
41	FTLX3815M341	194.1	1544.53
42	FTLX3815M342	194.2	1543.73
43	FTLX3815M343	194.3	1542.94
44	FTLX3815M344	194.4	1542.14
45	FTLX3815M345	194.5	1541.35
46	FTLX3815M346	194.6	1540.56
47	FTLX3815M347	194.7	1539.77
48	FTLX3815M348	194.8	1538.98
49	FTLX3815M349	194.9	1538.19
50	FTLX3815M350	195.0	1537.40
51	FTLX3815M351	195.1	1536.61
52	FTLX3815M352	195.2	1535.82
53	FTLX3815M353	195.3	1535.04
54	FTLX3815M354	195.4	1534.25
55	FTLX3815M355	195.5	1533.47
56	FTLX3815M356	195.6	1532.68
57	FTLX3815M357	195.7	1531.90
58	FTLX3815M358	195.8	1531.12
59	FTLX3815M359	195.9	1530.33
60	FTLX3815M360	196.0	1529.55
61	FTLX3815M361	196.1	1528.77

1174161	Rev.: A04	Page 7 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

V. Additional Specifications and Response Timing

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate	BR	8.5		11.35	Gb/s	1
Maximum Supported Link Length	L _{MAX}		80		km	2

Notes:

1. Amplified SONET OC-192, 10G Ethernet, SONET OC-192 with FEC, 10G Ethernet with FEC, 10GFC, and 8GFC
2. Distance indicates dispersion budget. Optical amplification may be required to achieve maximum distance.

Response timing:

Parameter		Min	Typ	Max	Units	Ref.
Tx_Dis	Assert			10	us	
	De-assert			2	ms	
Rx_LOS	Asset			100	us	
	De-assert			100	us	
Mod_NR	Asset			1	ms	
	De-assert			1	ms	
Interrupt	Asset			200	ms	
	De-assert			500	us	
P_Down/RST Time		10			us	
P_Down/RST Asser Delay				100	us	
Start-up time (Initialize time)				300	ms	1

1. Time required for transponder to be ready to begin I2C communication with host from a cold start or a hardware reset condition.

1174161	Rev.: A04	Page 8 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

VI. Environmental Specifications

Finisar XFP transceivers have an operating temperature range from 0°C to +70°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T _{op}	0		70	°C	
Storage Temperature	T _{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar XFP transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard	Certificate Number
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50	TBD
Laser Eye Safety	TÜV	EN 60825-1: 1994+A11:1996+A2:2001 IEC 60825-1: 1993+A1:1997+A2:2001 IEC 60825-2: 2000, Edition 2	TBD
Electrical Safety	TÜV	EN 60950	TBD
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87	TBD

Copies of the referenced certificates are available at Finisar Corporation upon request.

1174161	Rev.: A04	Page 9 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

VIII. Digital Diagnostics Functions

As defined by the XFP MSA¹, Finisar XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage
- TEC Temperature

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information, including memory map definitions, please see the XFP MSA documentation¹.

Receiver Threshold Adjustment

The FTLX3815M3xx also provide access to receiver decision threshold adjustment via 2-wire serial interface, in order to improve receiver OSNR performance based on specific link conditions. It is implemented as follows:

- Rx Threshold of XFP transceivers will be factory-set for optimized performance in non-FEC applications. This will be the default value during both cold start (power-up) and warm start (module reset).

1174161	Rev.: A04	Page 10 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

- The transceiver supports adjustment of Rx Threshold value by the host through register 76d, table 01h. This is intended to be used in FEC applications.
- Register 76d, table 01h is a volatile memory. Therefore if the transceiver is power-cycled, the register starts up with a value of 00h which corresponds to the default Rx Threshold value.
- The threshold adjustment input value is 2's complement 7 bit value (-128 to +127). The default Rx threshold value will be approximately 0. Full range of adjustment provides at least a $\pm 10\%$ change in Rx threshold from the default value.

SBS suppression, dither tone

Set Address 111, bit 1 to “0” to enable tone, “1” to disable dither tone (defaults: frequency = 40kHz , tone is disabled). Please contact your Finisar RSM or PLM if specific amplitudes and frequencies are needed for SBS suppression.

8.5Gb/s Fibre-Channel CDR Bypass rate select:

For 8G FC operation, write “1” to Byte 116, bit 1. Every time that the module is power cycled, this will need to be re-written (bit goes back to “0” and CDR is now set for 10Gb/s operation) in order to operate properly at 8G FC.

Contact your Finisar RSM or PLM for details on the CDR Bypass.

Write “1” to Byte 116, bit 1. Every time that the module is power cycled, this will need to be re-written (bit goes back to “0” and CDR is now set for 10Gb/s operation) in order to operate properly at 8G FC.

1174161	Rev.: A04	Page 11 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

Alarm and Warning Threshold Values

Address	Parameter	Threshold Values	UNITS
02-03	Temp High Alarm	78	C
04-05	Temp Low Alarm	-13	C
06-07	Temp High Warning	73	C
08-09	Temp Low Warning	-8	C
10-17	Reserved		
18-19	Bias High Alarm	120	mA
20-21	Bias Low Alarm	10	mA
22-23	Bias High Warning	100	mA
24-25	Bias Low Warning	15	mA
26-27	TX Power High Alarm	+5	dBm
28-29	TX Power Low Alarm	-3	dBm
30-31	TX Power High Warning	+4	dBm
32-33	TX Power Low Warning	-2	dBm
34-35	RX Power High Alarm	-4	dBm
36-37	RX Power Low Alarm	-31	dBm
38-39	RX Power High Warning	-5	dBm
40-41	RX Power Low Warning	-25	dBm
42-43	AUX 1 High Alarm	57	C
44-45	AUX 1 Low Alarm	20	C
46-47	AUX 1 High Warning	54	C
48-49	AUX 1 Low Warning	25	C
50-51	AUX 2 High Alarm	3.564	V
52-53	AUX 2 Low Alarm	3.036	V
54-55	AUX 2 High Warning	3.465	V
56-57	AUX 2 Low Warning	3.135	V

A/D Table

Address	Parameter	Accuracy	Resolution	Units	Note s
96-97	Internal module Temp	+/-3	+/- 0.1	degC	PCB mounted thermocouple
98-99	Reserved				
100-101	TX bias current	+/-8	+/-2	uA	
102-103	Transmit Power	+/-1.5 dB	0.1	uW	
104-105	Receive Power	+/-1.5 dB	+/-0.1	uW	
106-107	Auxiliary monitor1	+/-3	+/-0.1	degC	Laser Temperature
108-109	Auxiliary monitor2	+/-3	+/-100	uV	3.3V Supply Voltage

1174161	Rev.: A04	Page 12 of 23
Finisar	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

EEPROM (Table A0h)

Byte Addr	Hex	LSB	Bit Size	Name	Description	Value	Hex Value
0	00	0	8	Identifier	Type of serial transceiver	6	6
1	01	0	8	Signal Conditioner Control	Signal Conditioner Control	0	0
2	02	0	16	Temp High Alarm	MSB at low address	78	
4	04	0	16	Temp Low Alarm	MSB at low address	-13	
6	06	0	16	Temp High Warning	MSB at low address	73	
8	08	0	16	Temp Low Warning	MSB at low address	-8	
10	0A	0	16	Aux3 High Alarm	MSB at low address	0	0000
12	0C	0	16	Aux3 Low Alarm	MSB at low address	0	0000
14	0E	0	16	Aux3 High Warning	MSB at low address	0	0000
16	10	0	16	Aux3 Low Warning	MSB at low address	0	0000
18	12	0	16	Bias High Alarm	MSB at low address	120	
20	14	0	16	Bias Low Alarm	MSB at low address	10	
22	16	0	16	Bias High Warning	MSB at low address	110	
24	18	0	16	Bias Low Warning	MSB at low address	15	
26	1A	0	16	TX Power High Alarm	MSB at low address	+5	
28	1C	0	16	TX Power Low Alarm	MSB at low address	-3	
30	1E	0	16	TX Power High Warning	MSB at low address	+4	
32	20	0	16	TX Power Low Warning	MSB at low address	-2	
34	22	0	16	RX Power High Alarm	MSB at low address	-4	
36	24	0	16	RX Power Low Alarm	MSB at low address	-31	
38	26	0	16	RX Power High Warning	MSB at low address	-5	
40	28	0	16	RX Power Low Warning	MSB at low address	-25	
42	2A	0	16	AUX 1 High Alarm	MSB at low address	57	
44	2C	0	16	AUX 1 Low Alarm	MSB at low address	20	
46	2E	0	16	AUX 1 High Warning	MSB at low address	54	
48	30	0	16	AUX 1 Low Warning	MSB at low address	25	
50	32	0	16	AUX 2 High Alarm	MSB at low address	3.564	
52	34	0	16	AUX 2 Low Alarm	MSB at low address	3.036	
54	36	0	16	AUX 2 High Warning	MSB at low address	3.465	
56	38	0	16	AUX 2 Low Warning	MSB at low address	3.135	
58	3A	0	16	Optional VPS Control Registers	Optional VPS Control Registers	0	
60	3C	0	80	RESERVED	RESERVED	NA	NA
70	46	0	8	Acceptable BER	Acceptable BER Reported by the FEC to the Module	0	0
71	47	0	8	Actual BER	Actual BER Reported by the FEC to the Module	0	0
72	48	0	8	Wavelength Set MSB	User input of Wavelength setpoint. (Units of 0.05nm)	0	0
73	49	0	8	Wavelength Set LSB	User input of Wavelength setpoint. (Units of 0.05nm)	0	0
74	4A	0	8	Wavelength Error MSB	Monitor of Current Wavelength Error. (Units of 0.005nm)	0	0
75	4B	0	8	Wavelength Error MSB	Signed 2's complement value	0	0
76	4C	0	8	Amplitude Adjustment	Relative amplitude of receive quantization threshold	0	0
77	4D	0	8	Phase Adjustment	Phase of receive quantization relative to 0.5 UI	0	0
78	4E	0	16	RESERVED	RESERVED	NA	NA
80	50	0	1	L- TX Power Low Alarm	Latched low TX Power alarm.	FALSE	0
80	50	1	1	L- TX Power High Alarm	Latched high TX Power alarm.	FALSE	0
80	50	2	1	L- TX Bias Low Alarm	Latched low TX Bias alarm.	FALSE	0
80	50	3	1	L- TX Bias High Alarm	Latched high TX Bias alarm.	FALSE	0
80	50	4	1	L- Vcc Low Alarm	Latched low Vcc alarm.	FALSE	0
80	50	5	1	L- Vcc High Alarm	Latched high Vcc alarm.	FALSE	0
80	50	6	1	L- Temp Low Alarm	Latched low Temperature alarm.	FALSE	0
80	50	7	1	L- Temp High Alarm	Latched high Temperature alarm	FALSE	0
81	51	0	1	RESERVED	RESERVED	NA	NA
81	51	1	1	RESERVED	RESERVED	NA	NA
81	51	2	1	L- AUX 2 Low Alarm	Latched low AUX2 monitor alarm.	FALSE	0
81	51	3	1	L- AUX 2 High Alarm	Latched high AUX2 monitor alarm.	FALSE	0
81	51	4	1	L- AUX 1 Low Alarm	Latched low AUX1 monitor alarm.	FALSE	0
81	51	5	1	L- AUX 1 High Alarm	Latched high AUX1 monitor alarm.	FALSE	0
81	51	6	1	L- RX Power Low Alarm	Latched low RX Power alarm.	FALSE	0
81	51	7	1	L- RX Power High Alarm	Latched high RX Power alarm.	FALSE	0

1174161

Rev.: A04

Page 13 of 23

Finisar

This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.

Printed copy may not be the latest revision please refer to Agile for current revision

EEPROM (Table A0h) continued

82	52	0	1	L- TX Power Low Warning	Latched low TX Power warning.	FALSE	0
82	52	1	1	L- TX Power High Warning	Latched high TX Power warning.	FALSE	0
82	52	2	1	L- TX Bias Low Warning	Latched low TX Bias warning.	FALSE	0
82	52	3	1	L- TX Bias High Warning	Latched high TX Bias warning.	FALSE	0
82	52	4	1	L- Vcc Low Warning	Latched low Vcc warning.	FALSE	0
82	52	5	1	L- Vcc High Warning	Latched high Vcc warning.	FALSE	0
82	52	6	1	L- Temp Low Warning	Latched low Temperature warning.	FALSE	0
82	52	7	1	L- Temp High Warning	Latched high Temperature warning.	FALSE	0
83	53	0	1	RESERVED	RESERVED	NA	NA
83	53	1	1	RESERVED	RESERVED	NA	NA
83	53	2	1	L- AUX 3 Low Warning	Latched low AUX2 monitor warning.	FALSE	0
83	53	3	1	L- AUX 2 High Warning	Latched high AUX2 monitor warning.	FALSE	0
83	53	4	1	L- AUX 1 Low Warning	Latched low AUX1 monitor warning.	FALSE	0
83	53	5	1	L- AUX 1 High Warning	Latched high AUX1 monitor warning.	FALSE	0
83	53	6	1	L- RX Power Low Warning	Latched low RX Power warning.	FALSE	0
83	53	7	1	L- RX Power High Warning	Latched high RX Power warning.	FALSE	0
84	54	0	1	L- Reset Complete	Latched Reset Complete Flag	FALSE	0
84	54	1	1	L- MOD_NR	Latched Mirror of MOD_NR pin	FALSE	0
84	54	2	1	L- RX CDR not Locked	Latched RX CDR Loss of Lock	FALSE	0
84	54	3	1	L- LOS	Latched mirror of LOS pin (RX optical loss of signal)	FALSE	0
84	54	4	1	L- RX_NR	Latched RX_NR Status	FALSE	0
84	54	5	1	L- TX CDR not Locked	Latched TX CDR Loss of Lock	FALSE	0
84	54	6	1	L- TX_Fault	Latched Laser Fault condition. Generated by laser safety system.	FALSE	0
84	54	7	1	L- TX_NR	Latched TX_NR Status.	FALSE	0
85	55	0	5	RESERVED	RESERVED	NA	NA
85	55	5	1	L- Wavelength Unlocked	Latched Wavelength Unlocked Condition	FALSE	0
85	55	6	1	L- TEC Fault	Latched TEC Fault	FALSE	0
85	55	7	1	L- APD Supply Fault	Latched APD Supply Fault	FALSE	0
86	56	0	16	RESERVED	RESERVED	NA	NA
88	58	0	1	M- TX Power Low Alarm	Masking bit for low TX Power alarm.	FALSE	0
88	58	1	1	M- TX Power High Alarm	Masking bit for high TX Power alarm.	FALSE	0
88	58	2	1	M- TX Bias Low Alarm	Masking bit for low TX Bias alarm.	FALSE	0
88	58	3	1	M- TX Bias High Alarm	Masking bit for high TX Bias alarm.	FALSE	0
88	58	4	1	M- Vcc Low Alarm	Masking bit for low Vcc alarm.	FALSE	0
88	58	5	1	M- Vcc High Alarm	Masking bit for high Vcc alarm.	FALSE	0
88	58	6	1	M- Temp Low Alarm	Masking bit for low Temperature alarm.	FALSE	0
88	58	7	1	M- Temp High Alarm	Masking bit for high Temperature alarm.	FALSE	0
89	59	0	1	RESERVED	RESERVED	NA	NA
89	59	1	1	RESERVED	RESERVED	NA	NA
89	59	2	1	M- AUX 2 Low Alarm	Masking bit for low AUX2 monitor alarm.	FALSE	0
89	59	3	1	M- AUX 2 High Alarm	Masking bit for high AUX2 monitor alarm.	FALSE	0
89	59	4	1	M- AUX 1 Low Alarm	Masking bit for low AUX1 monitor alarm.	FALSE	0
89	59	5	1	M- AUX 1 High Alarm	Masking bit for high AUX1 monitor alarm.	FALSE	0
89	59	6	1	M- RX Power Low Alarm	Masking bit for low RX Power alarm.	FALSE	0
89	59	7	1	M- RX Power High Alarm	Masking bit for high RX Power alarm.	FALSE	0
90	5A	0	1	M- TX Power Low Warning	Masking bit for low TX Power warning.	FALSE	0
90	5A	1	1	M- TX Power High Warning	Masking bit for high TX Power warning.	FALSE	0
90	5A	2	1	M- TX Bias Low Warning	Masking bit for low TX Bias warning.	FALSE	0
90	5A	3	1	M- TX Bias High Warning	Masking bit for high TX Bias warning.	FALSE	0
90	5A	4	1	M- Vcc Low Warning	Masking bit for low Vcc warning.	FALSE	0
90	5A	5	1	M- Vcc High Warning	Masking bit for high Vcc warning.	FALSE	0
90	5A	6	1	M- Temp Low Warning	Masking bit for low Temperature warning.	FALSE	0
90	5A	7	1	M- Temp High Warning	Masking bit for high Temperature warning.	FALSE	0
91	5B	0	1	RESERVED	RESERVED	NA	NA
91	5B	1	1	RESERVED	RESERVED	NA	NA
91	5B	2	1	M- AUX 2 Low Warning	Masking bit for low AUX2 monitor warning.	FALSE	0
91	5B	3	1	M- AUX 2 High Warning	Masking bit for high AUX2 monitor warning.	FALSE	0
91	5B	4	1	M- AUX 1 Low Warning	Masking bit for low AUX1 monitor warning.	FALSE	0
91	5B	5	1	M- AUX 1 High Warning	Masking bit for high AUX1 monitor warning.	FALSE	0
91	5B	6	1	M- RX Power Low Warning	Masking bit for low RX Power warning.	FALSE	0
91	5B	7	1	M- RX Power High Warning	Masking bit for high RX Power warning.	FALSE	0
92	5C	0	1	M- Reset Complete	Masking bit for Reset Complete Flag	FALSE	0
92	5C	1	1	M- MOD_NR	Masking bit for Mirror of MOD-NR pin	FALSE	0
92	5C	2	1	M- RX CDR not Locked	Masking bit for RX CDR Loss of Lock	FALSE	0
92	5C	3	1	M- LOS	Masking bit for mirror of LOS pin (RX optical loss of signal)	FALSE	0
92	5C	4	1	M- RX_NR	Masking bit for RX_NR Status	FALSE	0
92	5C	5	1	M- TX CDR not Locked	Masking bit for TX CDR Loss of Lock	FALSE	0
92	5C	6	1	M- TX_Fault	Masking bit for Laser Fault condition. Generated by laser safety system.	FALSE	0
92	5C	7	1	M- TX_NR	Masking bit for TX_NR Status	FALSE	0

EEPROM (Table A0h) continued

93	5D	0	5	RESERVED	RESERVED	NA	NA
93	5D	5	1	M- Wavelength Unlocked	Masking bit for Wavelength Unlocked Condition	FALSE	0
93	5D	6	1	M- TEC Fault	Masking bit for TEC Fault	FALSE	0
93	5D	7	1	M- APD Supply Fault	Masking bit for APD Supply Fault	FALSE	0
94	5E	0	16	RESERVED	RESERVED	NA	NA
96	60	0	8	Temperature MSB	Internally measured module temperature	0	0
97	61	0	8	Temperature LSB	Internally measured module temperature	0	0
98	62	0	8	Vcc MSB	Internally measured supply voltage in transceiver	0	0
99	63	0	8	Vcc LSB	Internally measured supply voltage in transceiver	0	0
100	64	0	8	TX Bias MSB	Internally measured TX Bias Current	0	0
101	65	0	8	TX Bias LSB	Internally measured TX Bias Current	0	0
102	66	0	8	TX Power MSB	Measured TX output power	0	0
103	67	0	8	TX Power LSB	Measured TX output power	0	0
104	68	0	8	RX Power MSB	Measured RX output power	0	0
105	69	0	8	RX Power LSB	Measured RX output power	0	0
106	6A	0	8	AUX 1 MSB	Auxiliary measurement 1 defined in Byte 222 Page 01h	0	0
107	6B	0	8	AUX 1 LSB	Auxiliary measurement 1 defined in Byte 222 Page 01h	0	0
108	6C	0	8	AUX 2 MSB	Auxiliary measurement 2 defined in Byte 222 Page 01h	0	0
109	6D	0	8	AUX 2 LSB	Auxiliary measurement 2 defined in Byte 222 Page 01h	0	0
110	6E	0	1	Data_Not_Ready	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.	0	0
110	6E	1	1	LOS	Indicates Optical Loss of Signal (per relevant optical link standard). Updated within 100msec of change on pin	FALSE	0
110	6E	2	1	Interrupt	Digital state of the Interrupt output pin	FALSE	0
110	6E	3	1	Soft P_Down	Read/write bit that allows the module to be placed in the power down mode. This is identical to the P_Down hardware pin function except that it does not initiate a system reset	FALSE	0
110	6E	4	1	P_Down State	Digital state of the P_Down Pin. Updated within 100msec of change on pin	FALSE	0
110	6E	5	1	MOD_NR State	Digital state of the MOD_NR Pin. Updated within 100msec of change on pin	FALSE	0
110	6E	6	1	Soft TX Disable	Read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100msec max from acknowledgement of serial byte transmission. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.	0	0
110	6E	7	1	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin	FALSE	0
111	6F	0	3	RESERVED	RESERVED		
111	6F	3	1	RX_CDR not Locked	Identifies Loss of Lock in RX path CDR	FALSE	0
111	6F	4	1	RX_NR State	Identifies Not Ready condition as specific to the TX path	FALSE	0
111	6F	5	1	TX_CDR not Locked	Identifies Loss of Lock in TX path CDR	FALSE	0
111	6F	6	1	TX_Fault State	Identifies Laser fault condition (Generated by laser safety system)	FALSE	0
111	6F	7	1	TX_NR State	Identifies Not Ready condition as specific to the TX path	FALSE	0
112	70	0	48	RESERVED	RESERVED	NA	NA
118	76	0	1	Error Checking	Error Checking	Packet error checking not supported	0
118	76	1	7	RESERVED	RESERVED	NA	NA
119	77	0	32	New Password Entry	Location of Entry of New Optional Password	0	00 00 00 00
123	7B	0	32	Password Entry	Location for Entry of Optional Password	0	00 00 00 00
127	7F	0	8	Table Select	Entry Location for Table Select Byte	1	1

1174161

Rev.: A04

Page 15 of 23

Finisar

This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.

Printed copy may not be the latest revision please refer to Agile for current revision

EEPROM (Table 01h)

Byte Addr	Hex	LSB	Bit Size	Name	Description	Value	Hex Value
128	80	0	8	Identifier	Type of serial transceiver	XFP	6
129	81	0	3	RESERVED	RESERVED	NA	NA
129	81	3	1	CLEI code present in Table 02h	CLEI code present in Table 02h	No CLEI code present in Table 02h	0
129	81	4	1	TX Ref Clock Input Required	TX Ref Clock Input Required	Not Required	1
129	81	5	1	Module with CDR	Module with CDR	with CDR	0
129	81	6	2	Ext.Identifier	Defines Module Power Class	Power level 3 (<3.5W)	2
130	82	0	8	Connector	Code for connector type	LC	7
131	83	0	1	RESERVED	RESERVED	NA	NA
131	83	1	1	10GBASE-EW	10GBASE-EW	FALSE	0
131	83	2	1	10GBASE-LW	10GBASE-LW	FALSE	0
131	83	3	1	10GBASE-SW	10GBASE-SW	FALSE	0
131	83	4	1	10GBASE-LRM	10GBASE-LRM	FALSE	0
131	83	5	1	10GBASE-ER	10GBASE-ER	FALSE	0
131	83	6	1	10GBASE-LR	10GBASE-LR	FALSE	0
131	83	7	1	10GBASE-SR	10GBASE-SR	FALSE	0
132	84	0	4	RESERVED	RESERVED	NA	NA
132	84	4	1	Intermediate Reach 1300 nm FP	Intermediate Reach 1300 nm FP	FALSE	0
132	84	5	1	Extended Reach 1550 nm	Extended Reach 1550 nm	FALSE	0
132	84	6	1	1200-SM-LL-L	1200-SM-LL-L	FALSE	0
132	84	7	1	1200-MX-SN-I	1200-MX-SN-I	FALSE	0
133	85	0	8	RESERVED	RESERVED	NA	NA
134	86	0	1	RESERVED	RESERVED	NA	NA
134	86	1	1	OC-48-LR	Lower speed link compliance code	FALSE	0
134	86	2	1	OC-48-IR	Lower speed link compliance code	FALSE	0
134	86	3	1	OC-48-SR	Lower speed link compliance code	FALSE	0
134	86	4	1	2xFC SMF	Lower speed link compliance code	FALSE	0
134	86	5	1	2xFC MMF	Lower speed link compliance code	FALSE	0
134	86	6	1	1000BASE-LX/1xFC SMF	Lower speed link compliance code	FALSE	0
134	86	7	1	1000BASE-SX/1xFC MMF	Lower speed link compliance code	FALSE	0
135	87	0	2	RESERVED	RESERVED	NA	NA
135	87	2	1	I-64.5	Sonet codes	FALSE	0
135	87	3	1	I-64.3	Sonet codes	FALSE	0
135	87	4	1	I-64.2	Sonet codes	FALSE	0
135	87	5	1	I-64.2r	Sonet codes	FALSE	0
135	87	6	1	I-64.1	Sonet codes	FALSE	0
135	87	7	1	I-64.1r	Sonet codes	FALSE	0
136	88	0	1	RESERVED	RESERVED	NA	NA
136	88	1	1	S-64.5b	Sonet Short Haul Link codes	FALSE	0
136	88	2	1	S-64.5a	Sonet Short Haul Link codes	FALSE	0
136	88	3	1	S-64.3b	Sonet Short Haul Link codes	FALSE	0
136	88	4	1	S-64.3a	Sonet Short Haul Link codes	FALSE	0
136	88	5	1	S-64.2c	Sonet Short Haul Link codes	FALSE	0
136	88	6	1	S-64.2a	Sonet Short Haul Link codes	FALSE	0
136	88	7	1	S-64.1	Sonet Short Haul Link codes	FALSE	0
137	89	0	1	RESERVED	RESERVED	NA	NA
137	89	1	1	DWDM	DWDM	FALSE	0
137	89	2	1	G.959.1 P1L1-2D2	Sonet Long Haul Link codes	TRUE	1
137	89	3	1	L-64.3	Sonet Long Haul Link codes	FALSE	0
137	89	4	1	L-64.2c	Sonet Long Haul Link codes	FALSE	0
137	89	5	1	L-64.2b	Sonet Long Haul Link codes	FALSE	0
137	89	6	1	L-64.2a	Sonet Long Haul Link codes	FALSE	0
137	89	7	1	L-64.1	Sonet Long Haul Link codes	FALSE	0
138	8A	0	5	RESERVED	RESERVED	NA	NA
138	8A	5	1	V-64.3	Sonet Very Long Haul Link codes	FALSE	0
138	8A	6	1	V-64.2b	Sonet Very Long Haul Link codes	FALSE	0
138	8A	7	1	V-64.2a	Sonet Very Long Haul Link codes	FALSE	0
139	8B	0	2	RESERVED	RESERVED	NA	NA
139	8B	2	1	Tx Dither Supported		TRUE	1
139	8B	3	1	RZ	Encoding Support	FALSE	0
139	8B	4	1	NRZ	Encoding Support	TRUE	1
139	8B	5	1	Sonet Scrambled	Encoding Support	TRUE	1
139	8B	6	1	8B/10B	Encoding Support	TRUE	1
139	8B	7	1	64B/66B	Encoding Support	TRUE	1
140	8C	0	8	BR, minimum	Minimum Supported Bitrate (/100Mb)	99	63
141	8D	0	8	BR, maximum	Maximum Supported Bitrate (/100Mb)	113	71
142	8E	0	8	Length(SMF)-km	LENGTH (STANDARD SINGLE MODE FIBER)-KM	80	50
143	8F	0	8	Length(EMM-50um)-meter	LENGTH (EXTENDED BANDWIDTH 50 um MULTIMODE FIBER) (/2m)	0	0

EEPROM (Table 01h) continued

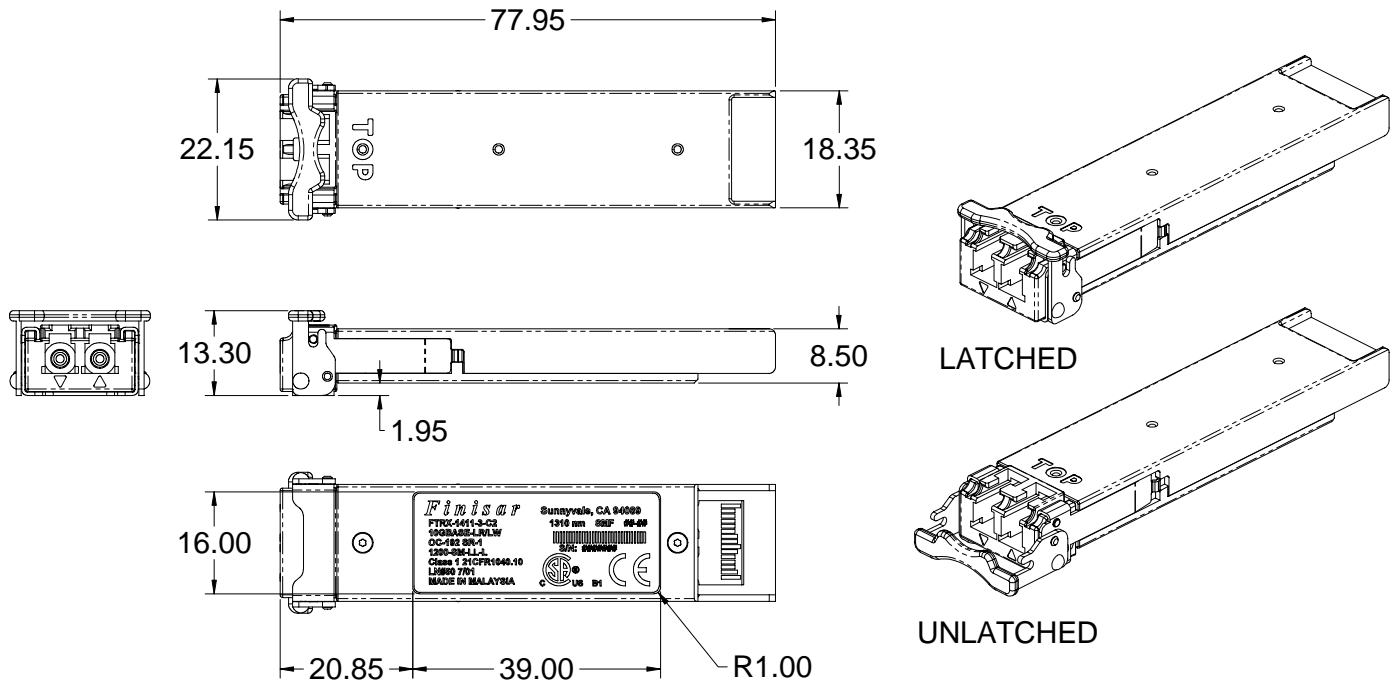
144	90	0	8	Length(50)-meter	LENGTH (50 UM MULTIMODE FIBER) (/1meter)	0	0
145	91	0	8	Length(62.5)-meter	LENGTH (62.5 UM MULTIMODE FIBER)(/1meter)	0	0
146	92	0	8	Length(Copper)-km	LENGTH (COPPER) (/1meter)	0	0
147	93	0	1	Tunable Transmitter	Device Technology	FALSE	0
147	93	1	1	Detector Type	Device Technology	APD	1
147	93	2	1	Cooled Transmitter	Device Technology	TRUE	1
147	93	3	1	Wavelength Control	Device Technology	FALSE	0
147	93	4	4	Transmitter Technology	Device Technology	1550 nm EML	7
148	94	0	128	Vendor Name	Vendor Name (ascii)	Finisar	46 69 6E 69 73 61 72 20 20 20 20 20 20 20 20 20
164	A4	0	1	XFI Loopback Supported	CDR support	TRUE	1
164	A4	1	1	Lineside Loopback Mode Supported	CDR support	FALSE	0
164	A4	2	1	RESERVED	RESERVED	NA	NA
164	A4	3	1	CDR support for 11.1 Gb/s	CDR support	TRUE	1
164	A4	4	1	CDR support for 10.7 Gb/s	CDR support	TRUE	1
164	A4	5	1	CDR support for 10.5 Gb/s	CDR support	TRUE	1
164	A4	6	1	CDR support for 10.3 Gb/s	CDR support	TRUE	1
164	A4	7	1	CDR support for 9.95 Gb/s	CDR support	TRUE	1
165	A5	0	24	Vendor OUI	SFP vendor IEEE company ID	00 90 65h (36965 Decimal)	00 90 65
168	A8	0	128	Vendor PN	Part number provided by vendor (ASCII)	FTLX3815M3xx	Variable
184	B8	0	16	Vendor Rev	Revision level for part number provided by vendor (ASCII)	0	Variable
186	BA	0	16	Wavelength	Nominal laser wavelength (Wavelength=value/20 in nm)	Variable	Variable
188	BC	0	16	Wavelength Tolerance	Guaranteed range of laser wavelength (+/- value) from Nominal wavelength. (Wavelength Tol. = value/200 in nm)	04	0004
190	BE	0	8	Max Case Temp	MAXIMUM CASE TEMPERATURE	70	46
191	BF	0	8	CC_BASE	Checksum (128 to 190)		Variable
192	C0	0	8	Maximum Power	Maximum Power Dissipation, Max power is 8 bit value * 20 mW.	175	AF
193	C1	0	8	Max Power in Power Down Mode	Maximum Total Power Dissipation in Power Down Mode, Max Power is 8 bit value * 10 mW.	100	64
194	C2	0	4	Max Current +3.3v	Maximum current required by +3.3V Supply. Max current is 4 bit value * 100 mA.	8	8
194	C2	4	4	Max Current +5v	Maximum current required by +5V Supply. Max current is 4 bit value * 50 mA. [500 mA max]	9	9
195	C3	0	4	Max Current -5v	Maximum current required by -5.2V Supply. Max current is 4 bit value * 50 mA. [500 mA max]	0	0
195	C3	4	4	Max Current +1.8v	Maximum current required by +1.8V Supply. Max current is 4 bit value * 100 mA.	0	0
196	C4	0	128	Vendor SN	Serial number provided by vendor (ASCII)	Variable	Variable
212	D4	0	16	Date Code - Year	Two low order digits of year (00 = 2000) - ASCII code	Variable	Variable
214	D6	0	16	Date Code - Month	Digits of month (01=JAN ~ 12=DEC) - ASCII code	Variable	Variable
216	D8	0	16	Date Code - Day	Digits of day (01-31) - ASCII code	Variable	Variable
218	DA	0	16	Date Code - Vendor specific lot code	Vendor specific lot code, may be left blank - ASCII code	0	0
220	DC	0	3	RESERVED	RESERVED	NA	NA
220	DC	3	1	Received power meas. Type	Special functions	Average power	1
220	DC	4	1	FEC BER support	Special functions	FALSE	0
220	DC	5	3	AUX3 (Finisar)	Aux3 minitor (1612 only)	RESERVED	0
221	DD	0	1	Optional CMU support mode	Enhanced Options	FALSE	0
221	DD	1	1	Wavelength Tunability implemented	Enhanced Options	FALSE	0
221	DD	2	1	Active FEC control function implemented	Enhanced Options	TRUE	1
221	DD	3	1	Support VPS bypass regulator mode	Enhanced Options	FALSE	0
221	DD	4	1	Support VPS LV regulator mode	Enhanced Options	FALSE	0
221	DD	5	1	Soft P_Down	Enhanced Options	TRUE	1
221	DD	6	1	Soft TX_DISABLE	Enhanced Options	TRUE	1
221	DD	7	1	Variable Power Supply Support	Enhanced Options	FALSE	0
222	DE	0	4	Aux A/D Input 2	Enhanced Options	+3.3V Supply Voltage	7
222	DE	4	4	Aux A/D Input 1	Enhanced Options	Laser Temperature	4
223	DF	0	8	CC_EXT	Check code for bytes 192 to 222		Variable
224	E0	0	256	Vendor Specific	Vendor Specific EEPROM	0	0000000000000000 0000000000000000 0000000000000000 0000000000000000 0000

EEPROM (Table 02h)

All Bytes except 128 and 129 filled with “00” unless otherwise specified by customer requirements. Addresses 128 and 129 are filled with “FF”.

IX. Mechanical Specifications

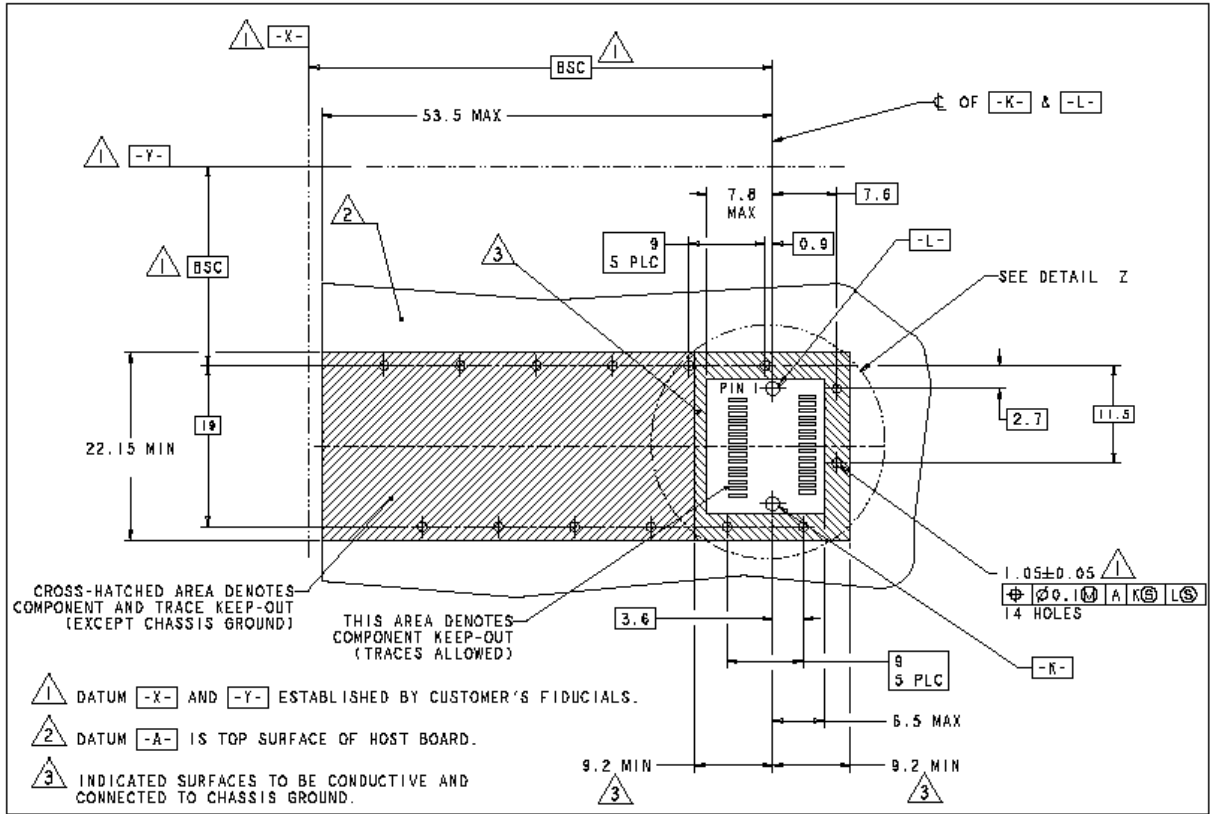
Finisar’s XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).



XFP Transceiver (dimensions are in mm)

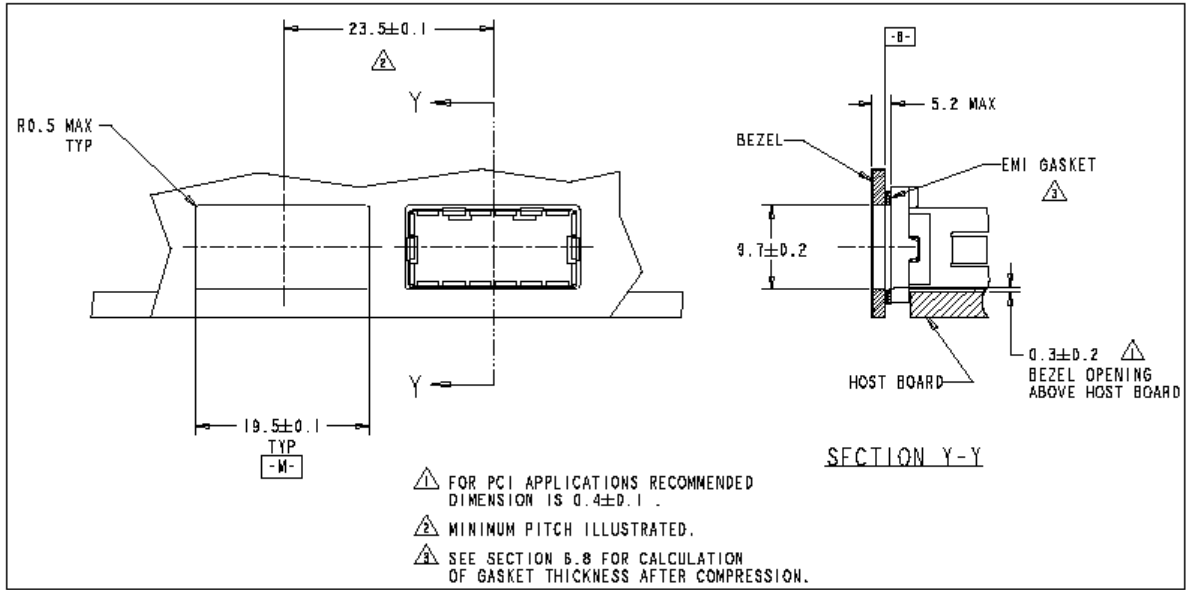
1174161	Rev.: A04	Page 18 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

X. PCB Layout and Bezel Recommendations



XFP Host Board Mechanical Layout (dimensions are in mm)

1174161	Rev.: A04	Page 19 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		



XFP Recommended Bezel Design (dimensions are in mm)

1174161	Rev.: A04	Page 21 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

XI. Notes & Exceptions

- The FTLX3815 product family has the following exceptions to the XFP MSA;
 - Initialize time of 2 sec maximum (MSA requires 300ms).
- XFI loopback operation:
 - When XFI Loopback is enabled, the Transmitter output is disabled.
 - When Line Loopback is enabled, the Receiver input is disabled.
- 8.5Gb/s operation requires configuration change via I2C vendor reserved command.

XIII. References

2. 10 Gigabit Small Form Factor Pluggable Module (XFP) Multi-Source Agreement (MSA), Rev 4.5 – August 2005. Documentation is currently available at <http://www.xfpmsa.org/>
3. Application Note AN-2035: “Digital Diagnostic Monitoring Interface for XFP Optical Transceivers” – Finisar Corporation, December 2003
4. Directive 2002/95/EC of the European Council Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment”. January 27, 2003.
5. “Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers”, Finisar Corporation, January 21, 2005.

1174161	Rev.: A04	Page 22 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		

XIII. Product Selection Details

FTLX3815M3xx

FT: FT Series

L: RoHS-6

X: 10G Bit Rate Class

38: 80km (asymmetric chirp)

1: XFP form factor

5: Standard Performance Class

M: Multiprotocol

3: Commercial temperature range

xx: Sub-Band start channel (please refer to page 6 for channel definition)

XIV. Revision History

Revision	Date	Description
A00	8/15/2012	Preliminary document created
A01	10/22/2012	Update EEPROM Table A0h and 01h
A02	10/31/2012	Include cold start timing, correct initialization timing, SBS/Dither Byte
A03	6/11/2014	Update TX Bias High Warning; EEPROM: update values for Bytes 188, 189, 193 in Table 01h, and values for Bytes 128 and 129 in Table 02h.
A04	11/1/2014	Data output Rise and Fall times adjusted to 40ps max.

XV. For more information

Finisar Corporation
 1389 Moffett Park Drive
 Sunnyvale, CA 94089-1133
 Tel. 1-408-548-1000
 Fax 1-408-541-6138
sales@finisar.com
www.finisar.com

1174161	Rev.: A04	Page 23 of 23
<i>Finisar</i>	This document contains proprietary and confidential information to Finisar Corp. This document and the entire information contained herein, and any other tangible representation thereof, is not to be copied, reproduced, duplicated, distributed, or modified, in whole or in part, and/or used without the expressed written consent of Finisar Corp.	
Printed copy may not be the latest revision please refer to Agile for current revision		