**Vishay Semiconductors** 

### Thyristor/Thyristor (MAGN-A-PAK Power Modules), 320 A



MAGN-A-PAK

320 A

Modules - thyristor, standard

MAGN-A-PAK

**PRIMARY CHARACTERISTICS** 

 $I_{T(AV)}$ 

Туре

Package

### FEATURES

- High voltage
- Electrically isolated base plate
- 3600  $V_{\text{RMS}}$  isolating voltage
- Industrial standard package
- · Simplified mechanical designs, rapid assembly
- High surge capability
- Large creepage distances
- UL approved file E78996
- Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

### DESCRIPTION

This VSK series of MAGN-A-PAK modules uses high voltage power thyristor/thyristor in doubler circuit configuration. The semiconductors are electrically isolated from the metal base, allowing common heatsinks and compact assemblies to be built. They can be interconnected to form single phase or three phase bridges or as AC-switches when modules are connected in anti-parallel mode. These modules are intended for general purpose applications such as battery chargers, welders, motor drives, UPS, etc.

MAJOR RATINGS AND CHARACTERISTICS						
SYMBOL	CHARACTERISTICS	VALUES	UNITS			
I <sub>T(AV)</sub>	70 °C	320				
I <sub>T(RMS)</sub>		710	A			
I <sub>TSM</sub>	50 Hz	9000	A			
	60 Hz	9420	]			
l <sup>2</sup> t	50 Hz	405	- kA <sup>2</sup> s			
	60 Hz	370	KA-S			
l²√t		4050	kA²√s			
V <sub>DRM</sub> /V <sub>RRM</sub>		1200 to 1600	V			
TJ	Range	-40 to +130	°C			

### **ELECTRICAL SPECIFICATIONS**

VOLTAGE R	ATINGS				
TYPE NUMBER	VOLTAGE CODE	V <sub>RRM</sub> /V <sub>DRM</sub> , MAXIMUM REPETITIVE PEAK REVERSE AND OFF-STATE BLOCKING VOLTAGE V	V <sub>RSM</sub> , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I <sub>RRM</sub> /I <sub>DRM</sub> AT 130 °C MAXIMUM mA	
VS-VSKT320-	12	1200	1300	50	
vo-vor 1320-	16	1600	1700	50	



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SHAY

## **VS-VSKT320PbF Series**

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PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current	I-reaso	180° conduction	half sine wave		320	А
at case temperature	I <sub>T(AV)</sub>		, nan sine wave		70	°C
Maximum RMS on-state current	I <sub>T(RMS)</sub>	As AC switch			710	
		t = 10 ms	No voltage		9000	
Maximum peak, one-cycle on-state		t = 8.3 ms	reapplied		9420	A
non-repetitive, surge current	I <sub>TSM</sub>	t = 10 ms	100 % V <sub>BBM</sub>		7570	
		t = 8.3 ms	reapplied	Sinusoidal half wave,	7920	
		t = 10 ms	No voltage	initial T <sub>J</sub> =	405	- kA <sup>2</sup> s
Manufacture 124 for function of	l <sup>2</sup> t	t = 8.3 ms	reapplied	T <sub>J</sub> maximum	370	
Maximum I <sup>2</sup> t for fusing	1-1	t = 10 ms	100 % V <sub>RRM</sub> reapplied		287	
		t = 8.3 ms			262	
Maximum I <sup>2</sup> $\sqrt{t}$ for fusing	l²√t	t = 0.1 ms to 10	ms, no voltage re	applied	4050	kA²√s
Low level value or threshold voltage	V <sub>T(TO)1</sub>	(16.7 % x $\pi$ x $I_{T(A)}$ T <sub>J</sub> = T <sub>J</sub> maximum			0.80	v
High level value of threshold voltage	V <sub>T(TO)2</sub>	$(I > \pi \times I_{T(AV)}), T_J$	= T <sub>J</sub> maximum		1.03	
Low level value on-state slope resistance	r <sub>t1</sub>	(16.7 % x $\pi$ x $I_{T(A)}$ T <sub>J</sub> = T <sub>J</sub> maximum	$A_{V} < I < \pi \times I_{T(AV)},$ n		0.75	
High level value on-state slope resistance	r <sub>t2</sub>	$(I > \pi \times I_{T(AV)}), T_J = T_J$ maximum			0.53	mΩ
Maximum peak on-state or		$I_{TM} = 750 \text{ A}, T_J = 25 \text{ °C}, 180^\circ \text{ conduction},$ average power = $V_{T(TO)} \times I_{T(AV)} + r_t \times (I_{T(RMS)})^2$		duction, t x (I <sub>T(RMS)</sub> ) <sup>2</sup>	1.40	N
forward voltage drop	V <sub>TM,</sub> V <sub>FM,</sub>	$I_{TM} = 750 \text{ A}, T_J = T_J \text{ maximum, } 180^{\circ} \text{ conduction,}$ average power = $V_{T(TO)} \times I_{T(AV)} + r_f \times (I_{T(RMS)})^2$			1.37	V
Maximum holding current	I <sub>H</sub>	Anode supply =	12 V, initial $I_T = 3$	0 A, T <sub>J</sub> = 25 °C	500	
Maximum latching current	١L	Anode supply = <sup>-</sup> gate pulse: 10 V,			1000	mA

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Typical delay time	t <sub>d</sub>	$T_J = 25 \text{ °C}$ , gate current = 1 A dl <sub>q</sub> /dt = 1 A/µs	1.0		
Typical rise time	t <sub>r</sub>	V <sub>d</sub> = 0.67 % V <sub>DRM</sub>	2.0	μs	
Typical turn-off time range	tq	$I_{TM}$ = 300 A; dl/dt = 15 A/μs; T <sub>J</sub> = T <sub>J</sub> maximum; V <sub>R</sub> = 50 V; dV/dt = 20 V/μs; gate 0 V, 100 Ω	200 to 350	F -	

BLOCKING						
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS		
Maximum peak reverse and off-state leakage current	I <sub>RRM,</sub> I <sub>DRM</sub>	$T_J = T_J$ maximum	50	mA		
RMS insulation voltage	V <sub>INS</sub>	50 Hz, circuit to base, all terminals shorted, 25 $^{\circ}\text{C},$ 1 s	3600	V		
Critical rate of rise of off-state voltage	dV/dt	$T_J$ = $T_J$ maximum, exponential to 67 $\%$ rated $V_{\text{DRM}}$	1000	V/µs		

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TRIGGERING						
PARAMETER	SYMBOL	TEST C	CONDITIONS	VALUES	UNITS	
Maximum peak gate power	P <sub>GM</sub>	$t_p \leq 5 \text{ ms},  \text{T}_\text{J} = \text{T}_\text{J} \text{ r}$	naximum	10.0	W	
Maximum average gate power	P <sub>G(AV)</sub>	$f = 50 \text{ Hz}, \text{ T}_{\text{J}} = \text{T}_{\text{J}} \text{ r}$	naximum	2.0	vv	
Maximum peak gate current	+ I <sub>GM</sub>	$t_p \leq 5$ ms, $T_J = T_J$ r	naximum	3.0	А	
Maximum peak negative gate voltage	- V <sub>GT</sub>	$t_p \leq 5 \text{ ms},  T_J = T_J \text{ r}$	naximum	5.0		
		T <sub>J</sub> = - 40 °C	Anode supply = 12 V, resistive load; Ra = 1 $\Omega$ .	4.0	V	
Maximum required DC gate voltage to trigger	V <sub>GT</sub>	T <sub>J</sub> = 25 °C		3.0		
		$T_J = T_J$ maximum		2.0		
		T <sub>J</sub> = - 40 °C	Anode supply = 12 V, resistive load; Ra = 1 $\Omega$	350	mA	
Maximum required DC gate current to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C		200		
		$T_J = T_J$ maximum		100		
Maximum gate voltage that will not trigger	V <sub>GD</sub>	$T_J = T_J$ maximum, rated $V_{DRM}$ applied		0.25	V	
Maximum gate current that will not trigger	I <sub>GD</sub>	$T_J = T_J$ maximum, rated $V_{DRM}$ applied		10.0	mA	
Maximum rate of rise of turned-on current	dl/dt	$T_J = T_J maximum,$ rated $V_{DRM}$ applied		500	A/µs	

THERMAL AND MECHANICAL SPECIFICATIONS						
PARAMETER	1	SYMBOL TEST CONDITIONS		VALUES	UNITS	
Junction operating and storage temperature range		T <sub>J</sub> , T <sub>Stg</sub>		-40 to +130 °C		
	rmal resistance, se per junction	R <sub>thJC</sub>	DC operation 0.125		K/W	
Typical thermal resistance, case to heatsink per module		R <sub>thCS</sub>	Mounting surface flat, smooth and greased	0.02		
Mounting torque	MAGN-A-PAK to heatsink		A mounting compound is recommended and the torque should be rechecked after	4 to 6	Nm	
± 10 %	busbar to MAGN-A-PAK		a period of about 3 hours to allow for the spread of the compound.	4100		
Approximate weight				500	g	
				17.8	oz.	
Case style				MAGN	-A-PAK	

DEVICES	SINUS	SINUSOIDAL CONDUCTION AT T <sub>J</sub> MAXIMUM					RECTANGULAR CONDUCTION AT T <sub>J</sub> MAXIMUM				
DEVICES	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	UNITS
VSKT320-	0.009	0.010	0.013	0.020	0.032	0.007	0.011	0.015	0.020	0.033	K/W

#### Note

Table shows the increment of thermal resistance R<sub>thJC</sub> when devices operate at different conduction angles than DC



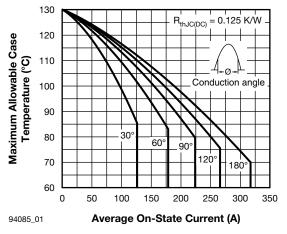


Fig. 1 - Current Ratings Characteristics

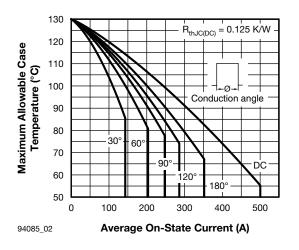


Fig. 2 - Current Ratings Characteristics

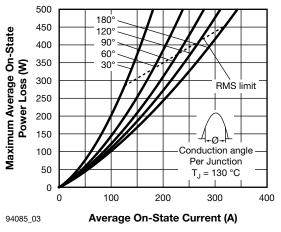


Fig. 3 - On-State Power Loss Characteristics

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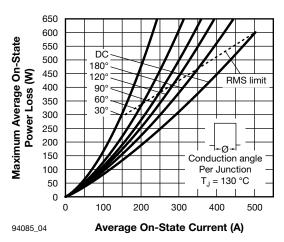
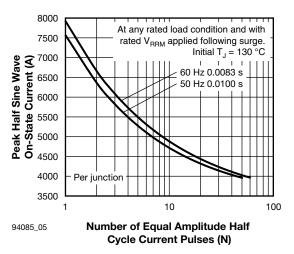
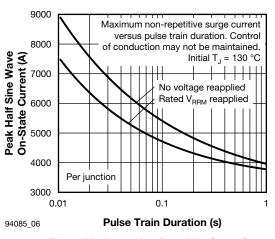


Fig. 4 - On-State Power Loss Characteristics









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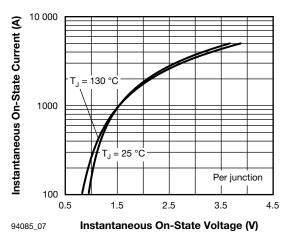
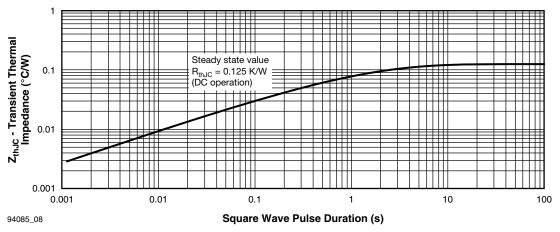


Fig. 7 - On-State Voltage Drop Characteristics





### **ORDERING INFORMATION TABLE**

Device code	vs-	vs	кт	320	-	16	PbF	
	(1	)	2	3	-	4	5	
	1	-	Vishay	Semico	nductors	product		
	2	-	Circuit	configura	ation (see	e dimensi	ons - link	at the end of datasheet)
	3	-	Curren	it rating				
	4	-	Voltage	e code x	100 = V <sub>F</sub>	RRM (see )	Voltage F	Ratings table)
	5	-	<ul> <li>None = standard production</li> <li>PbF = lead (Pb)-free</li> </ul>					

#### Note

To order the optional hardware go to <u>www.vishay.com/doc?95172</u>

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CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	KT	<ul> <li>→</li> <li>→</li></ul>

LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95086			



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