

LTC6955/LTC6955-1
Ultralow Jitter 11 Output
Fanout Buffer

DESCRIPTION

Demonstration Circuit 2611A features the [LTC®6955/LTC6955-1](#), Ultralow Jitter 11 Output Fanout Buffers.

By default, the DC2611A is powered from a single 3.3V supply. An option is provided to power to the DC2611A from dual supplies, allowing for the LTC6955's output supply pins to connect to an LTC Silent Switcher® and the LTC6955 input supply pin to connect to a low noise LDO.

The differential inputs and six of the differential outputs are populated with 0.5" spaced SMA connectors. These outputs are AC-coupled with 50Ω transmission lines

making them suitable to drive 50Ω impedance instruments. The remaining four differential outputs are terminated with 100Ω.

A calibration path is provided to aid in accurate LTC6955 propagation delay measurements. The calibration path can be also reconfigured as a DC path, which allows for a convenient method of locking the LTC6955 outputs to an external PLL/VCO, as shown in Figure 2.

Design files for this circuit board are available.

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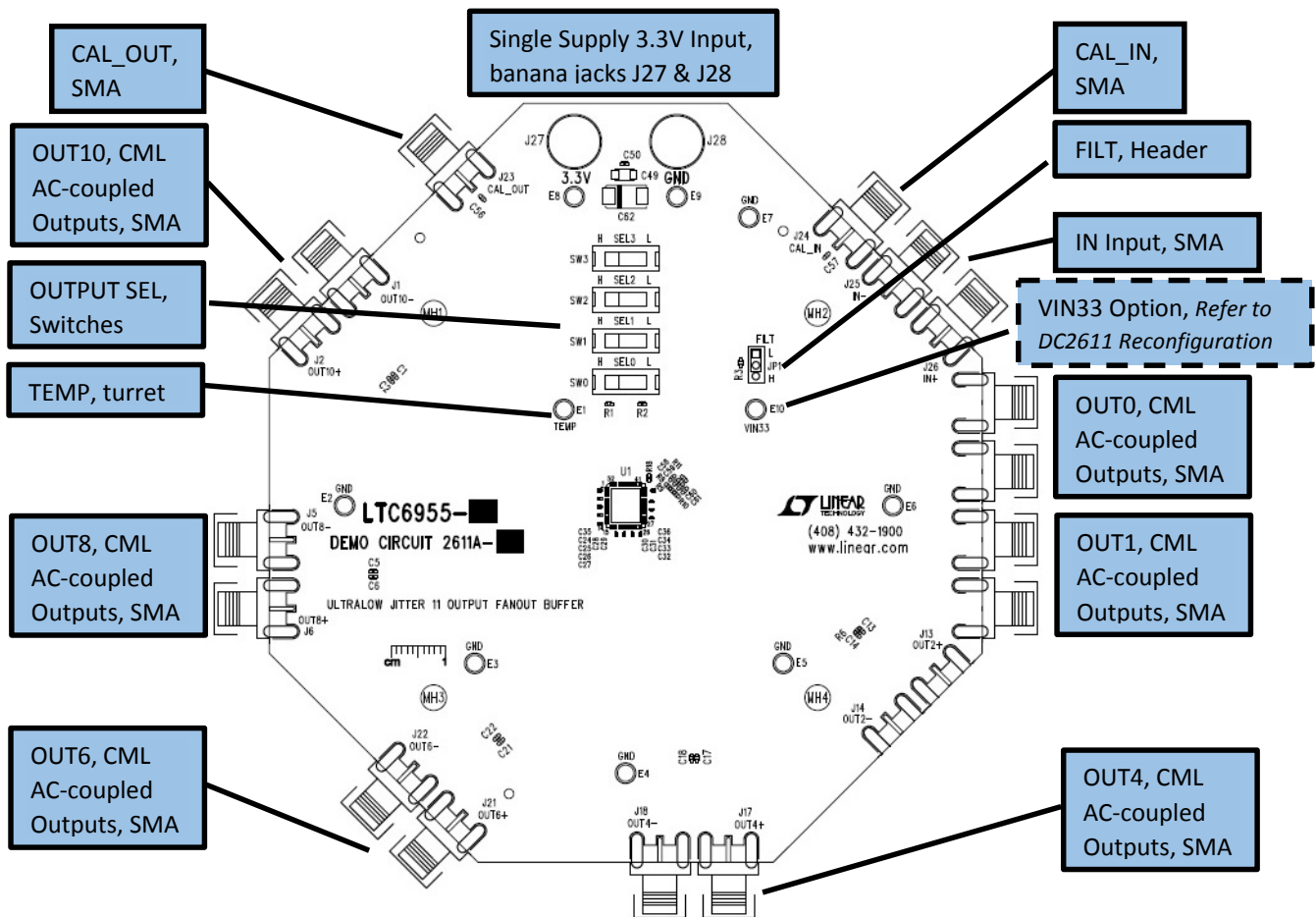


Figure 1. DC2611A Connections

QUICK START PROCEDURE

The DC2611A is easy to set up to evaluate the performance of the LTC6955. Follow the procedure below

DC2611A Configuration

1. Connect J27 and J28 to a power supply and apply power (see Figure 1 and the Typical DC2611A Requirements and Characteristics table).
2. Connect a low phase-noise (or jitter) single-ended signal to IN– (J25). Refer to the LTC6955 data sheet for acceptable input frequencies and amplitudes.
3. Connect desired output (OUT10, OUT8, OUT6, OUT4, OUT1 or OUT0) to a test instrument or other demo board to evaluate performance. Terminate the unused outputs with 50Ω.
4. Ensure SW0:3 are configured to enable the desired output. Setting SEL[3:1]=H and SEL0=L enables all outputs. Refer to Table 1 for a list of SEL[3:0] settings vs output states.

Be sure to power down or terminate any unused RF output with 50Ω, or poor spurious performance may result.

Troubleshooting

If the LTC6955 does not output a signal

1. Ensure LTC6955 input signal is connected to the LTC6955 IN– pin, not the LTC6955 IN+ pin.

If DC2611A performance is less than the LTC6955 data sheet specifications:

1. For unexpected spurious response, verify power supplies are low noise and spurious free power supplies. Power supplies that are based off a switching regulator architecture are known to generate spurs on low jitter clock outputs.
2. For poor phase noise results, verify the phase noise specifications of the input signal and the phase noise measurement instrument. Traditional signal sources and spectrum analyzers have higher phase noise than the LTC6955 and will degrade measurement results. To measure phase noise performance it is recommended to use a low jitter oscillator and a signal source analyzer, such as Keysight’s (previously Agilent/HP) E5052.
3. Contact the factory for further troubleshooting.

Table 1. LTC6955 SEL[3:0] Settings vs Output States

SEL[3:0]	TEMP DIODE	OUT10	OUT9	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
0x0		Pwrnd										
0x1	ON	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd	Pwrnd	Pwrnd	Pwrnd	Pwrnd
0x2	ON	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd	Pwrnd	Pwrnd
0x3	ON	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd
0x4	ON	ON	ON	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd
0x5	ON	ON	Inverted	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd
0x6	ON	ON	ON	ON	ON	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd
0x7	ON	ON	Inverted	ON	Inverted	ON	Pwrnd	ON	Pwrnd	ON	Pwrnd	Pwrnd
0x8	ON	ON	ON	ON	ON	ON	ON	ON	Pwrnd	ON	Pwrnd	Pwrnd
0x9	ON	ON	Inverted	ON	Inverted	ON	Inverted	ON	Pwrnd	ON	Pwrnd	Pwrnd
0xA	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Pwrnd	Pwrnd
0xB	ON	ON	Inverted	ON	Inverted	ON	Inverted	ON	Inverted	ON	Inverted	Pwrnd
0xC	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	Pwrnd
0xD	ON	ON	Inverted	ON	Inverted	ON	Inverted	ON	Inverted	ON	Inverted	ON
0xE	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON	ON
0xF	ON	Pwrnd										

DC2611A RECONFIGURATION

The following covers the hardware reconfiguration of the DC2611A. Refer to LTC6955 data sheet for a better understanding of device specific considerations.

Power Supply Options

Table 2 provides the power supply options for DC2611A. By default the DC2611A is setup to use the single supply option. However, a dual supply option is available to power the higher current supply from our Silent Switcher, such as the LT8609S. The Silent Switcher improves the power efficiency over the low noise LDO. A spurious free supply, such as a low noise LDO, is required on the LTC6955's V_{IN}^+ supply pin.

Table 2. Power Supply Options

			Power Supply Voltage/Current (Recommended Supply)	
DEFAULT	OPTION	R18	J27 (3.3V)	E10 (VIN33)
x	Single Supply	Installed	3.3V/750mA (Low Noise LDO)	NA
	Dual Supply	Do Not Install	3.3V/750mA (Silent Switcher)	3.3V/150mA (Low Noise LDO)

Input Termination Options

Table 3 provides the single-ended and differential input termination options. By default the DC2611A is setup for a single-ended input on the IN- SMA (J25). For best performance different termination networks are provided for input signals <5GHz and input signals >5GHz.

LTC6955-1 Divide by Two Coupling Spur

To help reduce the LTC6955-1's OUT10 /2 coupling spur to other outputs a ferrite bead (FB1) should be installed on the OUT10 supply pin, VOUT+ (Pin 5). For the LTC6955 FB1 should be a 0Ω resistor.

Table 3. Input Termination Options (*)

DEFAULT	TERMINATION	R8 (Ω)	R9 (Ω)	R10 (Ω)	R11 (Ω)	R19 (Ω)	R20 (Ω)	C58	C59	C60	C61
DC2611A-A	SE, IN-, <5GHz	75	DNI	30	DNI	DNI	DNI	0.1uF	0.1uF	DNI	0.1uF
DC2611A-B	SE, IN-, ≥5GHz	DNI	DNI	DNI	1nH	DNI	49.9	DNI	1pF	1pF	DNI
	SE, IN+, <5GHz	30	DNI	75	DNI	DNI	DNI	0.1uF	DNI	0.1uF	0.1uF
	SE, IN+, ≥5GHz	DNI	DNI	DNI	1nH	49.9	DNI	DNI	1pF	1pF	DNI
	DIFF, CML or PECL, <5GHz	DNI	160	DNI	DNI	DNI	DNI	DNI	0.1uF	0.1uF	DNI
	DIFF, CML or PECL, ≥5GHz	DNI	DNI	DNI	1nH	DNI	DNI	DNI	1pF	1pF	DNI
	DIFF, LVDS	DNI	DNI	DNI	160	DNI	DNI	DNI	0.1uF	0.1uF	DNI

*SE = Single-Ended, DIFF = Differential, DNI = Do Not Install

CML Outputs, OUT[10:0]

The DC2611A has 11 CML outputs. Six of these outputs are AC-coupled and brought out to SMAs (OUT10, OUT8, OUT6, OUT4, OUT1 or OUT0). To drive 50Ω impedance instruments connect OUTx+ to the instrument and OUTx- to a 50Ω termination, or vice versa.

The remaining five outputs (OUT9, OUT7, OUT5, OUT3, and OUT2) are terminated with a 100Ω resistor on board. To connect these outputs to a 50Ω instrument, remove the 100Ω termination, and install the appropriate SMAs and AC blocking capacitors.

Refer to LTC6955 data sheet for differential termination options.

Alternate Configuration Options

To take advantage of the LTC6955's maximum output frequency and ultralow output additive phase noise, the DC2611A (LTC6955, LTC6955-1), the DC2609A (LTC6952) and the VCO rider board (DC2664A) were designed to mate directly together, as shown in Figure 2. This setup allows for options to lock the LTC6952 reference input to:

- A) A <7.5GHz VCO and LTC6955-1 output frequency, by utilizing the LTC6955-1 divide by two output on OUT10 to drive the LTC6952 VCO input. (refer to Figure 2)
- B) Any VCO and create lower jitter clocks from a LTC6955 or LTC6955-1 output than a standalone LTC6952 produces.

Refer to the LTC6952 and LTC6955 data sheet's typical application for measured results. Refer to the DC2664A demo manual for recommendation on loop filter component placement.

DC2611A RECONFIGURATION

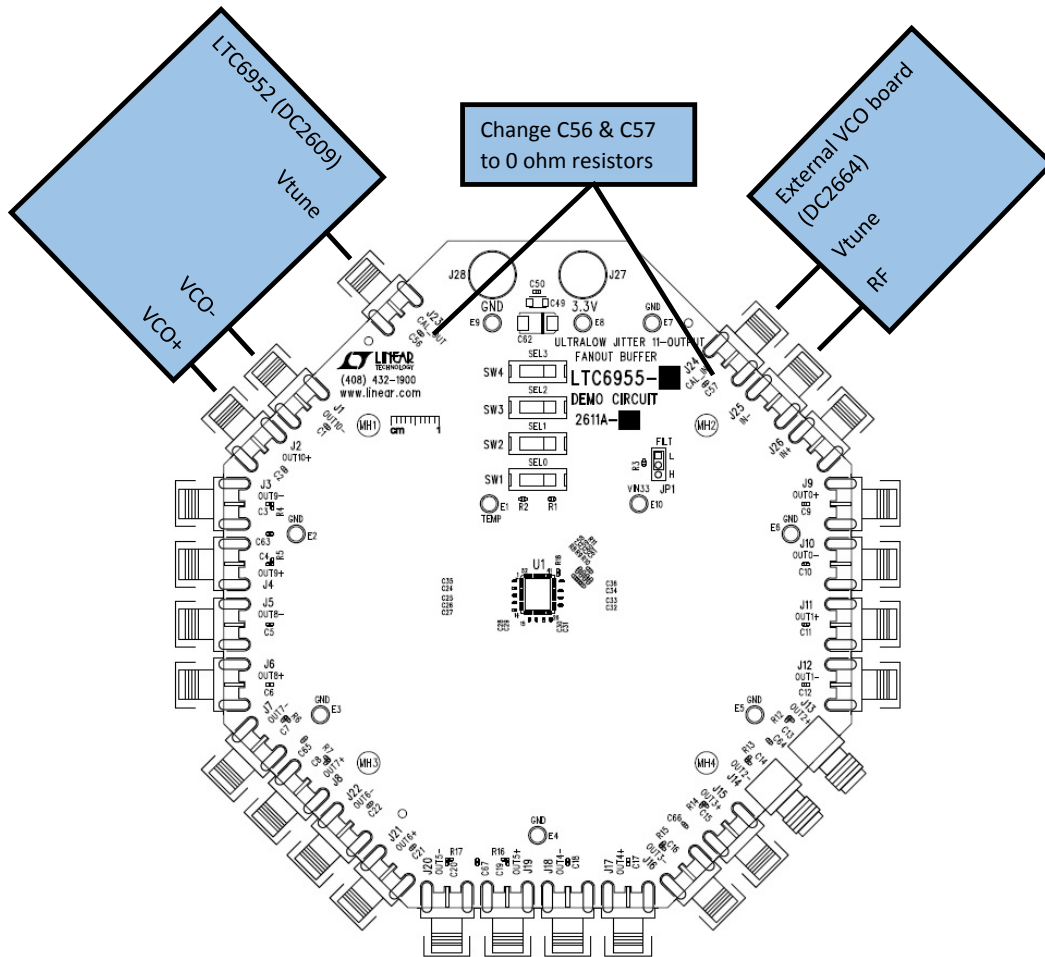
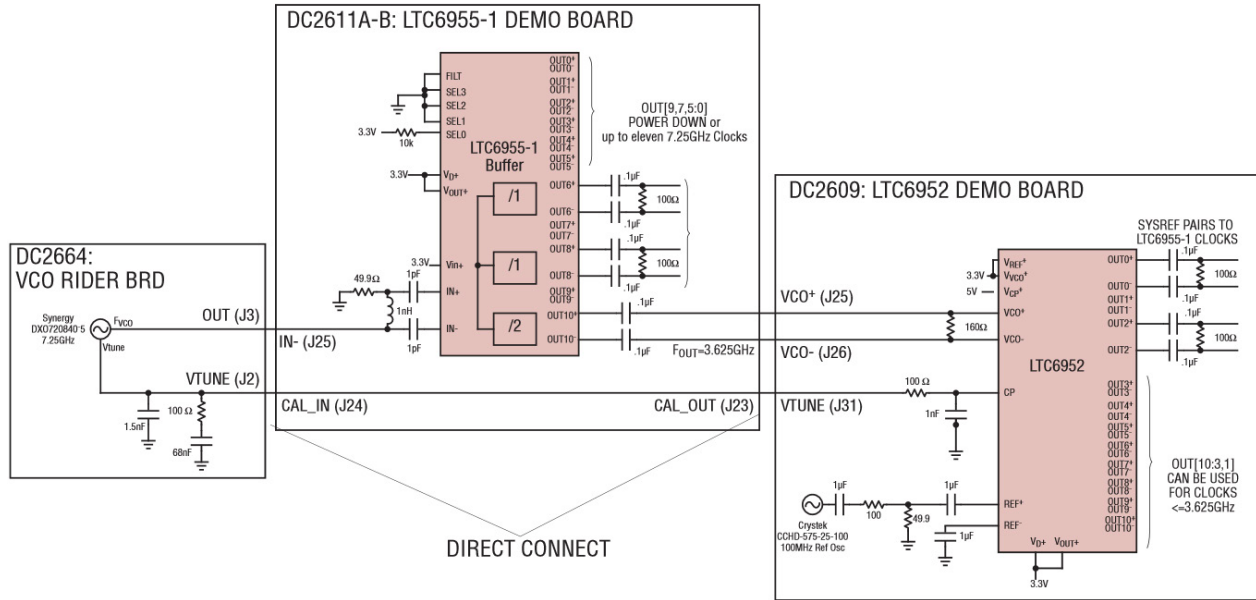


Figure 2. Alternate Configuration, Locking LTC6955 Outputs to an External PLL/VCO

TYPICAL DC2611A REQUIREMENTS AND CHARACTERISTICS

Table 4.

PARAMETER	INPUT OR OUTPUT	PHYSICAL LOCATION	DETAILS
3.3V Power Supply	Input	J27 and J28 BNC Banana Jacks	If R18 populated, default option , single supply: 3.3V low-noise and spur-free supply, 1A; If R18 depopulated , dual supply option, allows for experiments with more efficient power supply evaluation (Silent Switcher). See 3.3V power supply #2 (VIN33)
3.3V Power Supply #2 (VIN33)	Input	E10 Turret (VIN33)	If R18 depopulated, dual supply option , 3.3v low-noise and spur-free supply, 150mA;
OUT10+; OUT10-	Two Outputs	J1 and J2 SMA Connectors*	CML, AC-coupled, 800mV _{P-P} differential
OUT8+; OUT8-		J5 and J6 SMA Connectors*	
OUT6+; OUT6-		J21 and J22 SMA Connectors*	
OUT4+; OUT4-		J17 and J18 SMA Connectors*	
OUT1+; OUT1-		J11 and J12 SMA Connectors*	
OUT0+; OUT0-		J9 and J10 SMA Connectors*	
OUT9+; OUT9-	Two Outputs (Not Connected)	J3 and J4 (SMA Not Populated)	On board differential 100Ω termination
OUT7+; OUT7-		J7 and J8 (SMA Not Populated)	
OUT5+; OUT5-		J19 and J20 (SMA Not Populated)	
OUT3+; OUT3-		J15 and J16 (SMA Not Populated)	
OUT2+; OUT2-		J13 and J14 (SMA Not Populated)	
IN+	Input (Not Connected)	J26 SMA Connector	Default: Not connected (see Table 3, for correct input termination options)
IN-	Input	J25 SMA Connector	Default: Preferred single-ended input (see Table 3, for correct input termination options)
FILT	Input, Center Pin	JP1 3-Pin Header	L(Default): FILT disabled, set by pull-down resistor H: FILT enabled
TEMP	Output	E1 Turret (TEMP)	Internal temperature diode

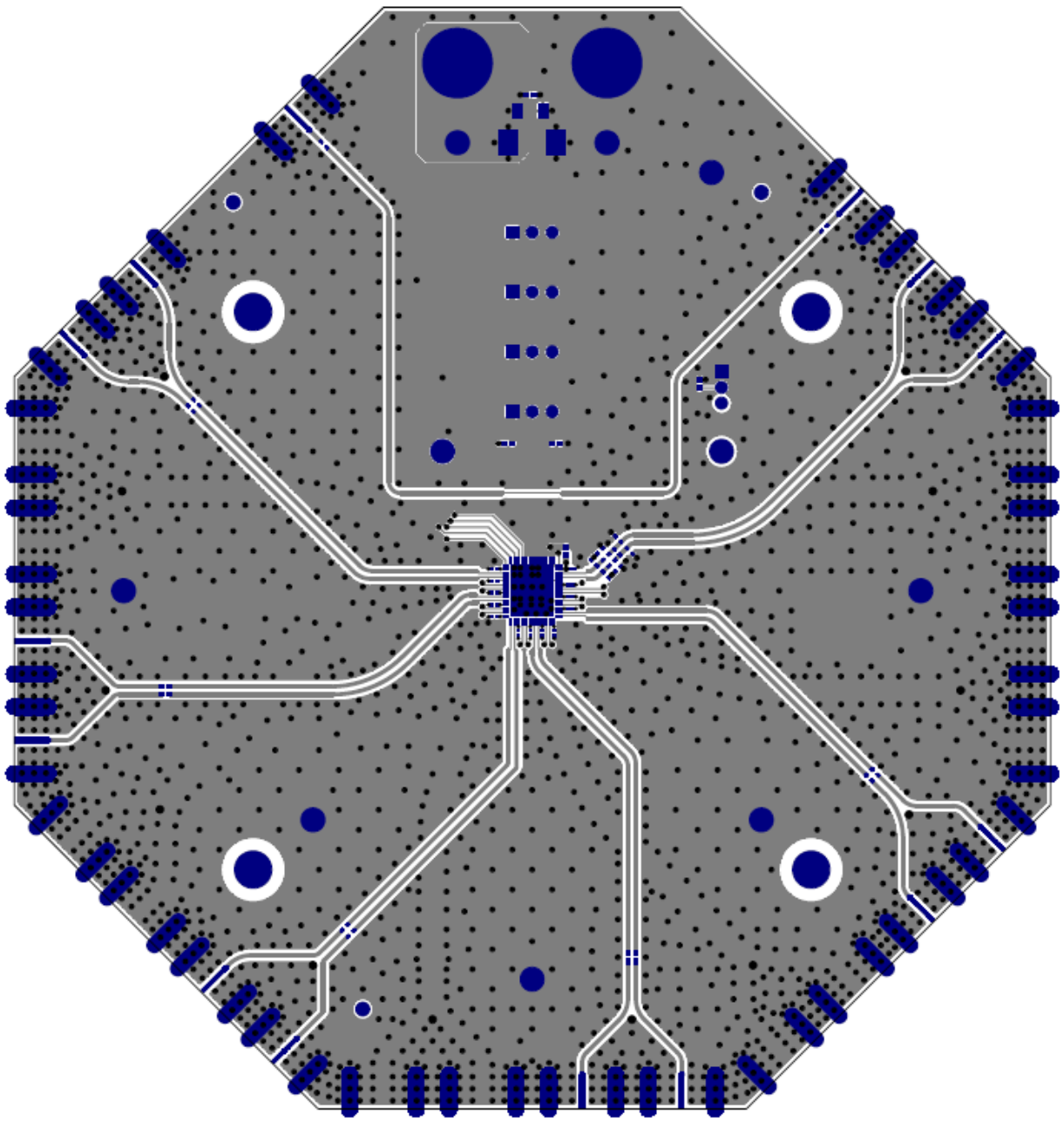
*Any unused RF output **must** be powered down or terminated with 50Ω, or poor spurious performance may result.

ASSEMBLY OPTIONS

Table 5. DC2611A Assembly Options

ASSEMBLY VERSION	U1 PART NUMBER
DC2611A-A	LTC6955IUKG
DC2611A-B	LTC6955IUKG-1

PCB LAYOUT



Top Layer

PARTS LIST

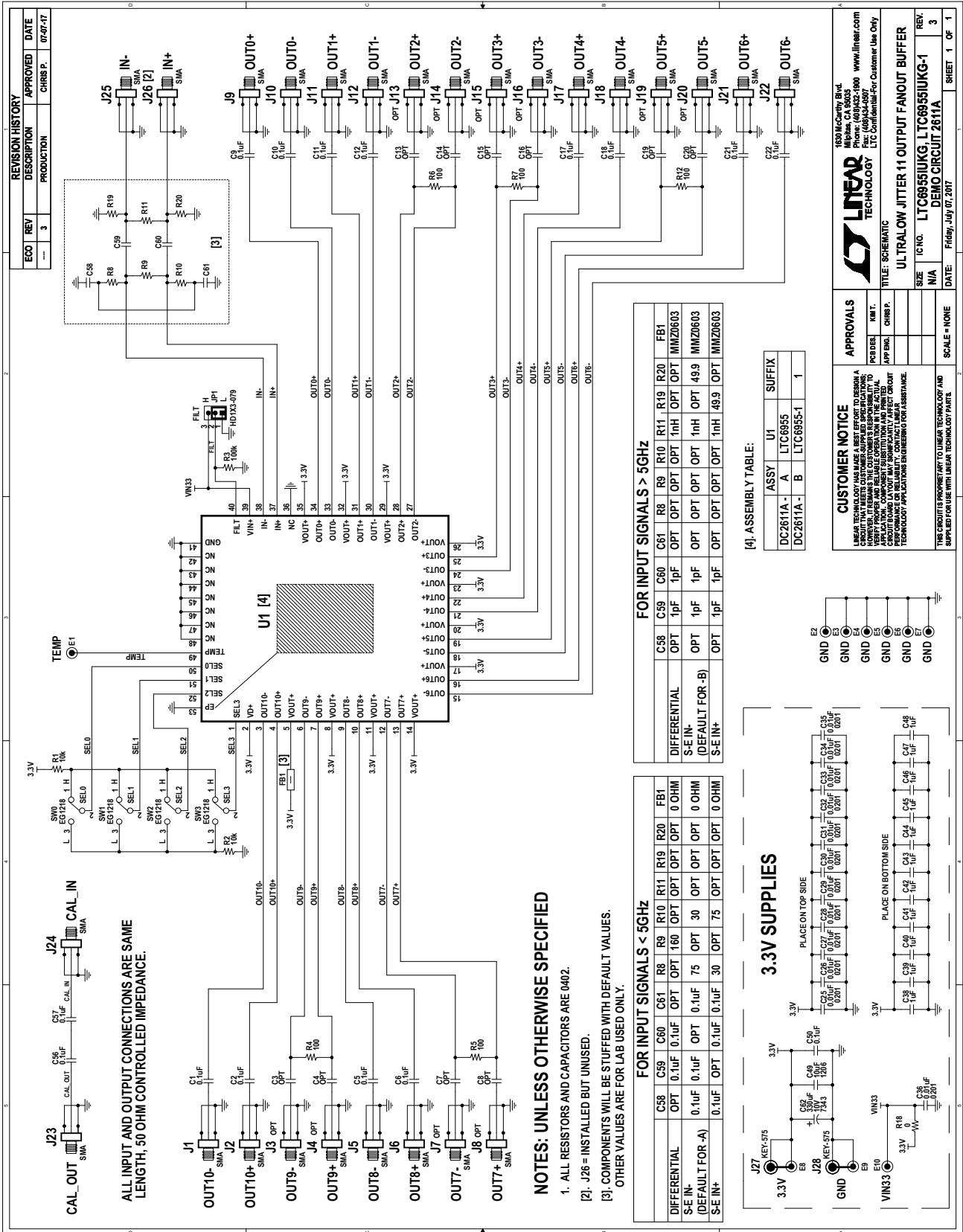
ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	15	C1, C2, C5, C6, C9-C12, C17, C18, C21, C22, C50, C56, C57	CAP, X7R, 0.1 μ F, 10V, 10%, 0402	MURATA, GRM155R71A104KA01D
2	0	C3, C4, C7, C8, C13-C16, C19, C20	CAP, 0402	OPT
3	12	C25-C36	CAP, X7R, 0.01 μ F, 6.3V, 10%, 0201	MURATA, GRM033R70J103KA01D
4	11	C38-C48	CAP, X5R, 1 μ F, 16V, 10%, 0402	MURATA, GRM155R61C105KE01D
5	1	C49	CAP, X7R, 10 μ F, 25V, 10%, 1206	MURATA, GRM31CR71E106KA12L
6	1	C62	CAP, TANT, 330 μ F, 10V, 10%, 7343	AVX, TPME337K010R0035
7	10	E1-E10	TURRET, TESTPOINT 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
8	1	JP1	CONN., HEADER, MALE, 1X3, 2mm, THT	WURTH ELEKTRONIK, 62000311121
9	16	J1, J2, J5, J6, J9-J12, J17, J18, J21-J26	CONN., SMA 50 Ω EDGE-LAUNCH, CON-SMA-R	CCSJ, 142-0701-851
10	0	J3, J4, J7, J8, J13-J16, J19, J20	CONN., SMA 50 Ω EDGE-LAUNCH, CON-SMA-R	OPT
11	2	J27, J28	CONN, JACK, BANANA	KEYSTONE, 575-4
12	2	R1, R2	RES., CHIP, 10k, 1/10W, 1% 0402	VISHAY, CRCW040210K0FKED
13	1	R3	RES., CHIP, 100k, 1/10W, 1% 0402	VISHAY, CRCW0402100KFKED
14	5	R4, R5, R6, R7, R12	RES., CHIP, 100 Ω , 1/16W, 1% 0402	VISHAY, CRCW0402100RFKED
15	1	R18	RES., CHIP, 0 Ω , 1/10W, 0402	VISHAY, CRCW04020000Z0ED
16	4	SW0, SW1, SW2, SW3	SWITCH, SLIDE SPDT 200MA 30V, SW-EG1218	E-SWITCH, EG1218
17	1	SHUNT ON JP1 (1&2)	SHUNT, 2mm	WURTH ELEKTRONIK, 60800213421
18	4	MH1-MH4	STANDOFF, NYLON, 0.5, 1/2"	WURTH ELEKTRONIK, 702935000
19	1	DUST CAP FOR J26	WYHP DUST CAP FOR SMA FEMALE RF CONN	AMAZON

DEMO MANUAL DC2611A

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC2611A3-A Required Circuit Components				
1	1		DC2611A3-GENERAL BOM	
2	3	C58, C59, C61	CAP, X7R, 0.1 μ F, 10V, 10%, 0402	MURATA, GRM155R71A104KA01D
3	0	C60	CAP, 0402	OPT
4	1	FB1	RES., CHIP, 0 Ω , 1/20W, 1% 0201	VISHAY, CRCW02010000Z0ED
5	1	R8	RES., CHIP, 75 Ω , 1/16W, 1% 0402	VISHAY, CRCW040275R0FKED
6	0	R9, R11, R19, R20	RES., 0402	OPT
7	1	R10	RES., CHIP, 30 Ω , 1/16W, 1% 0402	VISHAY, CRCW040230R0FKED
8	1	U1	I.C., ULTRALOW JITTER 11 OUTPUT FANOUT BUFFER, QFN52UKG-7X8	LINEAR TECH., LTC6955IUKG
DC2611A3-B Required Circuit Components				
1	1		DC2611A3-GENERAL BOM	
2	0	C58, C61	CAP, 0402	OPT
3	2	C59, C60	CAP, C0G, 1pF, 50V, 10%, 0402	MURATA, GJM1555C1H1R0CB01
4	1	FB1	IND., 47 Ω S AT 100MHz, FERRITE BEAD, 0201	TDK, MMZ0603D470ET000
5	0	R8, R9, R10, R19	RES., 0402	OPT
6	1	R11	IND., FIXED, HIFREQ, 47nH 5% 0.15A, 0402	COIL CRAFT, 0402CS-1NOXJL
7	1	R20	RES., CHIP, 49.9, 1/16W, 1% 0402	VISHAY, CRCW040249R9FKED
8	1	U1	I.C., ULTRALOW JITTER 11 OUTPUT FANOUT BUFFER, QFN52UKG-7X8	LINEAR TECH., LTC6955IUKG-1

SCHEMATIC DIAGRAM





ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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