19-3285; Rev 1; 5/05

EVALUATION KITS AVAILABLE

High-Side Power and Current Monitors

MAX4210/MAX4211

General Description

The MAX4210/MAX4211 low-cost, low-power, high-side power/current monitors provide an analog output voltage proportional to the power consumed by a load by multiplying load current and source voltage. The MAX4210/MAX4211 measure load current by using a high-side current-sense amplifier, making them especially useful in battery-powered systems by not interfering with the ground path of the load.

The MAX4210 is a small, simple 6-pin power monitor intended for limited board space applications. The MAX4210A/B/C integrate an internal 25:1 resistor-divider network to reduce component count. The MAX4210D/E/F use an external resistor-divider network for greater design flexibility.

The MAX4211 is a full-featured current and power monitor. The device combines a high-side current-sense amplifier, 1.21V bandgap reference, and two comparators with open-drain outputs to make detector circuits for overpower, overcurrent, and/or overvoltage conditions. The open-drain outputs can be connected to potentials as high as 28V, suitable for driving high-side switches for circuit-breaker applications.

Both the MAX4210/MAX4211 feature three different current-sense amplifier gain options: 16.67V/V, 25.00V/V, and 40.96V/V. The MAX4210 is available in 3mm x 3mm, 6-pin TDFN and 8-pin µMAX® packages and the MAX4211 is available in 4mm x 4mm, 16-pin thin QFN and 16-pin TSSOP packages. Both parts are specified for the -40°C to +85°C extended operating temperature range.

Applications

- Overpower Circuit Breakers
- Smart Battery Packs/Chargers
- Smart Peripheral Control
- Short-Circuit Protection
- Power-Supply Displays
- Measurement Instrumentation
- Baseband Analog Multipliers
- VGA Circuits
- Power-Level Detectors

Pin Configurations and Selector Guide appear at end of data sheet.

Features

- ♦ **Real-Time Current and Power Monitoring**
- ♦ **±1.5% (max) Current-Sense Accuracy**
- ♦ **±1.5% (max) Power-Sense Accuracy**
- ♦ **Two Uncommitted Comparators (MAX4211)**
- ♦ **1.21V Reference Output (MAX4211)**
- ♦ **Three Current/Power Gain Options**
- ♦ **100mV/150mV Current-Sense Full-Scale Voltage**
- ♦ **+4V to +28V Input Source Voltage Range**
- ♦ **+2.7V to +5.5V Power-Supply Voltage Range**
- ♦ **Low Supply Current: 380µA (MAX4210)**
- ♦ **220kHz Bandwidth**
- ♦ **Small 6-Pin TDFN and 8-Pin µMAX Packages (MAX4210)**

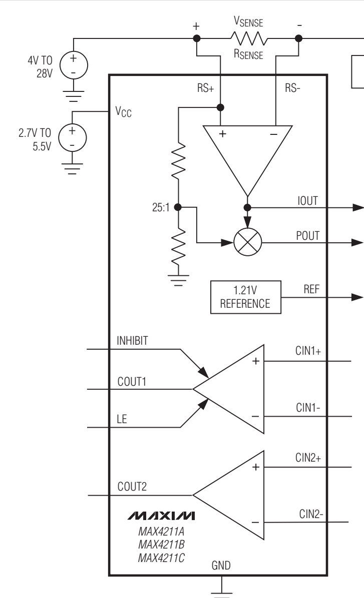
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4210AETT-T	-40°C to +85°C	6 TDFN-6-EP* (3mm x 3mm)	AHF
MAX4210AEUA	-40°C to +85°C	8 µMAX	—

**EP = Exposed paddle.*

Ordering Information continued at end of data sheet.

Functional Diagrams



Functional Diagrams continued at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN, CIN1, CIN2 to GND ....-0.3V to +6V
RS+, RS-, INHIBIT, LE, COUT1, COUT2 to GND ...-0.3V to +30V
IOUT, POUT, REF to GND ....-0.3V to (V_{CC} + 0.3V)
Differential Input Voltage (V_{RS+} - V_{RS-}) ....±5V
Maximum Current into Any Pin...±10mA
Output Short-Circuit Duration to V_{CC} or GND 10s
Continuous Power Dissipation (T_A = +70°C)
6-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 754mW
16-Pin Thin QFN (derate 25mW/°C above +70°C) 2000mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range (Note 2)	V_{CC}			2.7		5.5	V
Common-Mode Input Range (Note 3)	V_{CMR}	Measured at RS+		4		28	V
Supply Current	I_{CC}	T_A = +25°C, V_{CC} = +5.5V	MAX4210		380	570	µA
			MAX4211		670	960	
		V_{CC} = +5.5V	MAX4210			670	
			MAX4211			1100	
Input Bias Current	I_{RS+}	V_{SENSE} = 0mV	MAX421_A/B/C		14	25	µA
			MAX421_D/E/F		3	8	
	I_{RS-}	V_{SENSE} = 0mV			3	8	
IN Input Bias Current	I_{IN}	MAX421_D/E/F			-0.1	-1	µA
Leakage Current	I_{RS+}, I_{RS-}	V_{CC} = 0V			0.1	1	µA
V_{SENSE} Full-Scale Voltage (Note 4)	V_{SENSE_FS}	MAX421_A/B/D/E		150			mV
		MAX421_C/F		100			
IN Full-Scale Voltage (Note 4)	V_{IN_FS}	MAX421_D/E/F, V_{SENSE} = 10mV to 100mV		1			V
IN Input Voltage Range (Note 5)	V_{IN}	MAX421_D/E/F, V_{SENSE} = 10mV to 100mV		0.16		1.10	V
V_{RS+} Full-Scale Voltage (Note 4)		MAX421_A/B/C, V_{SENSE} = 10mV to 100mV		25			V
V_{RS+} Input Voltage Range (Note 5)	V_{RS+}	MAX421_A/B/C, V_{SENSE} = 10mV to 100mV		4		28	V
Minimum IOUT/POUT Voltage	V_{OUT_MIN}	V_{SENSE} = 0V, V_{RS+} = 25V	Current into IOUT = 10µA		1.5		mV
			Current into IOUT = 100µA		2.5	80	
			Current into POUT = 10µA		1.5		
			Current into POUT = 100µA		2.5	80	
Maximum IOUT/POUT Voltage (Note 6)	V_{OUT_MAX}	V_{SENSE} = 300mV, V_{RS+} = 25V	Current out of IOUT = 500µA			V_{CC} - 0.25	V
			Current out of POUT = 500µA			V_{CC} - 0.25	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Sense Amplifier Gain	V_{IOUT}/ V_{SENSE}	MAX4211A/D			16.67		V/V
		MAX4211B/E			25.00		
		MAX4211C/F			40.96		
Power-Sense Amplifier Gain	V_{POUT}/ (V_{SENSE} x V_{RS+})	MAX421_A			0.667		1/V
		MAX421_B			1.00		
		MAX421_C			1.64		
	V_{POUT}/ (V_{SENSE} x V_{IN})	MAX421_D			16.67		
		MAX421_E			25.00		
		MAX421_F			40.96		
IOUT Common-Mode Rejection	CMRI	MAX4211, V_{RS+} = 4V to 28V		60	80		dB
POUT Common-Mode Rejection	CMRP	MAX421_D/E/F, V_{RS+} = 4V to 28V		60	80		dB
IOUT Power-Supply Rejection	PSRI	V_{CC} = 2.7V to 5.5V		52	80		dB
POUT Power-Supply Rejection	PSRP	V_{CC} = 2.7V to 5.5V		52	70		dB
Output Resistance for POUT, IOUT, REF	R_{OUT}				0.5		Ω
IOUT -3dB Bandwidth	$BW_{IOUT/SENSE}$	V_{SENSE} = 100mV, V_{SENSE} AC source			220		kHz
POUT -3dB Bandwidth	$BW_{POUT/SENSE}$	V_{SENSE} = 100mV, V_{SENSE} AC source			220		kHz
	$BW_{POUT/VIN}$	V_{SENSE} = 100mV, V_{IN} AC source, MAX421_D/E/F			500		
	$BW_{POUT/RS+}$	V_{SENSE} = 100mV, V_{RS+} AC source, MAX421_A/B/C			250		
Capacitive-Load Stability (POUT, IOUT, REF)	C_{LOAD}	No sustained oscillations			450		pF
Current Output (IOUT) Settling Time to 1% of Final Value		MAX4211	V_{SENSE} = 10mV to 100mV		15		μs
			V_{SENSE} = 100mV to 10mV		15		
Power Output (POUT) Settling Time to 1% of Final Value		MAX421_A/B/C	V_{SENSE} = 10mV to 100mV		10		μs
			V_{SENSE} = 100mV to 10mV		10		
			V_{RS+} = 4V to 25V, V_{SENSE} = 100mV		15		
			V_{RS+} = 25V to 4V, V_{SENSE} = 100mV		15		
		MAX421_D/E/F	V_{SENSE} = 10mV to 100mV		10		
			V_{SENSE} = 100mV to 10mV		10		
			V_{IN} = 160mV to 1V, V_{SENSE} = 100mV		10		
			V_{IN} = 1V to 160mV, V_{SENSE} = 100mV		10		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Up Time to 1% of Current Output Final Value		V_{SENSE} = 100mV, C_{LOAD} = 10pF, MAX4211		100		µs
Power-Up Time to 1% of Power Output Final Value		V_{SENSE} = 100mV, C_{LOAD} = 10pF		100		µs
Saturation Recovery Time for Current Out (Note 7)		C_{LOAD} = 10pF, V_{SENSE} = -100mV to +100mV		35		µs
		C_{LOAD} = 10pF, V_{SENSE} = 1.5V to 100mV		35		
Saturation Recovery Time for Power Out (Note 7)		V_{CC} = 5V, V_{RS+} = 10V, C_{LOAD} = 10pF, V_{SENSE} = -100mV to +100mV		25		µs
		V_{CC} = 5V, V_{RS+} = 10V, C_{LOAD} = 10pF, V_{SENSE} = 1.5V to 100mV		25		
Reference Voltage	V_{REF}	I_{REF} = 0 to 100µA, T_A = +25°C	1.20	1.21	1.22	V
		I_{REF} = 0 to 100µA, T_A = -40°C to +85°C	1.19		1.23	
Comparator Input Offset		Common-mode voltage = REF		±0.5	±5	mV
Comparator Hysteresis				5		mV
Comparator Common-Mode Low		Functional test		0.1		V
Comparator Common-Mode High		Functional test		V_{CC} - 1.15		V
Comparator Input Bias Current	I_{BIAS}			-2		nA
Comparator Output Low Voltage	V_{OL}	I_{SINK} = 1mA		0.2	0.6	V
Comparator Output-High Leakage Current (Note 8)		V_{PULLUP} = 28V			1	µA
LE Logic Input-High Voltage Threshold	V_{IH}		0.67 x V_{CC}			V
LE Logic Input-Low Voltage Threshold	V_{IL}				0.33 x V_{CC}	V
LE Logic Input Internal Pulldown Current			0.68	1	2.20	µA
INHIBIT Logic Input-High Voltage Threshold			1.3			V
INHIBIT Logic Input-Low Voltage Threshold					0.5	V
INHIBIT Logic Input Hysteresis				0.6		V
INHIBIT Logic Input Internal Pulldown Current			0.68	1	2.20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Comparator Propagation Delay	t_{PD+}, t_{PD-}	C_{LOAD} = 10pF, R_{LOAD} = 10kΩ pullup to V_{CC}, 5mV overdrive			4		µs
Minimum INHIBIT Pulse Width					1		µs
Minimum LE Pulse Width					1		µs
Comparator Power-Up Blanking Time From V_{CC}	t_{ON}	V_{CC} from 0 to (2.7V to 5.5V)			300		µs
LATCH Setup Time	t_{SETUP}				3		µs
MAX4210A/MAX4211A (power gain = 0.667)							
POUT Gain Accuracy (Note 9)	ΔV_{POUT}/ ΔV_{SENSE}	V_{SENSE} = 10mV to 100mV, V_{RS+} = 25V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT}/ ΔV_{RS+}	V_{SENSE} = 100mV, V_{RS+} = 5V to 25V	T_A = +25°C		±0.5	±1.5	
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total POUT Output Error (Note 10)	ΔV_{POUT_MAX}/ FSO	V_{SENSE} = 5mV to 100mV, V_{RS+} = 5V to 25V	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT_MAX}/ V_{POUT}	V_{SENSE} = 150mV, V_{RS+} ≥ 15V	T_A = +25°C		±0.2	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 100mV, V_{RS+} ≥ 4V			±2.5		
		V_{SENSE} = 100mV, V_{RS+} ≥ 9V			±1.2		
		V_{SENSE} = 50mV, V_{RS+} ≥ 6V			±1.8		
		V_{SENSE} = 25mV, V_{RS+} ≥ 15V			±1.8		
POUT Output Offset Voltage (Note 11)		V_{SENSE} = 0V, V_{RS+} = 25V	T_A = +25°C		1.5	5	mV
			T_A = T_{MIN} to T_{MAX}			15	
MAX4210B/MAX4211B (power gain = 1.00)							
POUT Gain Accuracy (Note 9)	ΔV_{POUT}/ ΔV_{SENSE}	V_{SENSE} = 10mV to 100mV, V_{RS+} = 25V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT}/ ΔV_{RS+}	V_{SENSE} = 100mV, V_{RS+} = 5V to 25V	T_A = +25°C		±0.5	±1.5	
			T_A = T_{MIN} to T_{MAX}			±3.0	

**FSO refers to full-scale output under the conditions: V_{SENSE} = 100mV, V_{RS+} = +25V, or V_{IN} = 1V.*

High-Side Power and Current Monitors

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total POUT Output Error (Note 10)	ΔV_{POUT_MAX}/ FSO	V_{SENSE} = 5mV to 100mV, V_{RS+} = 5V to 25V	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT_MAX}/ V_{POUT}	V_{SENSE} = 150mV, V_{RS+} > 15V	T_A = +25°C		±0.2	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 100mV, V_{RS+} > 4V			±2.5		
		V_{SENSE} = 100mV, V_{RS+} > 9V			±1.2		
		V_{SENSE} = 50mV, V_{RS+} > 6V			±1.8		
		V_{SENSE} = 25mV, V_{RS+} > 15V			±1.8		
POUT Output Offset Voltage (Note 11)		V_{SENSE} = 0V, V_{RS+} = 25V	T_A = +25°C		2	6.5	mV
			T_A = T_{MIN} to T_{MAX}			20	
MAX4210C/MAX4211C (power gain = 1.64)							
POUT Gain Accuracy (Note 9)	ΔV_{POUT}/ ΔV_{SENSE}	V_{SENSE} = 10mV to 100mV, V_{RS+} = 25V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT}/ ΔV_{RS+}	V_{SENSE} = 100mV, V_{RS+} = 5V to 25V	T_A = +25°C		±0.5	±1.5	
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total POUT Output Error (Note 10)	ΔV_{POUT_MAX}/ FSO	V_{SENSE} = 5mV to 100mV, V_{RS+} = 5V to 25V	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT_MAX}/ V_{POUT}	V_{SENSE} = 100mV, V_{RS+} ≥ 4V			±2.5		%
		V_{SENSE} = 100mV, V_{RS+} ≥ 9V			±1.2		
		V_{SENSE} = 50mV, V_{RS+} ≥ 6V			±1.8		
		V_{SENSE} = 25mV, V_{RS+} ≥ 15V			±1.8		
POUT Output Offset Voltage (Note 11)		V_{SENSE} = 0V, V_{RS+} = 25V	T_A = +25°C		3	10	mV
			T_A = T_{MIN} to T_{MAX}			30	
MAX4210D/MAX4211D (power gain = 16.67)							
POUT Gain Accuracy (Note 9)	ΔV_{POUT}/ ΔV_{SENSE}	V_{SENSE} = 10mV to 100mV, V_{IN} = 1V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT}/ ΔV_{IN}	V_{SENSE} = 100mV, V_{IN} = 0.2V to 1V	T_A = +25°C		±0.5	±1.5	
			T_A = T_{MIN} to T_{MAX}			±3.0	

**FSO refers to full-scale output under the conditions: V_{SENSE} = 100mV, V_{RS+} = +25V, or V_{IN} = 1V.*

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total POUT Output Error (Note 10)	ΔV_{POUT_MAX}/FSO	V_{SENSE} = 5mV to 100mV, V_{RS+} = 25V, V_{IN} = 0.2V to 1V	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT_MAX}/V_{POUT}	V_{SENSE} = 150mV, V_{RS+} = 25V, V_{IN} = 600mV	T_A = +25°C		±0.2	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 100mV, V_{RS+} = 15V, V_{IN} ≥ 160mV			±2.5		
		V_{SENSE} = 100mV, V_{RS+} = 15V, V_{IN} ≥ 360mV			±1.2		
		V_{SENSE} = 50mV, V_{RS+} = 15V, V_{IN} ≥ 240mV			±1.8		
		V_{SENSE} = 25mV, V_{RS+} = 15V, V_{IN} ≥ 600mV			±1.8		
POUT Output Offset Voltage (Note 11)		V_{SENSE} = 0V, V_{RS+} = 25V, V_{IN} = 1V	T_A = +25°C		1.5	5	mV
			T_A = T_{MIN} to T_{MAX}			15	
MAX4210E/MAX4211E (power gain = 25.00)							
POUT Gain Accuracy (Note 9)	ΔV_{POUT}/ΔV_{SENSE}	V_{SENSE} = 10mV to 100mV, V_{IN} = 1V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT}/ΔV_{IN}	V_{SENSE} = 100mV, V_{IN} = 0.2V to 1V	T_A = +25°C		±0.5	±1.5	
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total POUT Output Error (Note 10)	ΔV_{POUT_MAX}/FSO	V_{SENSE} = 5mV to 100mV, V_{RS+} = 25V, V_{IN} = 0.2V to 1V	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{POUT_MAX}/V_{POUT}	V_{SENSE} = 150mV, V_{RS+} =25V, V_{IN} = 600mV	T_A = +25°C		±0.2	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 100mV, V_{RS+} = 15V, V_{IN} ≥ 160mV			±2.5		
		V_{SENSE} = 100mV, V_{RS+} = 15V, V_{IN} ≥ 360mV			±1.2		
		V_{SENSE} = 50mV, V_{RS+} = 15V, V_{IN} ≥ 240mV			±1.8		
		V_{SENSE} = 25mV, V_{RS+} = 15V, V_{IN} ≥ 600mV			±1.8		
POUT Output Offset Voltage (Note 11)		V_{SENSE} = 0V, V_{RS+} = 25V, V_{IN} = 1V	T_A = +25°C		2	6.5	mV
			T_A = T_{MIN} to T_{MAX}			20	

**FSO refers to full-scale output under the conditions: V_{SENSE} = 100mV, V_{RS+} = +25V, or V_{IN} = 1V.*

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAX4210F/MAX4211F (power gain = 40.96)							
POUT Gain Accuracy (Note 9)	$\Delta V_{POUT}/\Delta V_{SENSE}$	V_{SENSE} = 10mV to 100mV, V_{IN} = 1V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
	$\Delta V_{POUT}/\Delta V_{IN}$	V_{SENSE} = 100mV, V_{IN} = 0.2V to 1V	T_A = +25°C		±0.5	±1.5	
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total POUT Output Error (Note 10)	ΔV_{POUT_MAX}/FSO	V_{SENSE} = 5mV to 100mV, V_{RS+} = 25V, V_{IN} = 0.2V to 1V	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	$\Delta V_{POUT\_MAX}/V_{POUT}$	V_{SENSE} = 100mV, V_{RS+} = 15V, V_{IN} ≥ 160mV			±2.5		%
		V_{SENSE} = 100mV, V_{RS+} = 15V, V_{IN} ≥ 360mV			±1.2		
		V_{SENSE} = 50mV, V_{RS+} = 15V, V_{IN} ≥ 240mV			±1.8		
		V_{SENSE} = 25mV, V_{RS+} = 15V, V_{IN} ≥ 600mV			±1.8		
POUT Output Offset Voltage (Note 11)		V_{SENSE} = 0V, V_{RS+} = 25V, V_{IN} = 1V	T_A = +25°C		3	10	mV
			T_A = T_{MIN} to T_{MAX}			30	
MAX4211A/MAX4211D (current gain = 16.67)							
IOUT Gain Accuracy	$\Delta V_{IOUT}/\Delta V_{SENSE}$	V_{SENSE} = 20mV to 100mV, V_{RS+} = 25V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total IOUT Output Error (Note 10)	ΔV_{IOUT_MAX}/FSO	V_{SENSE} = 5mV to 100mV	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	$\Delta V_{IOUT\_MAX}/V_{IOUT}$	V_{SENSE} = 150mV	T_A = +25°C		±0.2	±1.5	%
			T_A= T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 50mV			±1.2		
		V_{SENSE} = 25mV			±1.8		
		V_{SENSE} = 5mV			±20		

**FSO refers to full-scale output under the conditions: V_{SENSE} = 100mV, V_{RS+} = +25V, or V_{IN} = 1V.*

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 5mV, V_{IN} = 1.0V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = GND, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAX4211B/MAX4211E (current gain = 25.00)							
IOUT Gain Accuracy	ΔV_{IOUT}/ ΔV_{SENSE}	V_{SENSE} = 20mV to 100mV, V_{RS+} = 25V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total IOUT Output Error (Note 10)	ΔV_{IOUT_MAX}/ FSO	V_{SENSE} = 5mV to 100mV	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{IOUT_MAX}/ V_{IOUT}	V_{SENSE} = 150mV	T_A = +25°C		±0.2	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 50mV			±1.2		
		V_{SENSE} = 25mV			±1.8		
		V_{SENSE} = 5mV			±20		
MAX4211C/MAX4211F (current gain = 40.96)							
IOUT Gain Accuracy	ΔV_{IOUT}/ ΔV_{SENSE}	V_{SENSE} = 20mV to 100mV, V_{RS+} =25V	T_A = +25°C		±0.5	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
Total IOUT Output Error (Note 10)	ΔV_{IOUT_MAX}/ FSO	V_{SENSE} = 5mV to 100mV	T_A = +25°C		±0.15	±1.5	% FSO*
			T_A = T_{MIN} to T_{MAX}			±3.0	
	ΔV_{IOUT_MAX}/ V_{IOUT}	V_{SENSE} = 100mV	T_A = +25°C		±0.2	±1.5	%
			T_A = T_{MIN} to T_{MAX}			±3.0	
		V_{SENSE} = 50mV			±1.2		
		V_{SENSE} = 25mV			±1.8		
		V_{SENSE} = 5mV			±20		

**FSO refers to full-scale output under the conditions:* V_{SENSE} = 100mV, V_{RS+} = +25V, *or* V_{IN} = 1V.

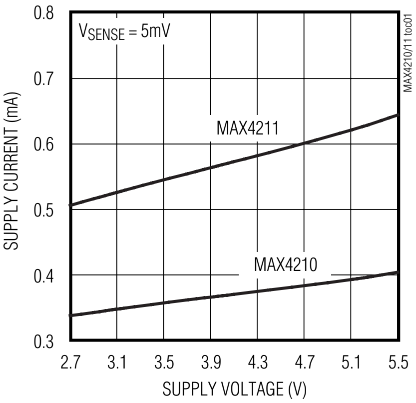
Note 1: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 2: Guaranteed by power-supply rejection test.
Note 3: Guaranteed by output voltage error tests (IOUT).
Note 4: Guaranteed by output voltage error tests (IOUT or POUT, or both).
Note 5: IN Input Voltage Range (MAX421_D/E/F) and V_{RS+} Input Voltage Range (MAX421_A/B/C) are guaranteed by design (GBD) and not production tested. See Multiplier Transfer Characteristics graphs in the *Typical Operating Characteristics*.
Note 6: This test does not apply to the low gain options, MAX421_A/D, because OUT is clamped at approximately 4V.
Note 7: The device does not experience phase reversal when overdriven.
Note 8: V_{PULLUP} is defined as an externally applied voltage through a resistor, R_{PULLUP}, to pull up the comparator output.
Note 9: POUT gain accuracy is the sum of gain error and multiplier nonlinearity.
Note 10: Total output voltage error is the sum of gain and offset voltage errors.
Note 11: POUT Output Offset Voltage is the sum of offset and multiplier feedthrough.

High-Side Power and Current Monitors

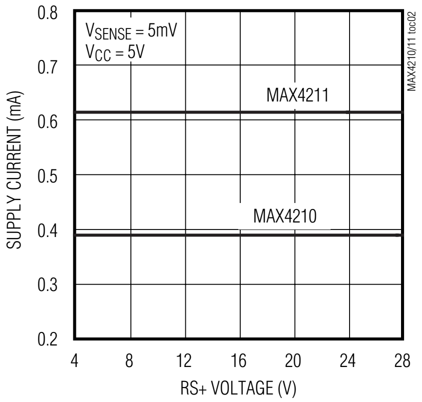
Typical Operating Characteristics

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 100mV, V_{IN} = 1V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = 0V, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = +25°C, unless otherwise noted.)

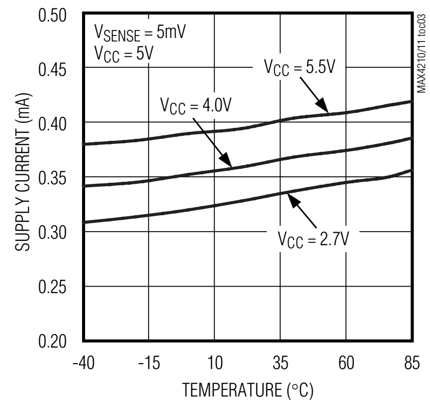
SUPPLY CURRENT vs. SUPPLY VOLTAGE



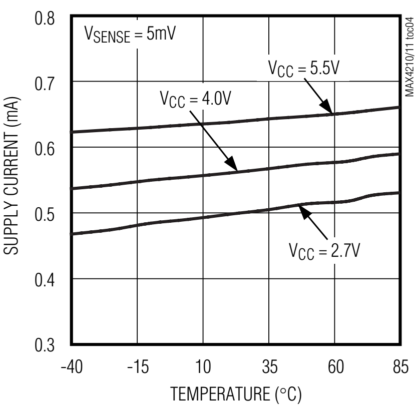
SUPPLY CURRENT vs. COMMON-MODE VOLTAGE



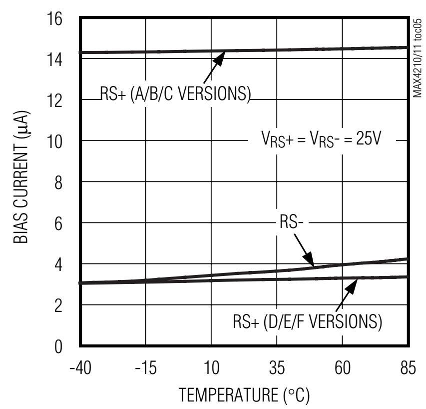
MAX4210 SUPPLY CURRENT vs. TEMPERATURE



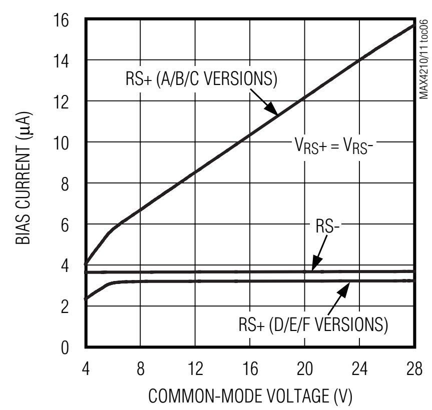
MAX4211 SUPPLY CURRENT vs. TEMPERATURE



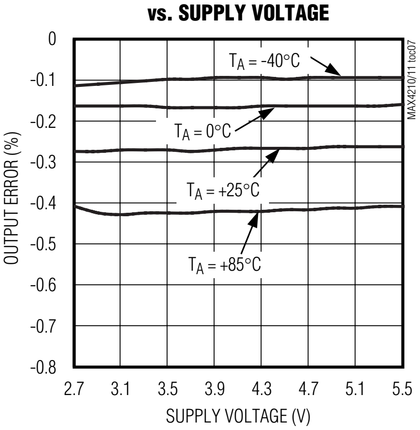
RS+/RS- BIAS CURRENT vs. TEMPERATURE



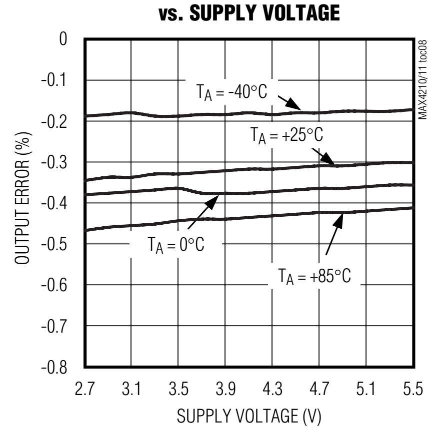
RS+/RS- BIAS CURRENT vs. COMMON-MODE VOLTAGE



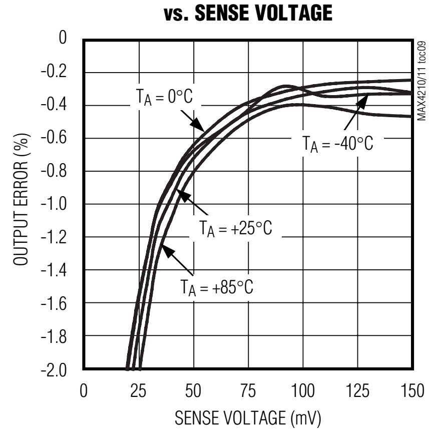
POWER OUTPUT ERROR vs. SUPPLY VOLTAGE



CURRENT OUTPUT ERROR vs. SUPPLY VOLTAGE



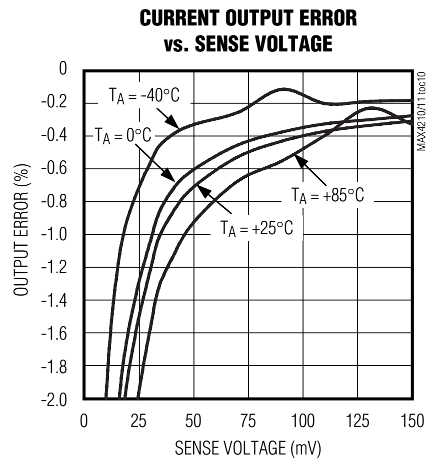
POWER OUTPUT ERROR vs. SENSE VOLTAGE

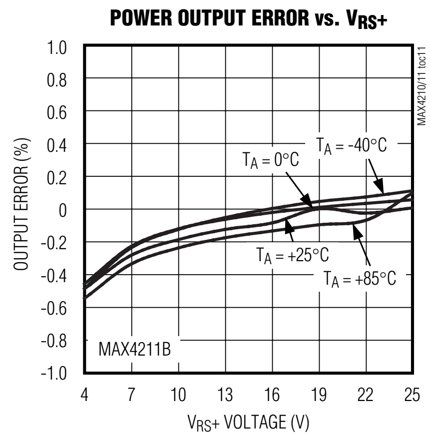


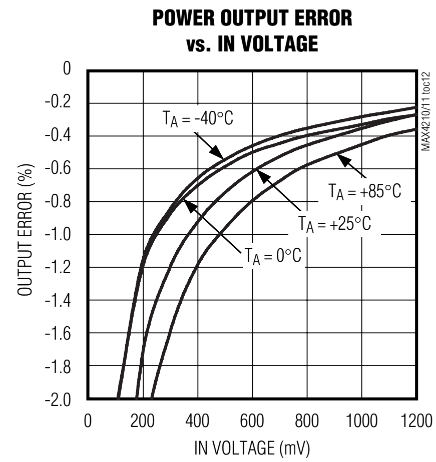
High-Side Power and Current Monitors

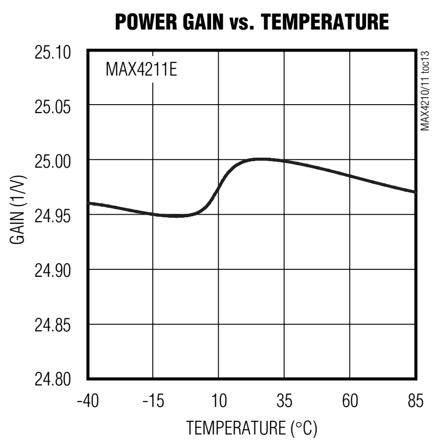
Typical Operating Characteristics (continued)

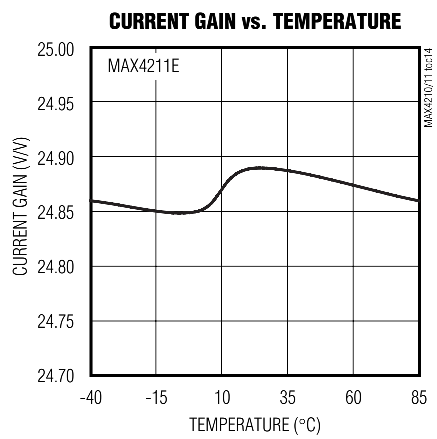
(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 100mV, V_{IN} = 1V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = 0V, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = +25°C, unless otherwise noted.)

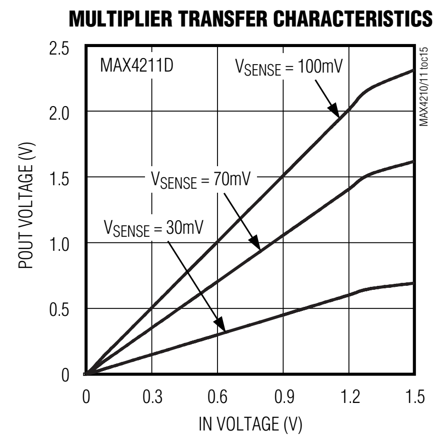


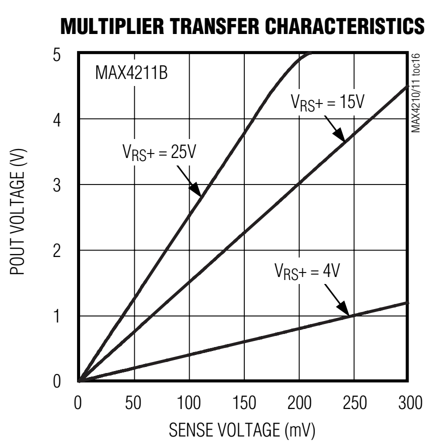


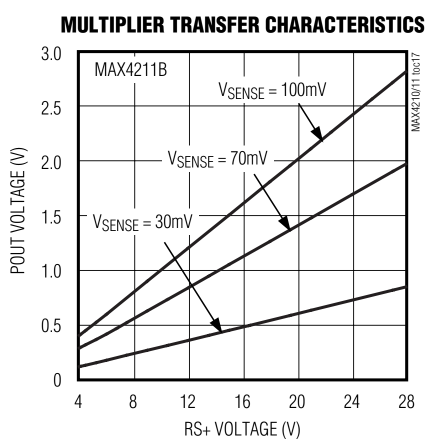


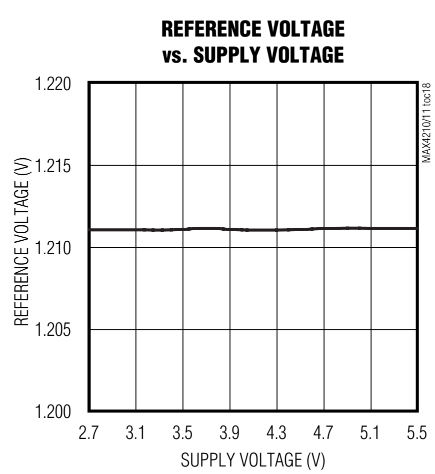








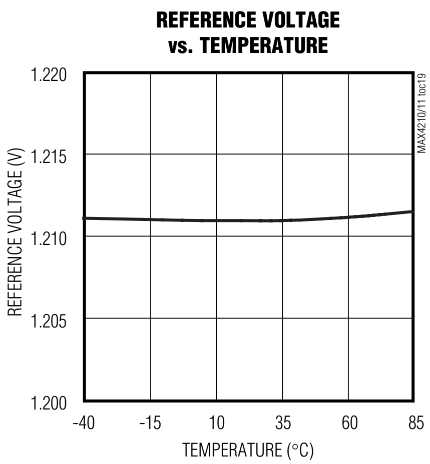


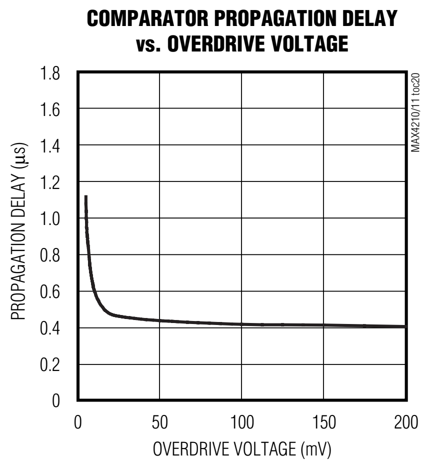


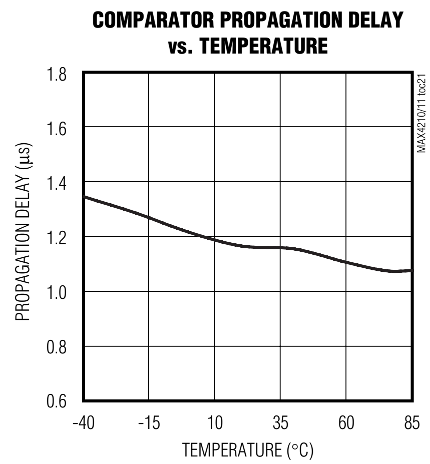
High-Side Power and Current Monitors

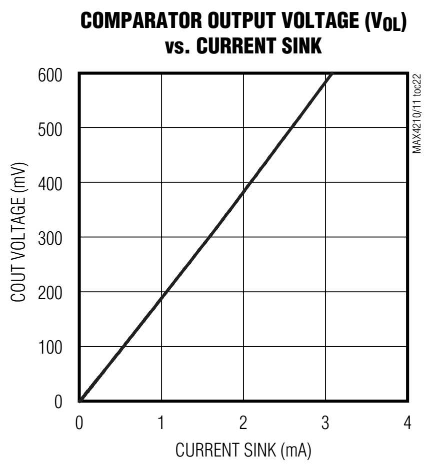
Typical Operating Characteristics (continued)

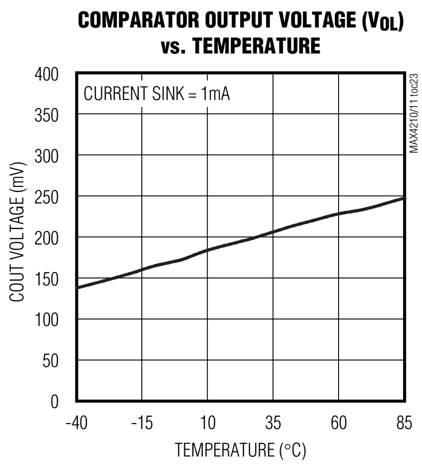
(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 100mV, V_{IN} = 1V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = 0V, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = +25°C, unless otherwise noted.)

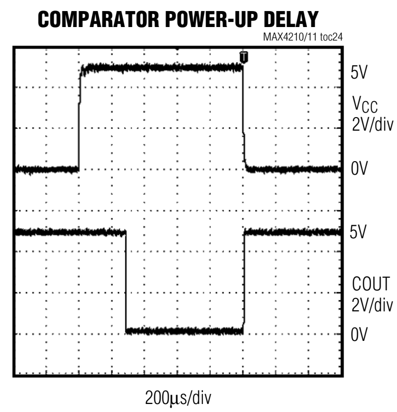


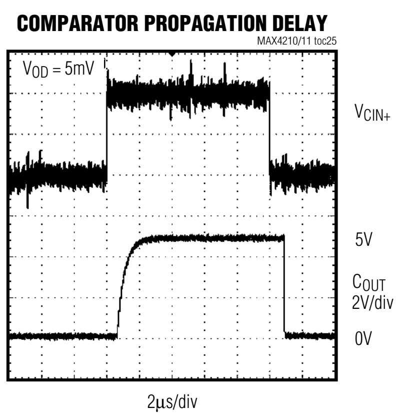


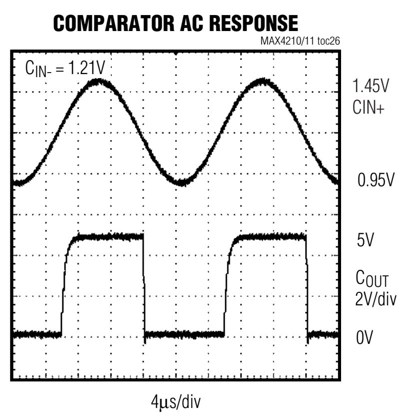


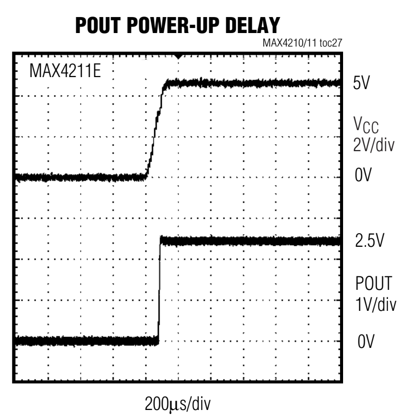








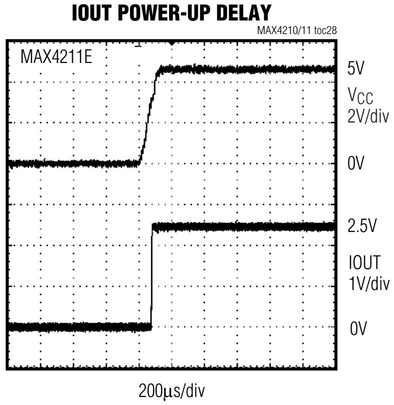




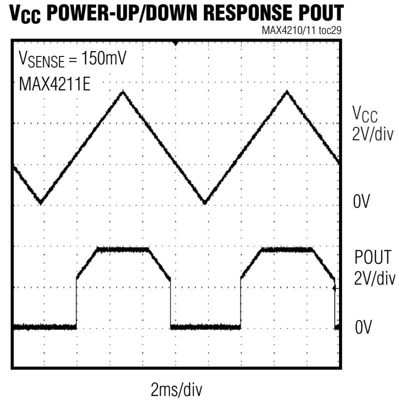
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 100mV, V_{IN} = 1V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = 0V, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = +25°C, unless otherwise noted.)

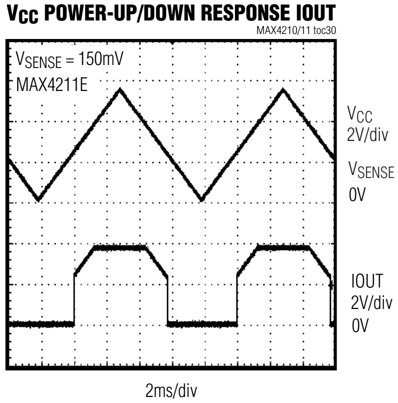
IOUT POWER-UP DELAY



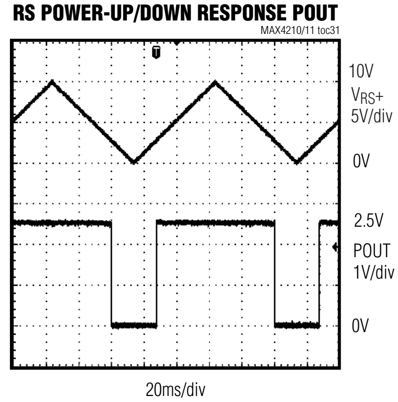
V_{CC} POWER-UP/DOWN RESPONSE POUT



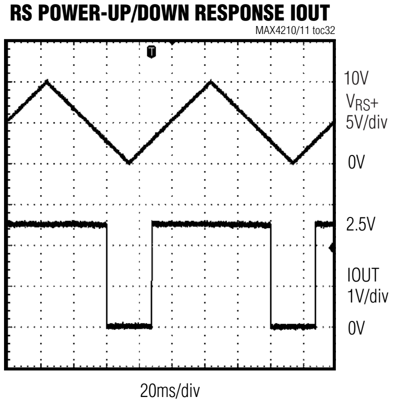
V_{CC} POWER-UP/DOWN RESPONSE IOUT



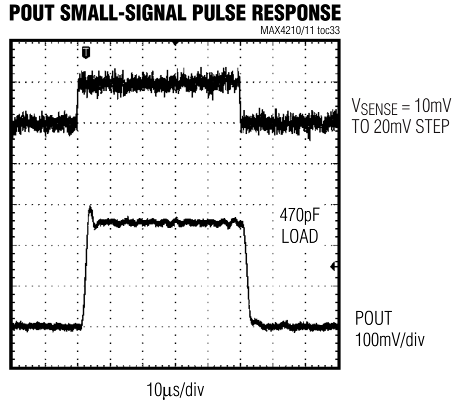
RS POWER-UP/DOWN RESPONSE POUT



RS POWER-UP/DOWN RESPONSE IOUT



POUT SMALL-SIGNAL PULSE RESPONSE

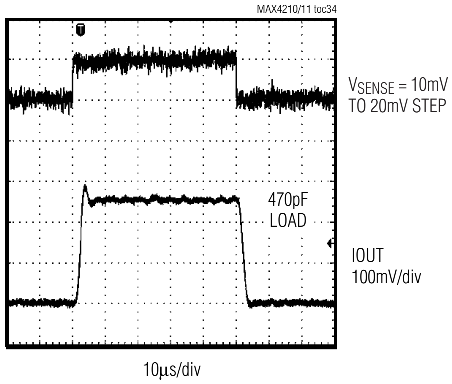


High-Side Power and Current Monitors

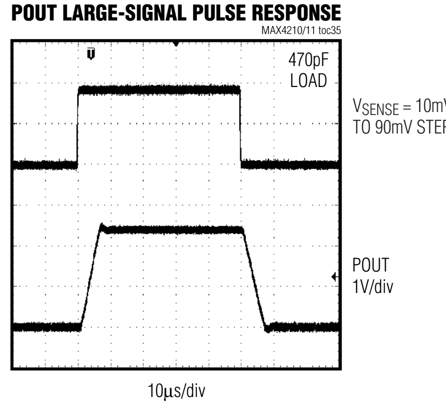
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 100mV, V_{IN} = 1V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = 0V, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = +25°C, unless otherwise noted.)

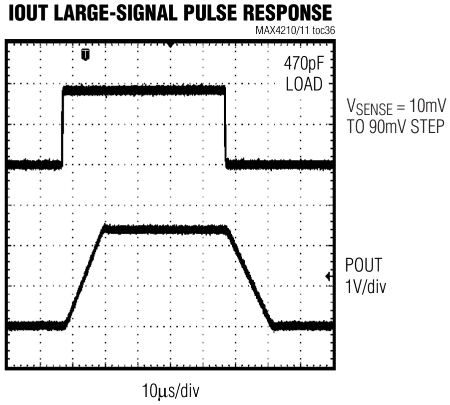
IOUT SMALL-SIGNAL PULSE RESPONSE



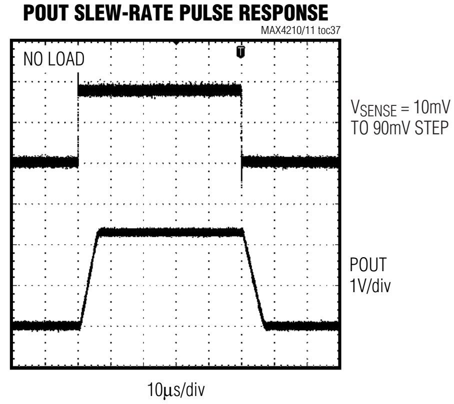
POUT LARGE-SIGNAL PULSE RESPONSE



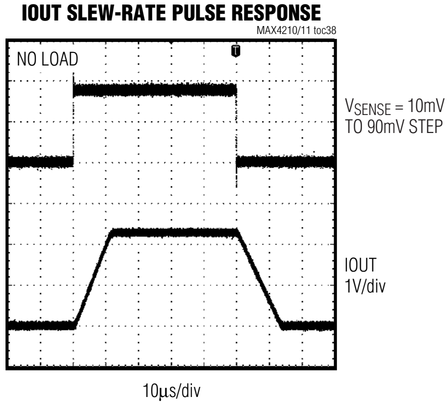
IOUT LARGE-SIGNAL PULSE RESPONSE



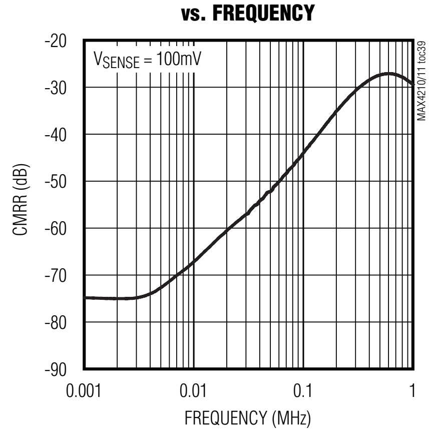
POUT SLEW-RATE PULSE RESPONSE



IOUT SLEW-RATE PULSE RESPONSE



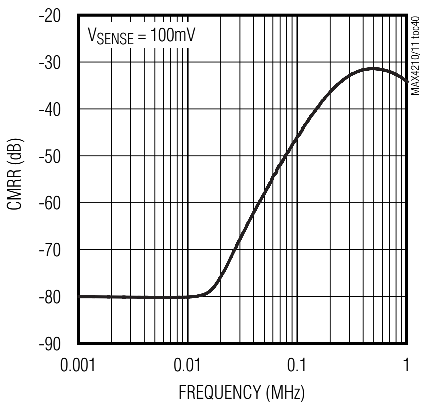
POUT COMMON-MODE REJECTION RATIO vs. FREQUENCY



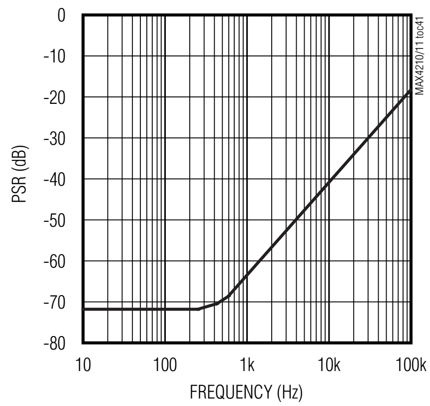
Typical Operating Characteristics (continued)

(V_{CC} = 5.0V, V_{RS+} = 25V, V_{SENSE} = 100mV, V_{IN} = 1V, V_{LE} = 0V, R_{IOUT} = R_{POUT} = 1MΩ, V_{CIN1+} = V_{CIN2+} = V_{REF}, V_{CIN1-} = V_{CIN2-} = 0V, $V_{INHIBIT}$ = 0V, R_{COUT1} = R_{COUT2} = 5kΩ connected to V_{CC}, T_A = +25°C, unless otherwise noted.)

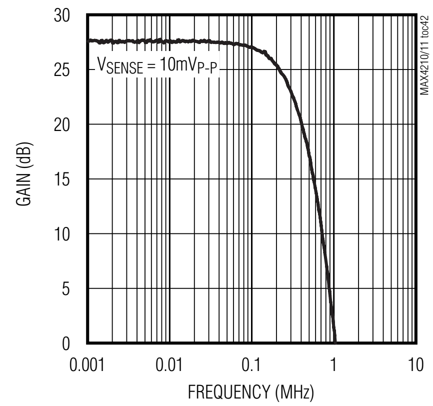
IOUT COMMON-MODE REJECTION RATIO vs. FREQUENCY



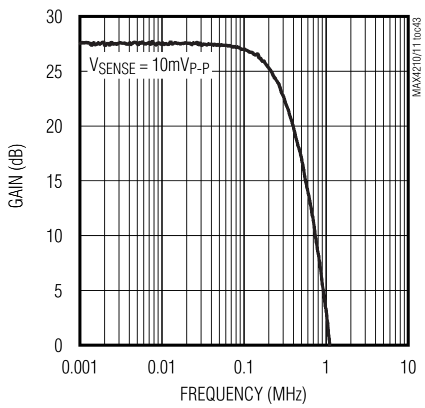
POWER-SUPPLY REJECTION vs. FREQUENCY



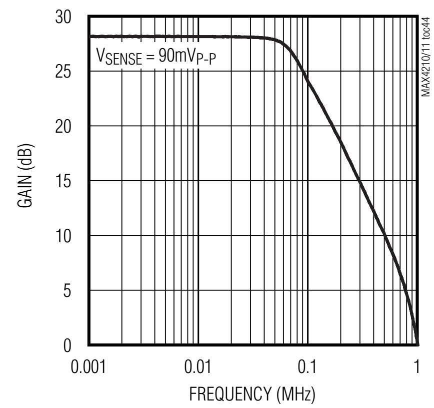
POUT SMALL-SIGNAL GAIN vs. FREQUENCY



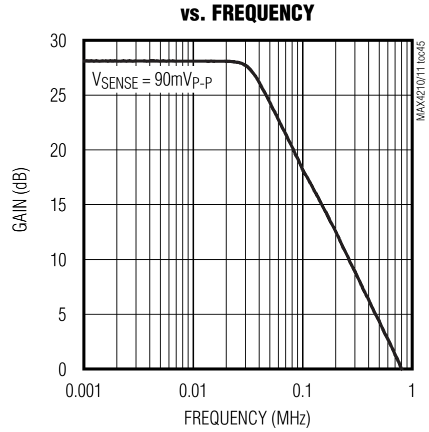
IOUT SMALL-SIGNAL GAIN vs. FREQUENCY



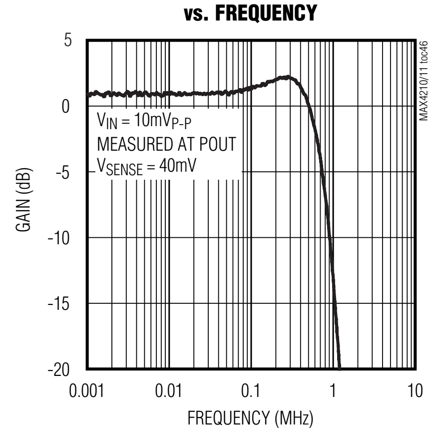
POUT LARGE-SIGNAL GAIN vs. FREQUENCY



IOUT LARGE-SIGNAL GAIN vs. FREQUENCY



IN SMALL-SIGNAL GAIN vs. FREQUENCY



High-Side Power and Current Monitors

MAX4210A/B/C Pin Description

PIN		NAME	FUNCTION
6 TDFN	8 μMAX		
1	1	GND	Ground
2	2, 3, 6	N.C.	No Connection. Not internally connected.
3	4	V_{CC}	Power-Supply Voltage. Connect a 0.1μF bypass capacitor from V_{CC} to GND.
4	5	RS+	Power Connection to External-Sense Resistor and Internal Resistor-Divider
5	7	RS-	Load-Side Connection for External-Sense Resistor
6	8	POUT	Power Output Voltage. Voltage output proportional to source power (input voltage multiplied by load current).
EP	—	EP*	Exposed Paddle. EP is internally connected to GND.

**TDFN package only.*

MAX4210D/E/F Pin Description

PIN		NAME	FUNCTION
6 TDFN	8 μMAX		
1	1	GND	Ground
2	2	IN	Multiplier Input Voltage. Voltage input for internal multiplier.
3	4	V_{CC}	Power-Supply Voltage. Connect a 0.1μF bypass capacitor from V_{CC} to GND.
4	5	RS+	Power Connection to External-Sense Resistor
5	7	RS-	Load-Side Connection for External-Sense Resistor
6	8	POUT	Power Output Voltage. Voltage output proportional to source power (input voltage multiplied by load current).
EP	—	EP*	Exposed Paddle. EP is internally connected to GND.
—	3, 6	N.C.	No Connection. Not internally connected.

**TDFN package only.*

MAX4211A/B/C Pin Description

PIN		NAME	FUNCTION
16 THIN QFN	16 TSSOP		
1	3	V_{CC}	Power-Supply Voltage. Connect a 0.1µF bypass capacitor from V_{CC} to GND.
2	4	N.C.	No Connection. Not internally connected.
3	5	LE	Latch Enable for Comparator 1. Driving logic low makes the comparator transparent (regular comparator). Driving logic high latches the output.
4	6	COUT1	Open-Drain Comparator 1 Output. LE and INHIBIT control the comparator 1 output.
5	7	INHIBIT	INHIBIT for Comparator 1 Output. Driving logic high inhibits the comparator operation. Drive logic low for normal operation.
6	8	COUT2	Open-Drain Comparator 2 Output
7	9	GND	Ground
8	10	CIN2+	Comparator 2 Positive Input
9	11	CIN2-	Comparator 2 Negative Input
10	12	CIN1+	Comparator 1 Positive Input
11	13	CIN1-	Comparator 1 Negative Input
12	14	REF	1.21V Internal Reference Output
13	15	POUT	Power Output Voltage. Voltage output proportional to source power (input voltage multiplied by load current).
14	16	IOUT	Current Output Voltage. Voltage output proportional to V_{SENSE} (V_{RS+} - V_{RS-}) load current.
15	1	RS-	Load-Side Connection for External-Sense Resistor
16	2	RS+	Power Connection to External-Sense Resistor and Internal Resistor-Divider
EP	—	EP*	Exposed Paddle. EP is internally connected to GND.

*Thin QFN package only.

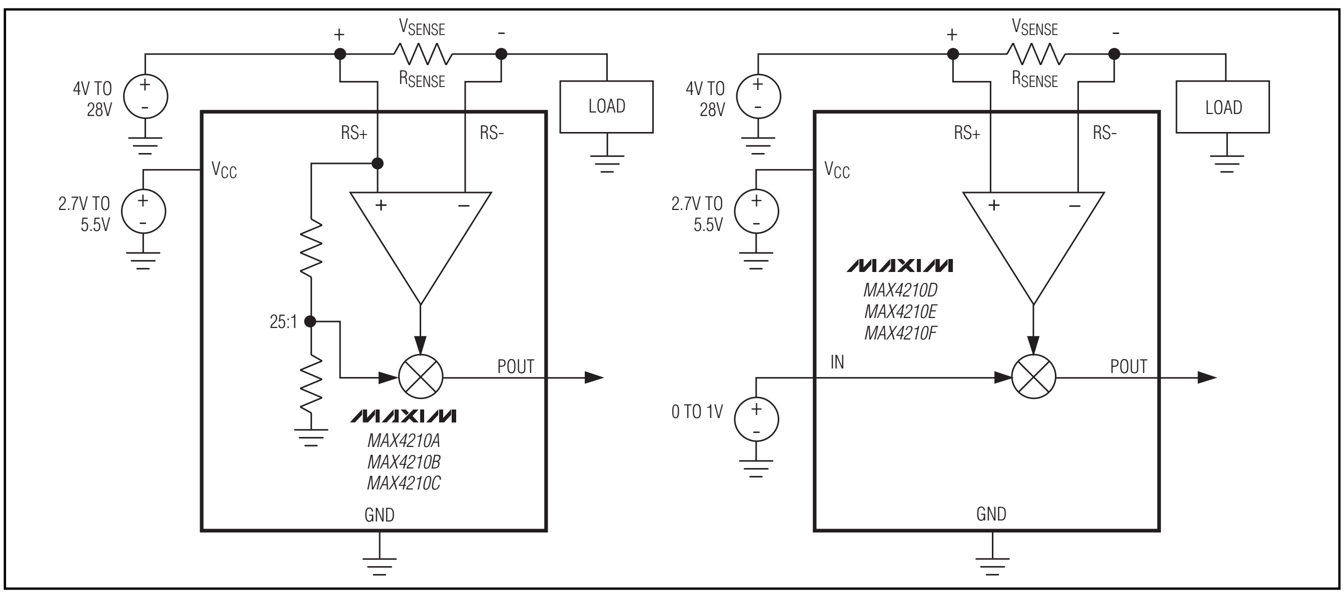
High-Side Power and Current Monitors

MAX4211D/E/F Pin Description

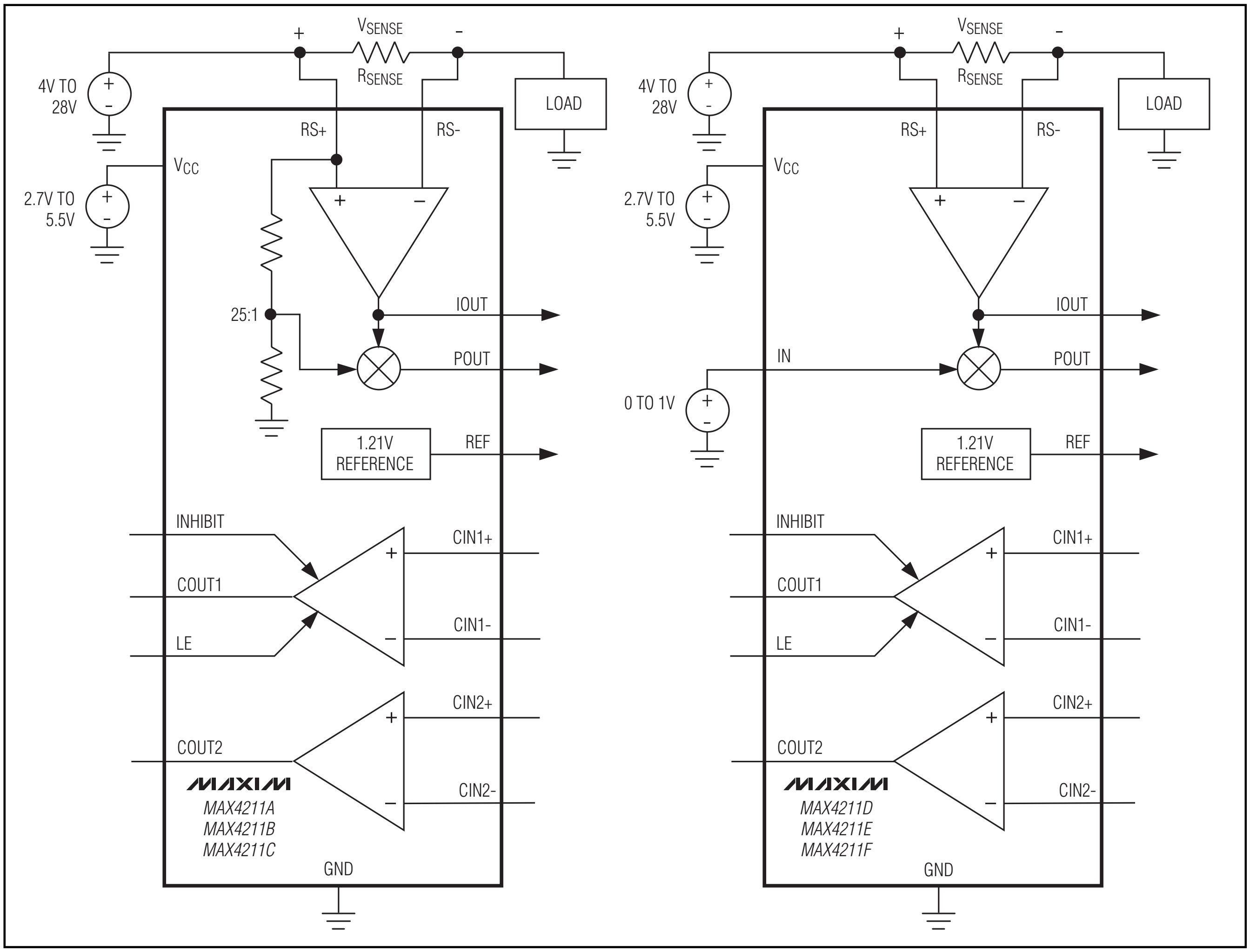
PIN		NAME	FUNCTION
16 THIN QFN	16 TSSOP		
1	3	V_{CC}	Power-Supply Voltage. Connect a 0.1µF bypass capacitor from V_{CC} to GND.
2	4	IN	Multiplier Input Voltage. Voltage input for internal multiplier.
3	5	LE	Latch Enable for Comparator 1. Driving logic low makes the comparator transparent (regular comparator). Driving logic high latches the output.
4	6	COUT1	Open-Drain Comparator 1 Output. Output controlled by LE and INHIBIT.
5	7	INHIBIT	INHIBIT for Comparator 1 Output. Driving logic high inhibits the comparator operation. Drive logic low for normal operation.
6	8	COUT2	Open-Drain Comparator 2 Output
7	9	GND	Ground
8	10	CIN2+	Comparator 2 Positive Input
9	11	CIN2-	Comparator 2 Negative Input
10	12	CIN1+	Comparator 1 Positive Input
11	13	CIN1-	Comparator 1 Negative Input
12	14	REF	1.21V Internal Reference Output
13	15	POUT	Power Output Voltage. Voltage output proportional source power (input voltage multiplied by load current).
14	16	IOUT	Current Output Voltage. Voltage output proportional V_{SENSE} (V_{RS+} - V_{RS-}) load current.
15	1	RS-	Load-Side Connection for External-Sense Resistor
16	2	RS+	Power Connection to External-Sense Resistor
EP	—	EP*	Exposed Paddle. EP is internally connected to GND.

**Thin QFN package only.*

Functional Diagrams



Functional Diagrams (continued)



Detailed Description

The MAX4210/MAX4211 families of current- and power-monitoring ICs integrate a precision current-sense amplifier and an analog multiplier for a variety of current and power measurements. The MAX4211 integrates an additional uncommitted 1.21V reference and two comparators with open-drain outputs. These features enable the design of detector circuits for overpower, overcurrent, overvoltage, or any combination of fault conditions. The MAX4210/MAX4211 offer various gains, packages, and configurations allowing for greater design flexibility and lower overall cost.

These devices monitor the load current with their high-side current-sense amplifiers and provide an analog output voltage proportional to that current at IOUT (MAX4211). This voltage is fed to the analog multiplier for multiplying the load current with a source voltage to obtain a voltage proportional to load power at POUT.

Current-Sense Amplifier

The integrated current-sense amplifier is a differential amplifier that amplifies the voltage across RS+ and RS-. A sense resistor, R_{SENSE}, is connected across RS+ and RS-. A voltage drop across R_{SENSE} is developed when a load current is passed through it. This voltage is amplified and is proportional to the load current. This voltage is also fed to the analog multiplier for power-sensing applications (see the *Analog Multiplier* section). The current-sense amplifiers feature three gain options: 16.67V/V, 25.0V/V, and 40.96V/V (see Table 1).

High-Side Power and Current Monitors

The common-mode voltage range is +4V to +28V and independent of the supply voltage. With this feature, the device can monitor the output current of a high-voltage source while running at a lower system voltage typically between 2.7V and 5.5V.

The MAX4211 has a current-sense amplifier output. The voltage at IOUT is proportional to the voltage across V_{SENSE}:

$$V_{IOUT} = A_{VIOUT} \times V_{SENSE}$$

where V_{SENSE} is the voltage across RS+ and RS-, and A_{VIOUT} is the amplifier gain of the device given in Table 1.

Analog Multiplier

The MAX4210/MAX4211 integrate an analog multiplier that enables real-time monitoring of power delivered to a load. The voltage proportional to the load current is fed to one input of the multiplier and a voltage proportional to the source voltage is fed to the other. The analog multiplier multiplies these two voltages to obtain an output voltage proportional to the load power. The analog multiplier is designed only to operate in the positive quadrant, that is, the inputs and outputs are always positive voltages.

For the MAX4210D/E/F and MAX4211D/E/F, the analog multiplier full-scale input at IN is approximately 1V. This independent multiplier input allows greater design flexibility when using an external voltage-divider. For the MAX4210A/B/C and MAX4211A/B/C, an integrated voltage-divider divides the source voltage at the RS+ pin by a nominal value of 25 and passes this voltage to the multiplier. Thus, the full-scale input voltage at RS+ is 25V. The integrated, trimmed resistor-dividers reduce external component count and cost.

The voltage output at POUT is proportional to the output power:

For the MAX4210A/B/C and MAX4211A/B/C:

$$V_{POUT} = A_{VPOUT} \times V_{SENSE} \times V_{RS+}$$

For the MAX4210D/E/F and MAX4211D/E/F:

$$V_{POUT} = A_{VPOUT} \times V_{SENSE} \times V_{IN}$$

Table 1. MAX4211 Current-Sense Amplifier Gain and Full-Scale Sense Voltage

PART	CURRENT-SENSE AMPLIFIER GAIN (A_{VIOUT}, V/V)	FULL-SCALE SENSE VOLTAGE (mV)
MAX4211A/D	16.67	150
MAX4211B/E	25.00	150
MAX4211C/F	40.96	100

where V_{SENSE} is the voltage across RS+ and RS- and A_{VPOUT} is the amplifier gain of the device given in Table 2.

Internal Comparators (MAX4211)

The MAX4211 features two uncommitted open-drain output comparators. These comparators can be configured to trip when load current or power reaches a set limit. They can also be configured as a window comparator with wire-OR output. Comparator 1 (COUT1) features latch-enable (LE) and inhibit (INHIBIT) inputs. When LE is low, the comparator is transparent (it functions as a regular unlatched comparator). When LE is high, the comparator output (COUT1) is latched. When high, the INHIBIT input suspends the comparator operation and latches the output to the current state. The operation of INHIBIT is similar to LE, except it has a different input threshold and wider hysteresis. The INHIBIT logic-high threshold is 1.21V and logic-low threshold is 0.6V with 0.6V hysteresis. INHIBIT is useful in preventing the comparator from giving false output during fast RS+ transients. INHIBIT is generally triggered by an RC network connected to RS+ (see the *Applications Information*). Both comparators have a built-in 300µs blanking period at power-up to prevent false outputs. The comparator outputs are open drain and they can be pulled up to V_{CC}, RS+, or any voltage less than +28V. LE and INHIBIT are internally pulled down by a 1µA source.

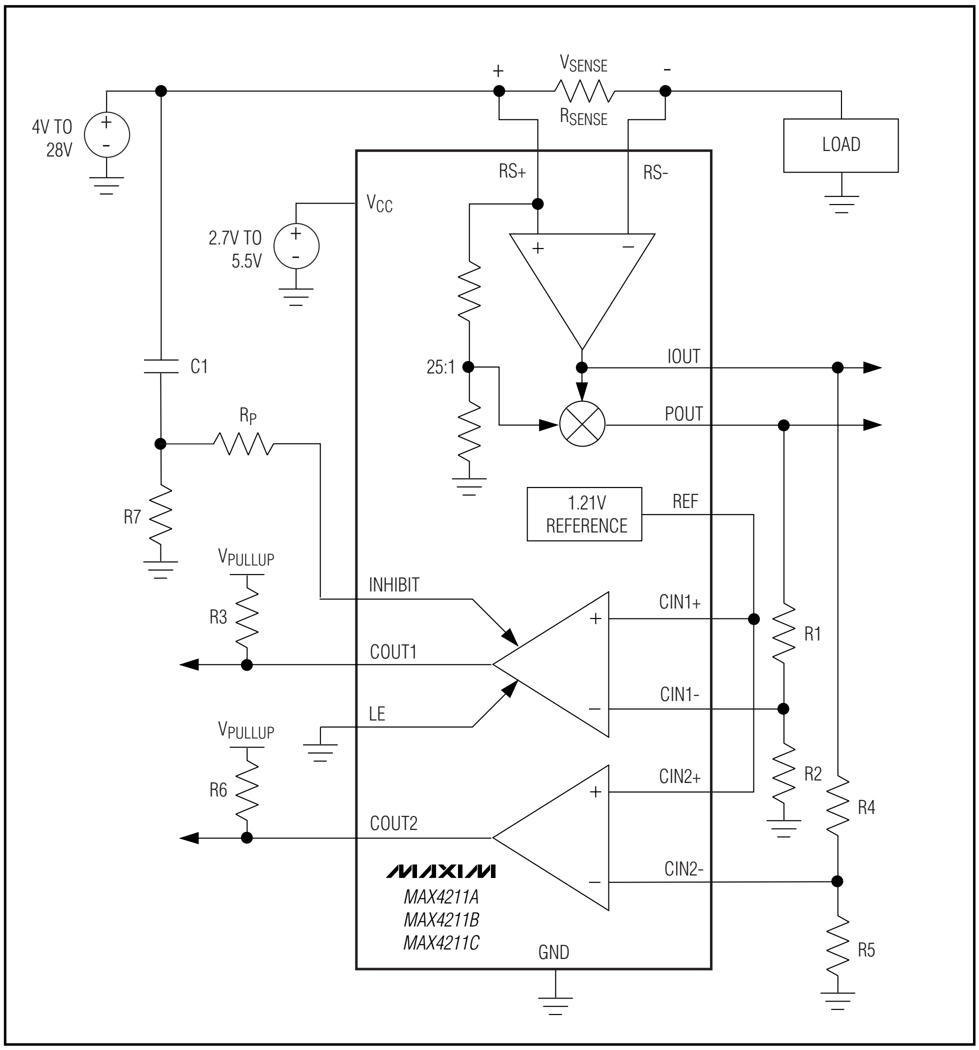
Table 2. MAX4210/MAX4211 Power-Sense Amplifier Gain and Full-Scale Sense Voltage

PART	POWER-SENSE AMPLIFIER GAIN (A_{VPOUT}, 1/V)	FULL-SCALE SENSE VOLTAGE (mV)
MAX4210A	0.667	150
MAX4210B	1.000	150
MAX4210C	1.640	100
MAX4210D	16.670	150
MAX4210E	25.000	150
MAX4210F	40.960	100
MAX4211A	0.667	150
MAX4211B	1.000	150
MAX4211C	1.640	100
MAX4211D	16.670	150
MAX4211E	25.000	150
MAX4211F	40.960	100

Internal Reference (MAX4211)

The MAX4211 features a 1.21V bandgap reference output, stable over supply voltage and temperature. Typically, the reference output is connected to one of the comparators' inputs. This is the comparison reference voltage. If a lower reference voltage is needed, use an external voltage-divider. The reference can source or sink a load current up to 100µA.

Typical Operating Circuit



High-Side Power and Current Monitors

Applications Information

Recommended Component Values

Ideally, the maximum load current develops the full-scale sense voltage across the current-sense resistor. Choose the gain version needed to yield the maximum current-sense amplifier output voltage without saturating it. The typical high-side saturation voltage is about V_{CC} - 0.25V. The current-sense amplifier output voltage is given by:

$$V_{IOUT} = V_{SENSE} \times A_{VIOUT}$$

where V_{IOUT} is the voltage fed to the analog multiplier or at IOUT. V_{SENSE} is the sense voltage. A_{VIOUT} is the current-sense amplifier gain of the device specified in Table 1. Calculate the maximum value for R_{SENSE} so the differential voltage across RS+ and RS- does not exceed the full-scale sense voltage:

$$R_{SENSE} = \frac{V_{SENSE(FULL-SCALE)}}{I_{LOAD(FULL-SCALE)}}$$

Choose the highest value resistance possible to maximize V_{SENSE} and thus minimize total output error. In applications monitoring high current, ensure that R_{SENSE} is able to dissipate its own I^2R power dissipation. If the resistor's power dissipation is exceeded, its value can drift or it can fail altogether, causing a differential voltage across the terminals in excess of the absolute maximum ratings. Use resistors specified for current-sensing applications.

Window Comparator

In some applications where undercurrent or underpower (open-circuit fault) and overcurrent or overpower (short-circuit fault) needs to be monitored, a window comparator is desirable. Figure 1 shows a simple circuit suitable for window detection. Let P_{OVER} be the minimum load power required to cause a low state at COUT2, and let P_{UNDER} be the maximum load current required to cause a high state at COUT1:

$$P_{UNDER}(WATTS) = \frac{V_{REF}}{A_{VPOUT} \times R_{SENSE}}\left(\frac{R1 + R_2}{R_2}\right)$$

$$P_{OVER}(WATTS) = \frac{V_{REF}}{A_{VPOUT} \times R_{SENSE}}\left(\frac{R4 + R_5}{R_5}\right)$$

where A_{VPOUT} is the power-sense amplifier gain given in Table 2, and V_{REF} is the internal reference voltage (1.2V, typ). The resulting comparator output is high when the current is inside the current window and low when the current is outside the window. Note that COUT1 and COUT2 are wire-ORed together.

Overpower Circuit Breaker

Figure 2 shows a circuit breaker that shuts off current to the load when an overpower fault is detected (the same circuit can be used to detect overcurrent conditions by connecting the R1-R2 resistor-divider to IOUT, instead of POUT). This circuit is useful for protecting the battery from short-circuit or overpower conditions. When a power fault is detected, the P-MOSFET, M1, is turned off and stays off until the manual reset button is pressed. Also, cycling the input power causes the LE pin to go low, which unlatches the comparator output OUT1 and resets the circuit breaker.

During power-up or when the characteristics of the load change, there can be an inrush current into the load. The temporary inrush current results in a higher voltage at POUT. This can bring the voltage at CIN+ above the reference voltage at CIN-, and, as a result, COUT1 goes high triggering the circuit-breaker function. This unwanted behavior can be disabled by bringing comparator 1's INHIBIT input high. An RC network connected to INHIBIT (R4 and C1) can be incorporated to suspend comparator 1's operation for a brief period. In this way, short surges in load power can be made invisible to the circuit-breaker function, while longer term overpower load demands (or a load short circuit) still "trip the breaker."

The logic-high threshold for INHIBIT is typically 1.2V, and the logic-low threshold is 0.6V. During power-up, INHIBIT quickly exceeds 1.2V through C1 and inhibits COUT1 from changing state. The comparator inputs are "inhibited" until the INHIBIT voltage is discharged to 0.6V. R3 is a current-limiting resistor, typically 10kΩ, which protects the INHIBIT input. Since INHIBIT is a high-impedance input, R3 has no effect on the R4-C1 charge/discharge time. The time during which the comparator is suspended is approximated by:

$$t_{INHIBIT} = R_4 \times C1 \ln\left(\frac{\Delta V}{0.6V}\right)$$

where ΔV is the voltage change at the load. For improved transient immunity, $t_{INHIBIT}$ can be increased as required, with the understanding that the breaker function will be suspended for this period.

If any comparator is not used, its input must be biased to a known state. For example, connect CIN+ to V_{CC} and CIN- to GND.

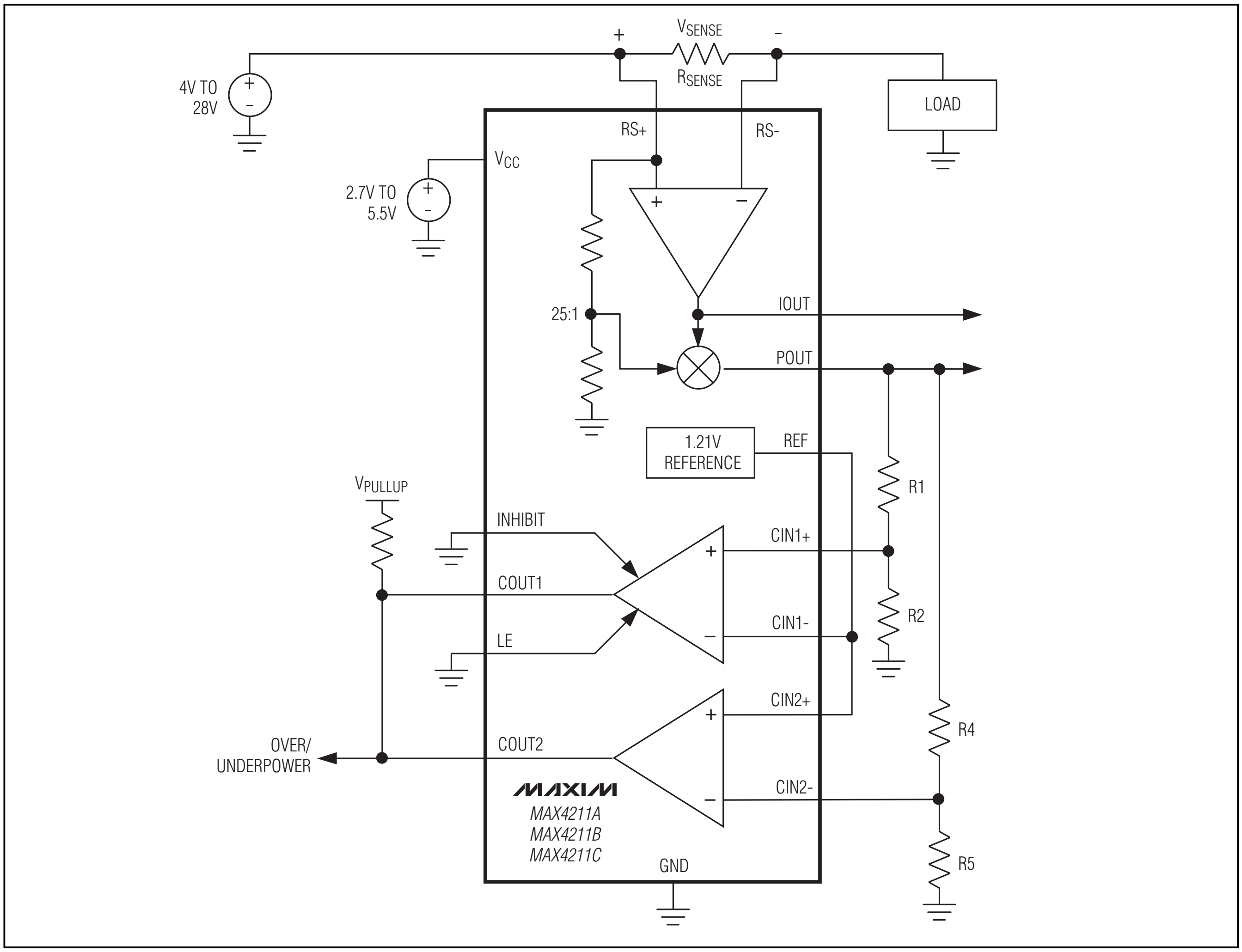


Figure 1. Window Comparator for Detecting Underpower and Overpower Faults (Also Detects Undercurrent and Overcurrent Faults by R1 and R4 to IOUT Instead of POUT)

Variable-Gain Amplifier

Figure 3 shows single-ended input, variable-gain amplifiers (VGA). This VGA features more than 200kHz bandwidth and is useful in automatic gain-control circuits commonly found in baseband processors. The gain is controlled by applying 0 to 1V to IN (V_{GC}) of the MAX4210D/E/F; 0V corresponds to minimum gain and 1V corresponds to maximum gain.

Measure Load Power

The MAX4210A/B/C and MAX4211A/B/C have internal voltage-divider resistors connected to RS+ and the analog multiplier input. This configuration measures source power accurately and provides protection to the power source such as a battery. To measure the load power accurately, choose the MAX4210D/E/F and MAX4211D/E/F with an external resistor-divider connected directly to the load as shown in Figure 4. This configuration improves the load-power measurement accuracy by excluding the additional power dissipated by R_{SENSE}.

Power-Supply Bypassing

Bypass V_{CC} to GND with a 0.1µF ceramic capacitor to isolate the IC from supply-voltage transients. To prevent high-frequency coupling, bypass RS+ or RS- with a 0.1µF capacitor. On the TDFN and thin QFN packages, there is an exposed paddle that does not carry any current, but should also be connected to the ground plane for rated power dissipation.

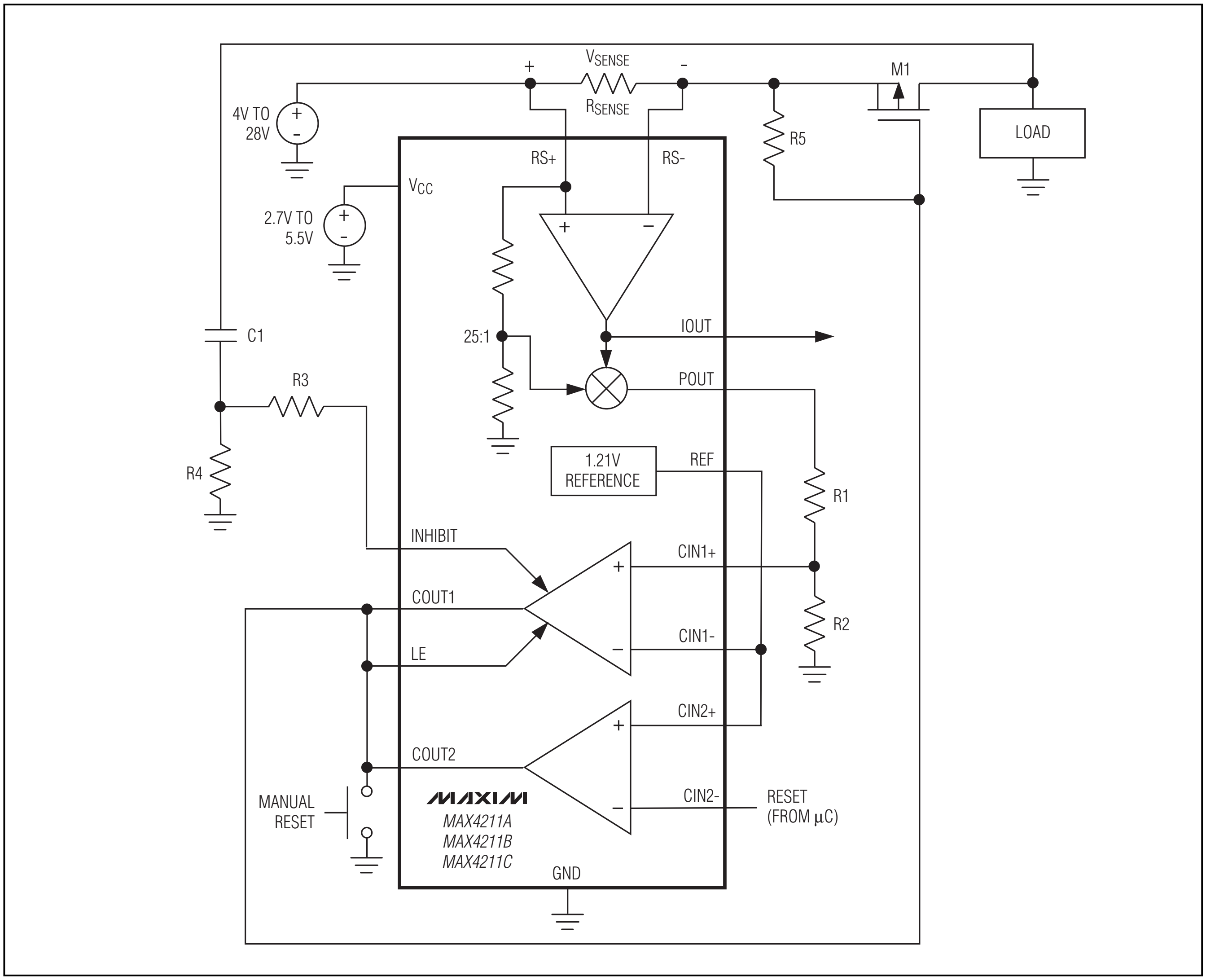


Figure 2. Overpower Circuit Breaker (For a Detailed Example, Refer to the MAX4211E EV Kit)

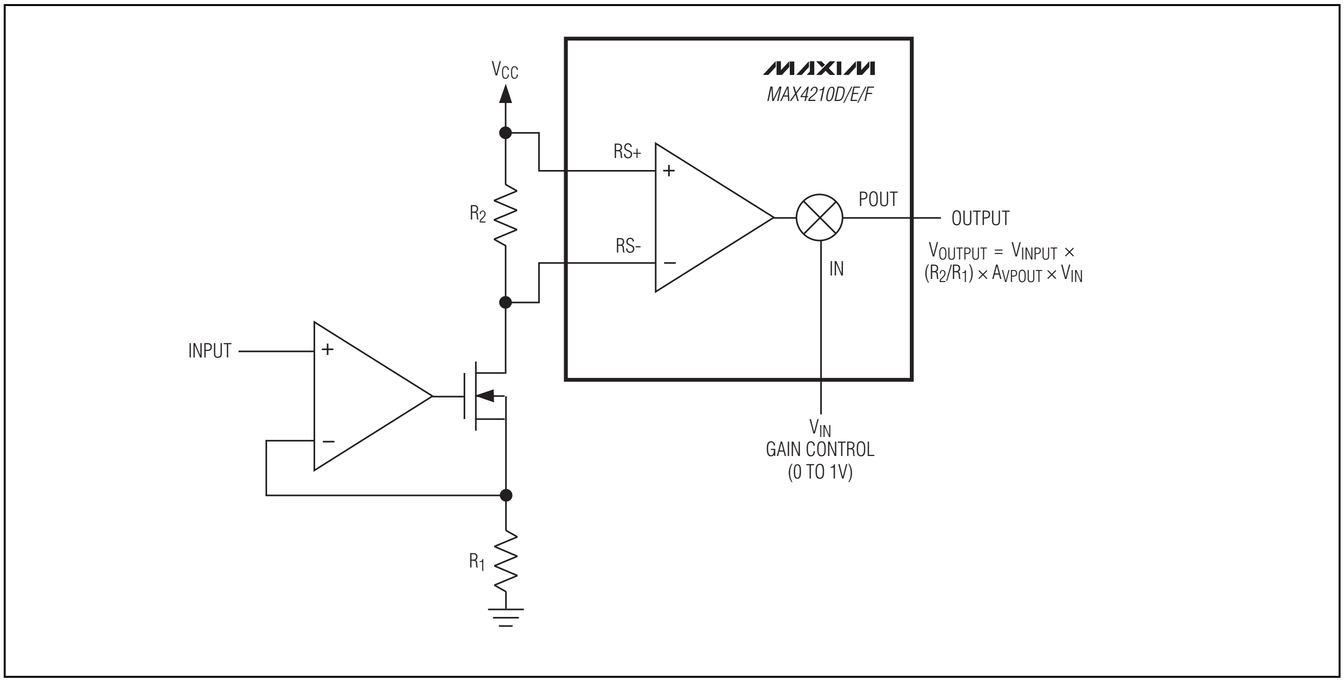


Figure 3. Single-Ended-Input, Variable-Gain Amplifier

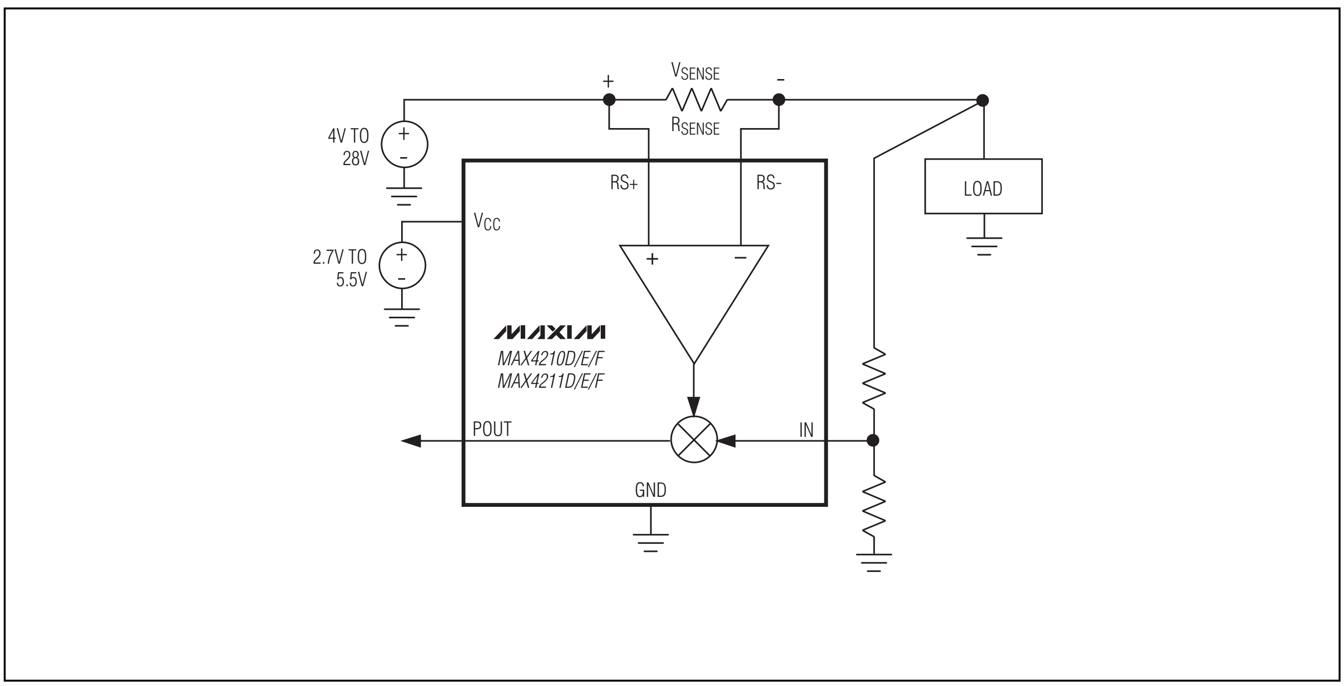


Figure 4. Load-Power Measurement with External Voltage-Divider

Selector Guide

PART	PIN-PACKAGE	CURRENT GAIN (V/V)	POWER GAIN (1/V)	CURRENT/ POWER MEASUREMENT OUTPUT	NO. OF COMPARATORS	INTERNAL REFERENCE	VOLTAGE-MULTIPLIER INPUT (INTERNAL RESISTOR-DIVIDER/ EXTERNAL INPUT)	FULL-SCALE V_{SENSE} VOLTAGE (mV)
MAX4210AETT	6 TDFN	—	0.667	P	None	N	INT	150
MAX4210AEUA	8 µMAX	—	0.667	P	None	N	INT	150
MAX4210BETT	6 TDFN	—	1.000	P	None	N	INT	150
MAX4210BEUA	8 µMAX	—	1.000	P	None	N	INT	150
MAX4210CETT	6 TDFN	—	1.640	P	None	N	INT	100
MAX4210CEUA	8 µMAX	—	1.640	P	None	N	INT	100
MAX4210DETT	6 TDFN	—	16.670	P	None	N	EXT	150
MAX4210DEUA	8 µMAX	—	16.670	P	None	N	EXT	150
MAX4210EETT	6 TDFN	—	25.000	P	None	N	EXT	150
MAX4210EEUA	8 µMAX	—	25.000	P	None	N	EXT	150
MAX4210FETT	6 TDFN	—	40.960	P	None	N	EXT	100
MAX4210FEUA	8 µMAX	—	40.960	P	None	N	EXT	100
MAX4211AETE	16 Thin QFN	16.67	0.667	C/P	2	Y	INT	150
MAX4211AEUE	16 TSSOP	16.67	0.667	C/P	2	Y	INT	150
MAX4211BETE	16 Thin QFN	25.00	1.000	C/P	2	Y	INT	150
MAX4211BEUE	16 TSSOP	25.00	1.000	C/P	2	Y	INT	150
MAX4211CETE	16 Thin QFN	40.96	1.640	C/P	2	Y	INT	100
MAX4211CEUE	16 TSSOP	40.96	1.640	C/P	2	Y	INT	100
MAX4211DETE	16 Thin QFN	16.67	16.670	C/P	2	Y	EXT	150
MAX4211DEUE	16 TSSOP	16.67	16.670	C/P	2	Y	EXT	150
MAX4211EETE	16 Thin QFN	25.00	25.000	C/P	2	Y	EXT	150
MAX4211EEUE	16 TSSOP	25.00	25.000	C/P	2	Y	EXT	150
MAX4211FETE	16 Thin QFN	40.96	40.960	C/P	2	Y	EXT	100
MAX4211FEUE	16 TSSOP	40.96	40.960	C/P	2	Y	EXT	100

C = Current Measurement Output Available (IOUT).

P = Power Measurement Output Available (POUT).

Y = Yes.

N = No.

INT = Internal Resistor-Divider.

EXT = External Input Pin.

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4210BETT	-40°C to +85°C	6 TDFN-6-EP* (3mm x 3mm)	AHG
MAX4210BEUA	-40°C to +85°C	8 μMAX	—
MAX4210CETT	-40°C to +85°C	6 TDFN-6-EP* (3mm x 3mm)	AHH
MAX4210CEUA	-40°C to +85°C	8 μMAX	—
MAX4210DETT	-40°C to +85°C	6 TDFN-6-EP* (3mm x 3mm)	AHI
MAX4210DEUA	-40°C to +85°C	8 μMAX	—
MAX4210EETT	-40°C to +85°C	6 TDFN-6-EP* (3mm x 3mm)	AHJ
MAX4210EEUA	-40°C to +85°C	8 μMAX	—
MAX4210FETT	-40°C to +85°C	6 TDFN-6-EP* (3mm x 3mm)	AHK
MAX4210FEUA	-40°C to +85°C	8 μMAX	—
MAX4211AETE	-40°C to +85°C	16 Thin QFN-EP* (4mm x 4mm)	—
MAX4211AEUE	-40°C to +85°C	16 TSSOP	—
MAX4211BETE	-40°C to +85°C	16 Thin QFN-EP* (4mm x 4mm)	—
MAX4211BEUE	-40°C to +85°C	16 TSSOP	—
MAX4211CETE	-40°C to +85°C	16 Thin QFN-EP* (4mm x 4mm)	—
MAX4211CEUE	-40°C to +85°C	16 TSSOP	—
MAX4211DETE	-40°C to +85°C	16 Thin QFN-EP* (4mm x 4mm)	—
MAX4211DEUE	-40°C to +85°C	16 TSSOP	—
MAX4211EETE	-40°C to +85°C	16 Thin QFN-EP* (4mm x 4mm)	—
MAX4211EEUE	-40°C to +85°C	16 TSSOP	—
MAX4211FETE	-40°C to +85°C	16 Thin QFN-EP* (4mm x 4mm)	—
MAX4211FEUE	-40°C to +85°C	16 TSSOP	—

**EP = Exposed paddle.*

Chip Information

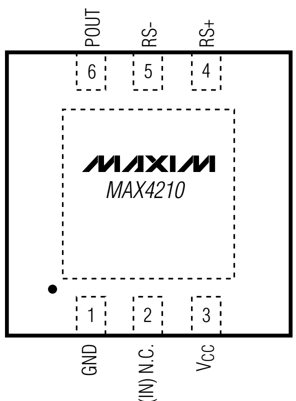
MAX4210 TRANSISTOR COUNT: 515

MAX4211 TRANSISTOR COUNT: 1032

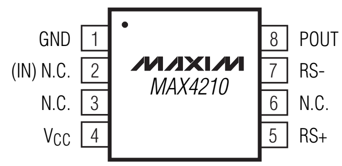
PROCESS: BiCMOS

Pin Configurations

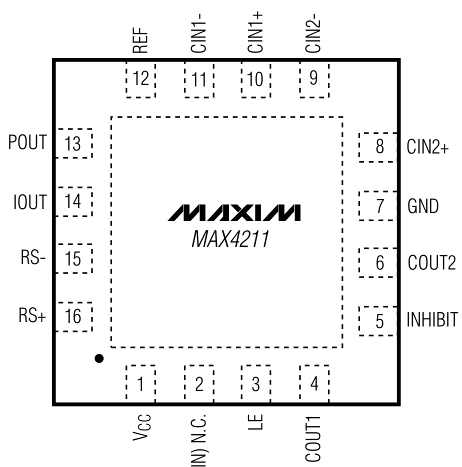
TOP VIEW



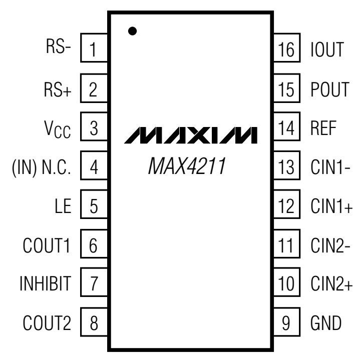
3mm x 3mm TDFN



µMAX



4mm x 4mm THIN QFN

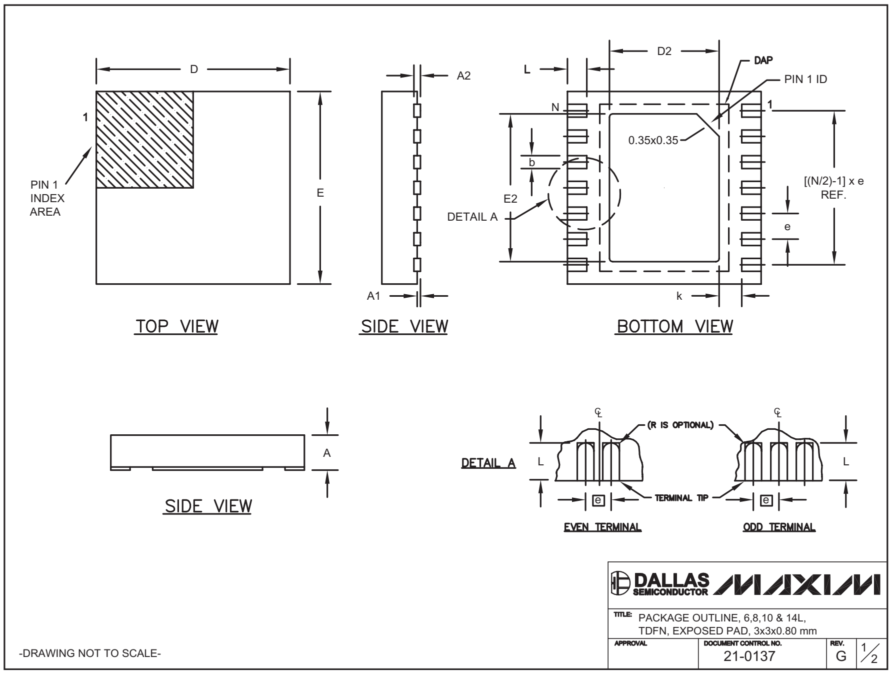


TSSOP

( ) ARE FOR MAX421_D/E/F.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS

PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF	NO
T633-2	6	1.50–0.10	2.30–0.10	0.95 BSC	MO229 / WEEA	0.40–0.05	1.90 REF	NO
T833-1	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF	NO
T833-2	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF	NO
T833-3	8	1.50–0.10	2.30–0.10	0.65 BSC	MO229 / WEEC	0.30–0.05	1.95 REF	YES
T1033-1	10	1.50–0.10	2.30–0.10	0.50 BSC	MO229 / WEED-3	0.25–0.05	2.00 REF	NO
T1433-1	14	1.70–0.10	2.30–0.10	0.40 BSC	- - - -	0.20–0.05	2.40 REF	YES
T1433-2	14	1.70–0.10	2.30–0.10	0.40 BSC	- - - -	0.20–0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

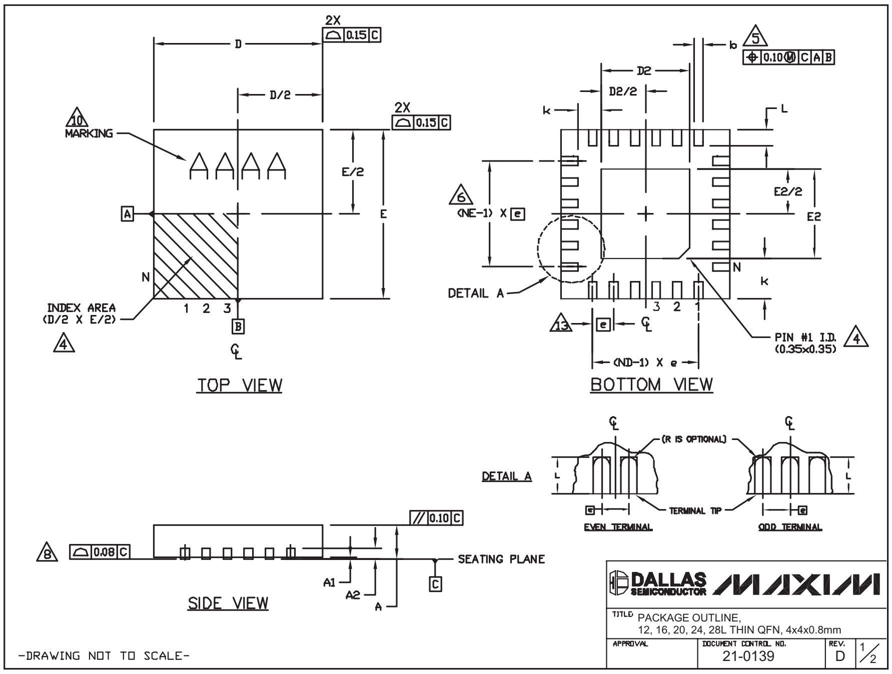
APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. G | 2/2

-DRAWING NOT TO SCALE-

NOTE: *THE TDFN EXPOSED PADDLE SIZE-VARIATION PACKAGE CODE: T633-1*

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS															
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm
12. WARPAGE SHALL NOT EXCEEND 0.10mm
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 12, 16, 20, 24, 28L THIN QFN, 4x4x0.8mm

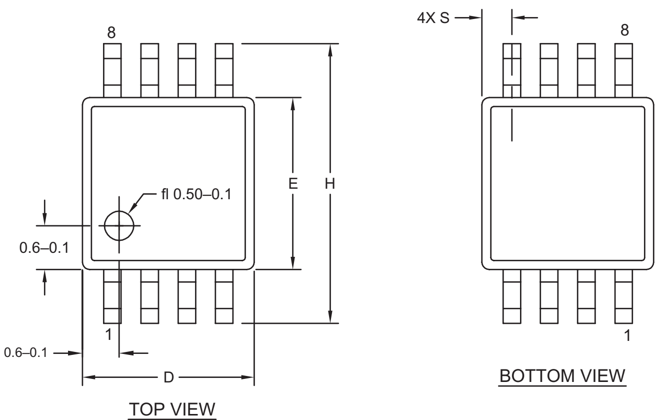
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV. D | 2/2

-DRAWING NOT TO SCALE-

NOTE: *THE THIN QFN EXPOSED PADDLE SIZE-VARIATION PACKAGE CODE: T1644-4*

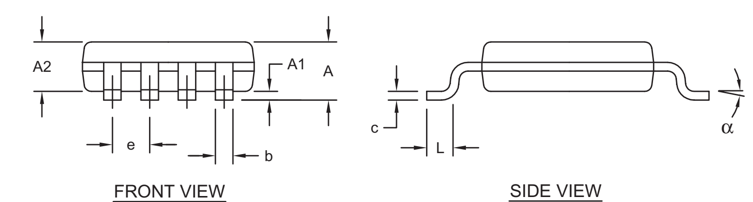
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0	6	0	6
S	0.0207 BSC		0.5250 BSC	

8LUMAXD.EPS



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

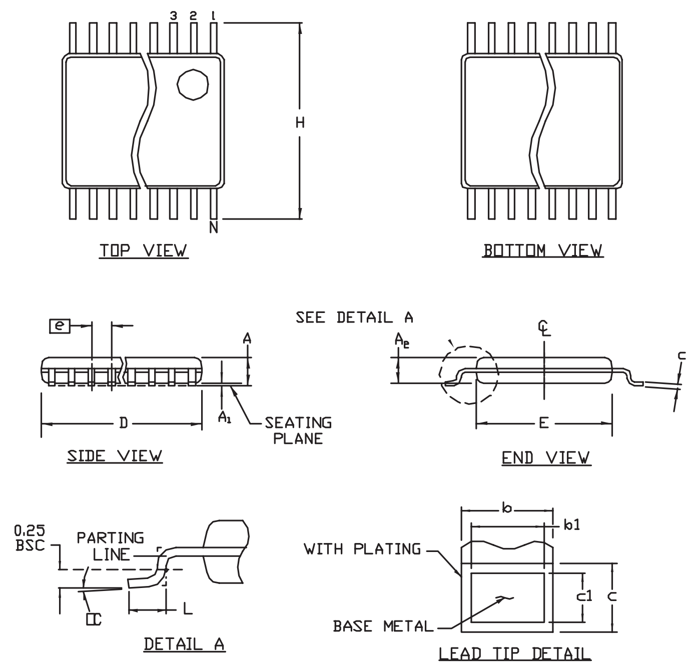
PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

High-Side Power and Current Monitors

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS

TSSOP4.40mm.EPS