No R_{SENSE}™ Electronic Circuit Breaker

FEATURES

- **Fast 1µs Response Circuit Breaker**
- **3 Selectable Circuit Breaker Thresholds**
- **No Sense Resistor Required**
- **Dual Level Overcurrent Fault Protection**
- **Controls Load Voltages from 0V to 6V**
- High-Side Drive for External N-Channel MOSFET
- Undervoltage Lockout
- READY Pin Signals When Circuit Breaker Armed
- Small Plastic (3mm × 2mm) DFN and TSOT-23 (ThinSOT™) Packages

APPLICATIONS

- Electronic Circuit Breaker
- High-Side Switch
- Hot Board Insertion

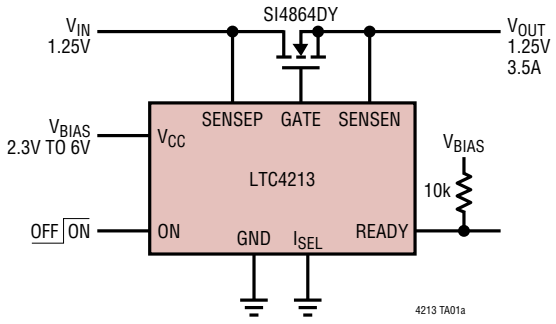
DESCRIPTION

The LTC®4213 is an electronic circuit breaker. An overcurrent circuit breaker senses the voltage across the drain and source terminals of an external N-channel MOSFET with no need for a sense resistor. The advantages are a lower cost and reduced voltage and power loss in the switch path. An internal high-side driver controls the external MOSFET gate.

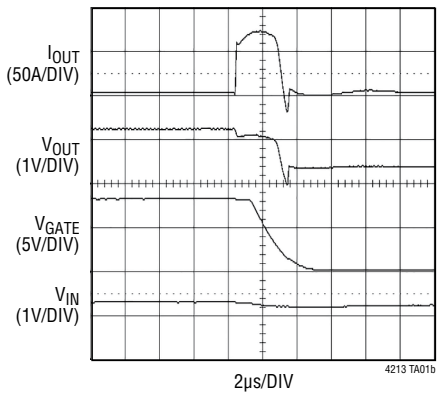
Two integrated comparators provide dual level overcurrent protection over the bias supply to ground common mode range. The slow comparator has 16µs response while the fast comparator trips in 1µs. The circuit breaker has three selectable trip thresholds: 25mV, 50mV and 100mV. An ON pin controls the ON/OFF and resets circuit breaker faults. READY signals the MOSFET is conducting and the circuit breaker is armed. The LTC4213 operates from V_{CC} = 2.3V to 6V.

TYPICAL APPLICATION

1.25V Electronic Circuit Breaker



Severe Overload Response



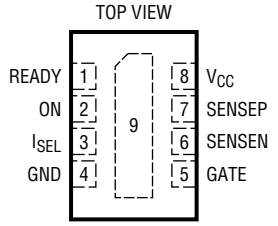
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Bias Supply Voltage (V_{CC}) ..... –0.3V to 9V
Input Voltages
ON, SENSEP, SENSEN ..... –0.3V to 9V
I_{SEL} ..... –0.3V to (V_{CC} + 0.3V)
Output Voltages
GATE ..... –0.3V to 15V
READY ..... –0.3V to 9V

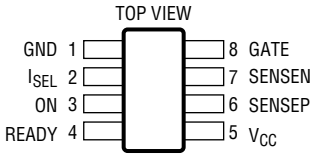
Operating Temperature Range
LTC4213C ..... 0°C to 70°C
LTC4213I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 250°C/W
EXPOSED PAD (PIN 9) PCB CONNECTION OPTIONAL



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 125°C, θ_{JA} = 195°C/W

ORDER INFORMATION

TAPE AND REEL	TAPE AND REEL (MINI)	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4213CDDB#TRPBF	N/A	LBHV	8-Lead (3mm × 2mm) Plastic DFN	0°C to 70°C
LTC4213IDDB#TRPBF	N/A	LBHV	8-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC4213CTS8#TRPBF	LTC4213CTS8#TRMPBF	LTHQB	8-Lead Plastic TSOT-23	0°C to 70°C
LTC4213ITS8#TRPBF	LTC4213ITS8#TRMPBF	LTHQB	8-Lead Plastic TSOT-23	–40°C to 85°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, I_{SEL} = 0 unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Bias Supply Voltage		●	2.3		6	V
V_{SENSEP}	SENSEP Voltage		●	0		6	V
I_{CC}	V_{CC} Supply Current		●		1.6	3	mA
$V_{CC(UVLR)}$	V_{CC} Undervoltage Lockout Release	V_{CC} Rising	●	1.8	2.07	2.23	V
$\Delta V_{CC(UVHYST)}$	V_{CC} Undervoltage Lockout Hysteresis		●	30	100	160	mV
I_{SENSEP}	SENSEP Input Current	V_{SENSEP} = V_{SENSEN} = 5V, Normal Mode		15	40	80	µA
		V_{SENSEP} = V_{SENSEN} = 0, Normal Mode			–1	±15	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, I_{SEL} = 0 unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SENSEN}	SENSEN Input Current	$V_{SENSEP} = V_{SENSEN}$ = 5V, Normal Mode		15	40	80	µA
		$V_{SENSEP} = V_{SENSEN}$ = 0, Normal Mode			–1	±15	µA
		$V_{SENSEP} = V_{SENSEN}$ = 5V, Reset Mode or Fault Mode		50	280		µA
V_{CB}	Circuit Breaker Trip Voltage $V_{CB} = V_{SENSEP} – V_{SENSEN}$	I_{SEL} = 0, $V_{SENSEP} = V_{CC}$	●	22.5	25	27.5	mV
		I_{SEL} = Floated, $V_{SENSEP} = V_{CC}$	●	45	50	55	mV
		$I_{SEL} = V_{CC}$, $V_{SENSEP} = V_{CC}$	●	90	100	110	mV
$V_{CB(FAST)}$	Fast Circuit Breaker Trip Voltage $V_{CB(FAST)} = V_{SENSEP} – V_{SENSEN}$	I_{SEL} = 0, $V_{SENSEP} = V_{CC}$	●	63	100	115	mV
		I_{SEL} = Floated, $V_{SENSEP} = V_{CC}$	●	126	175	200	mV
		$I_{SEL} = V_{CC}$, $V_{SENSEP} = V_{CC}$	●	252	325	371	mV
$I_{GATE(UP)}$	GATE Pin Pull Up Current	V_{GATE} = 0V	●	–50	–100	–150	µA
$I_{GATE(DN)}$	GATE Pin Pull Down Current	$\Delta V_{SENSEP} – V_{SENSEN}$ = 200mV, V_{GATE} = 8V	●	10	40		mA
ΔV_{GSMAX}	External N-Channel Gate Drive	V_{SENSEN} = 0, $V_{CC} \geq$ 2.97V, I_{GATE} = –1µA	●	4.8	6.5	8	V
		V_{SENSEN} = 0, V_{CC} = 2.3V, I_{GATE} = –1µA	●	2.65	4.3	8	V
ΔV_{GSARM}	V_{GS} Voltage to Arm Circuit Breaker	V_{SENSEN} = 0, $V_{CC} \geq$ 2.97V	●	4.4	5.4	7.6	V
		V_{SENSEN} = 0, V_{CC} = 2.3V	●	2.5	3.5	7	V
$\Delta V_{GSMAX} – \Delta V_{GSARM}$	Difference Between ΔV_{GSMAX} and ΔV_{GSARM}	V_{SENSEN} = 0, $V_{CC} \geq$ 2.97V	●	0.3	1.1		V
		V_{SENSEN} = 0, V_{CC} = 2.3V	●	0.15	0.8		V
$V_{READY(OL)}$	READY Pin Output Low Voltage	I_{READY} = 1.6mA, Pull-Down Device On	●		0.2	0.4	V
$I_{READY(LEAK)}$	READY Pin Leakage Current	V_{READY} = 5V, Pull-Down Device Off	●		0	±1	µA
$V_{ON(TH)}$	ON Pin High Threshold	ON Rising, GATE Pulls Up	●	0.76	0.8	0.84	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis	ON Falling, GATE Pulls Down		10	40	90	mV
$V_{ON(RST)}$	ON Pin Reset Threshold	ON Falling, Fault Reset, GATE Pull-Down	●	0.36	0.4	0.44	V
$I_{ON(IN)}$	ON Pin Input Current	V_{ON} = 1.2V	●		0	±1	µA
ΔV_{OV}	Overvoltage Threshold, $\Delta V_{OV} = V_{SENSEP} – V_{CC}$		●	0.41	0.7	1.1	V
t_{OV}	Overvoltage Protection Trip Time	$V_{SENSEP} = V_{SENSEN}$ = Step 5V to 6.2V		25	65	160	µs
$t_{FAULT(SLOW)}$	V_{CB} Trips to GATE Discharging	ΔV_{SENSE} Step 0mV to 50mV, V_{SENSEN} Falling, $V_{CC} = V_{SENSEP}$ = 5V	●	7	16	27	µs
$t_{FAULT(FAST)}$	$V_{CB(FAST)}$ Trips to GATE Discharging	ΔV_{SENSE} Step 0V to 0.3V, V_{SENSEN} Falling, V_{SENSEP} = 5V	●		1	2.5	µs
$t_{DEBOUNCE}$	Startup De-Bounce Time	V_{ON} = 0V to 2V Step to Gate Rising (Exiting Reset Mode)		27	60	130	µs
t_{READY}	READY Delay Time	V_{GATE} = 0V to 8V Step to READY Rising, $V_{SENSEP} = V_{SENSEN}$ = 0		22	50	115	µs
t_{OFF}	Turn-Off Time	V_{ON} = 2V to 0.6V Step to GATE Discharging		1.5	5	10	µs
t_{ON}	Turn-On Time	V_{ON} = 0.6V to 2V Step to GATE Rising (Normal Mode)		4	8	16	µs
t_{RESET}	Reset Time	V_{ON} Step 2V to 0V		20	80	150	µs

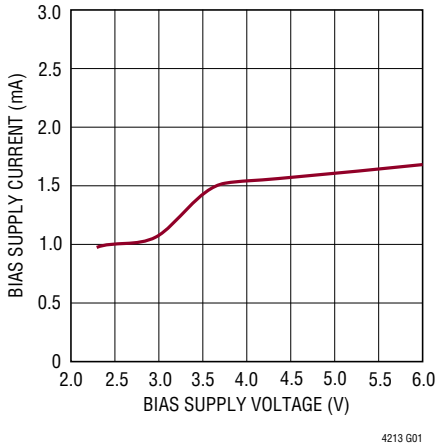
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

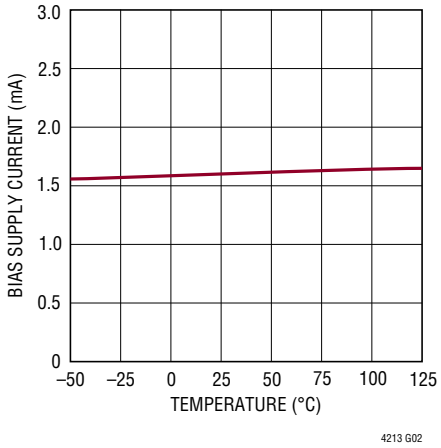
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = 5V unless otherwise noted.

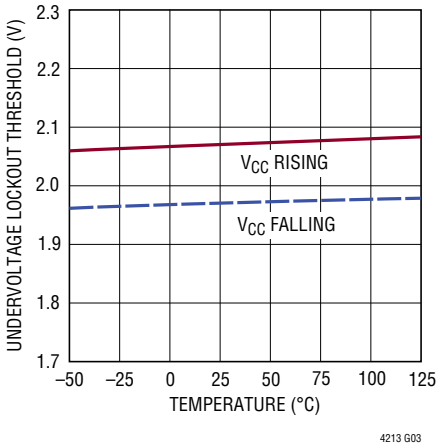
I_{CC} vs V_{CC}



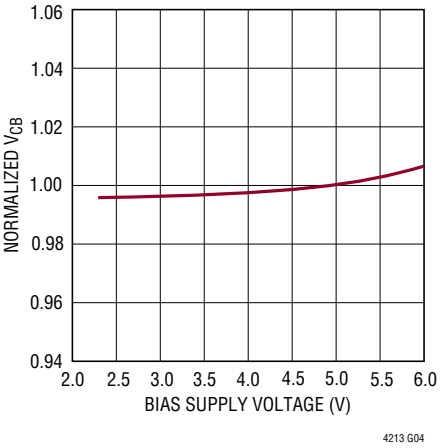
I_{CC} vs Temperature



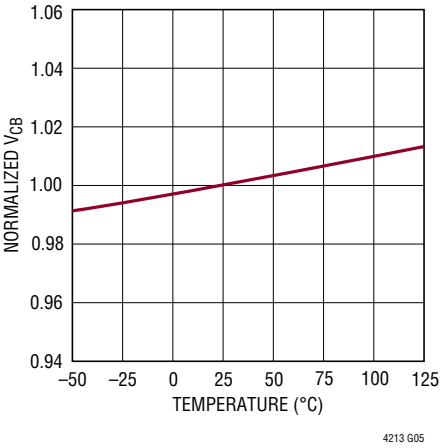
$V_{CC(UVLR)}$ vs Temperature



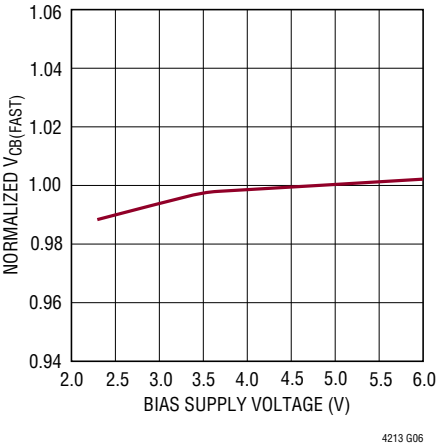
Normalized V_{CB} vs V_{CC}



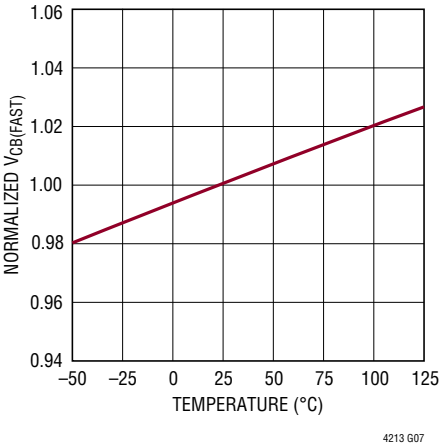
Normalized V_{CB} vs Temperature



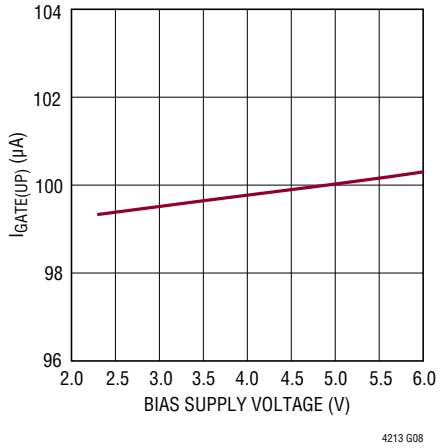
Normalized $V_{CB(FAST)}$ vs V_{CC}



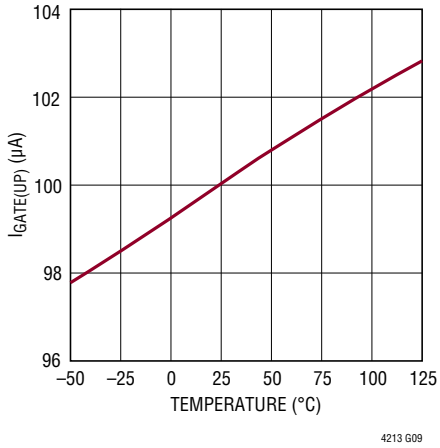
Normalized $V_{CB(FAST)}$ vs Temperature



$I_{GATE(UP)}$ vs V_{CC}



$I_{GATE(UP)}$ vs Temperature

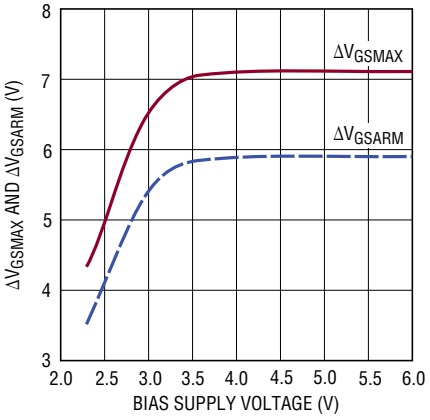


Rev. A

TYPICAL PERFORMANCE CHARACTERISTICS

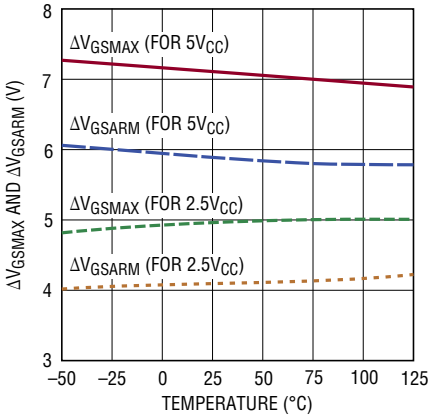
T_A = 25°C. V_{CC} = 5V unless otherwise noted.

ΔV_{GSMAX} and ΔV_{GSARM} vs V_{CC}



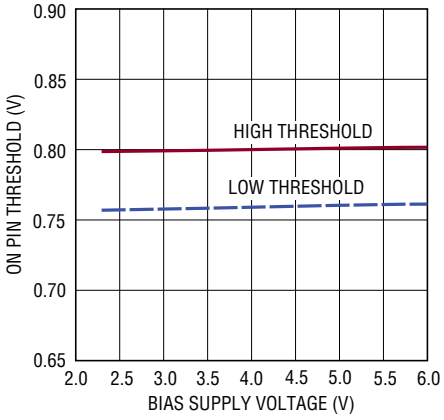
4213 G10

ΔV_{GSMAX} and ΔV_{GSARM} vs Temperature



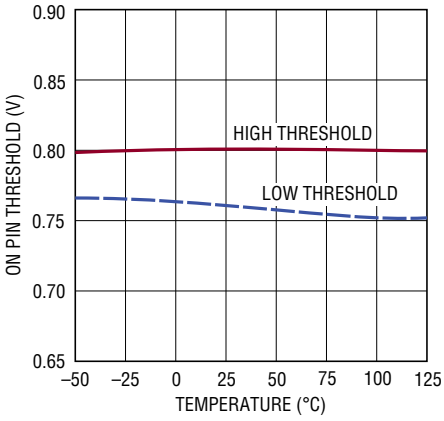
4213 G11

$V_{ON(TH)}$ vs V_{CC}



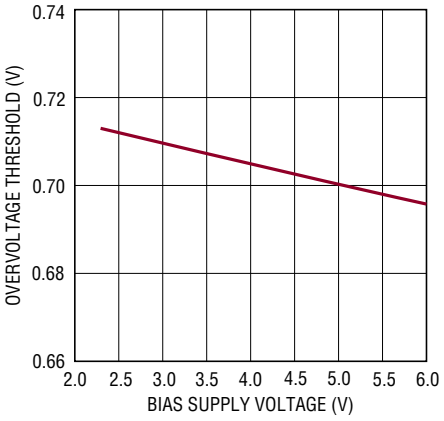
4213 G12

$V_{ON(TH)}$ vs Temperature



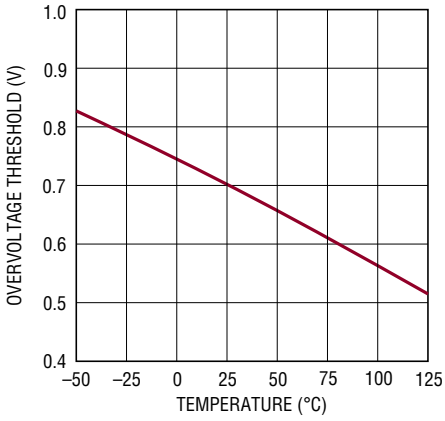
4213 G13

ΔV_{OV} vs V_{CC}



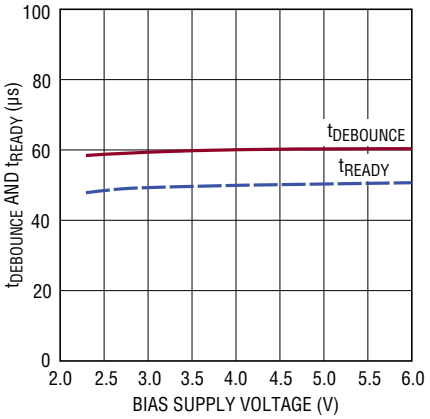
4213 G14

ΔV_{OV} vs Temperature



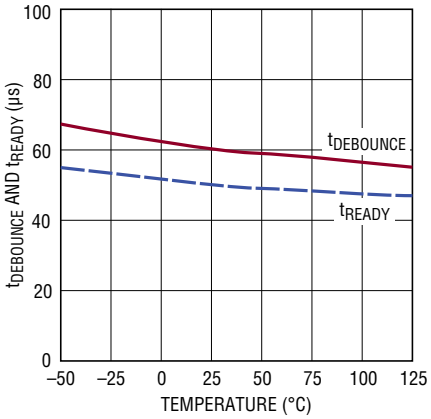
4213 G15

$t_{DEBOUNCE}$ and t_{READY} vs V_{CC}



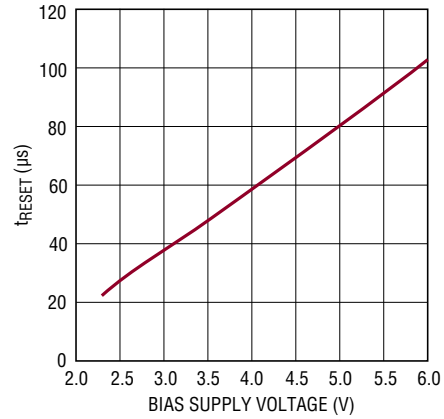
4213 G16

$t_{DEBOUNCE}$ and t_{READY} vs Temperature



4213 G17

t_{RESET} vs V_{CC}

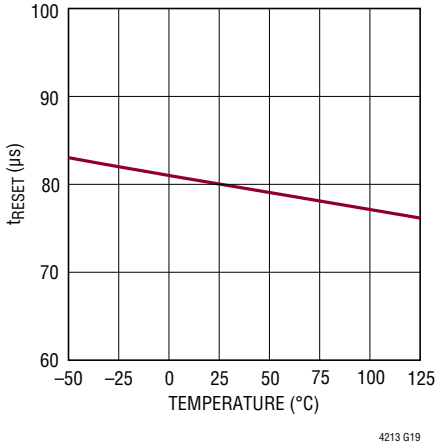


4213 G18

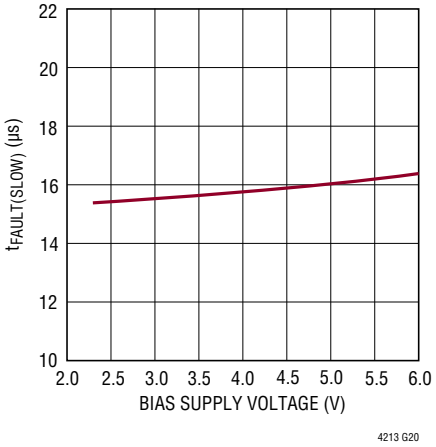
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C. V_{CC} = 5V unless otherwise noted.

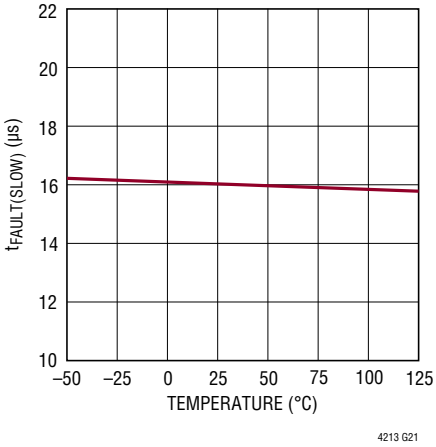
t_{RESET} vs Temperature



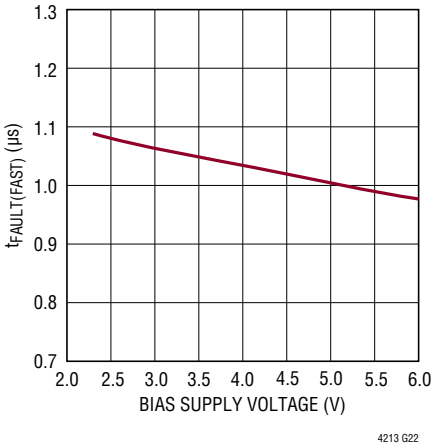
$t_{FAULT(SLOW)}$ vs V_{CC}



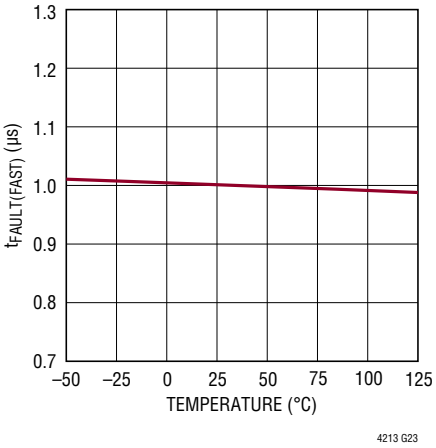
$t_{FAULT(SLOW)}$ vs Temperature



$t_{FAULT(FAST)}$ vs V_{CC}



$t_{FAULT(FAST)}$ vs Temperature



PIN FUNCTIONS (DFN/TSOT-23)

Exposed Pad (Pin 9, DDB Package Only): Exposed pad may be left open or connected to device ground.

GATE (Pin 5/Pin 8): GATE Drive Output. An internal charge pump supplies 100µA pull-up current to the gate of the external N-channel MOSFET. Internal circuitry limits the voltage between the GATE and SENSEN pins to a safe gate drive voltage of less than 8V. When the circuit breaker trips, the GATE pin abruptly pulls to GND.

GND (Pin 4/Pin 1): Device Ground.

I_{SEL} (Pin 3/Pin 2): Threshold Select Input. With the I_{SEL} pin grounded, float or tied to V_{CC} the V_{CB} is set to 25mV, 50mV or 100mV, respectively. The corresponding $V_{CB(FAST)}$ values are 100mV, 175mV and 325mV.

ON (Pin 2/Pin 3): ON Control Input. The LTC4213 is in reset mode when the ON pin is below 0.4V. When the ON pin increases above 0.8V, the device starts up and the GATE pulls up with a 100µA current source. When the ON pin drops below 0.76V, the GATE pulls down. To reset a circuit breaker fault, the ON pin must go below 0.4V.

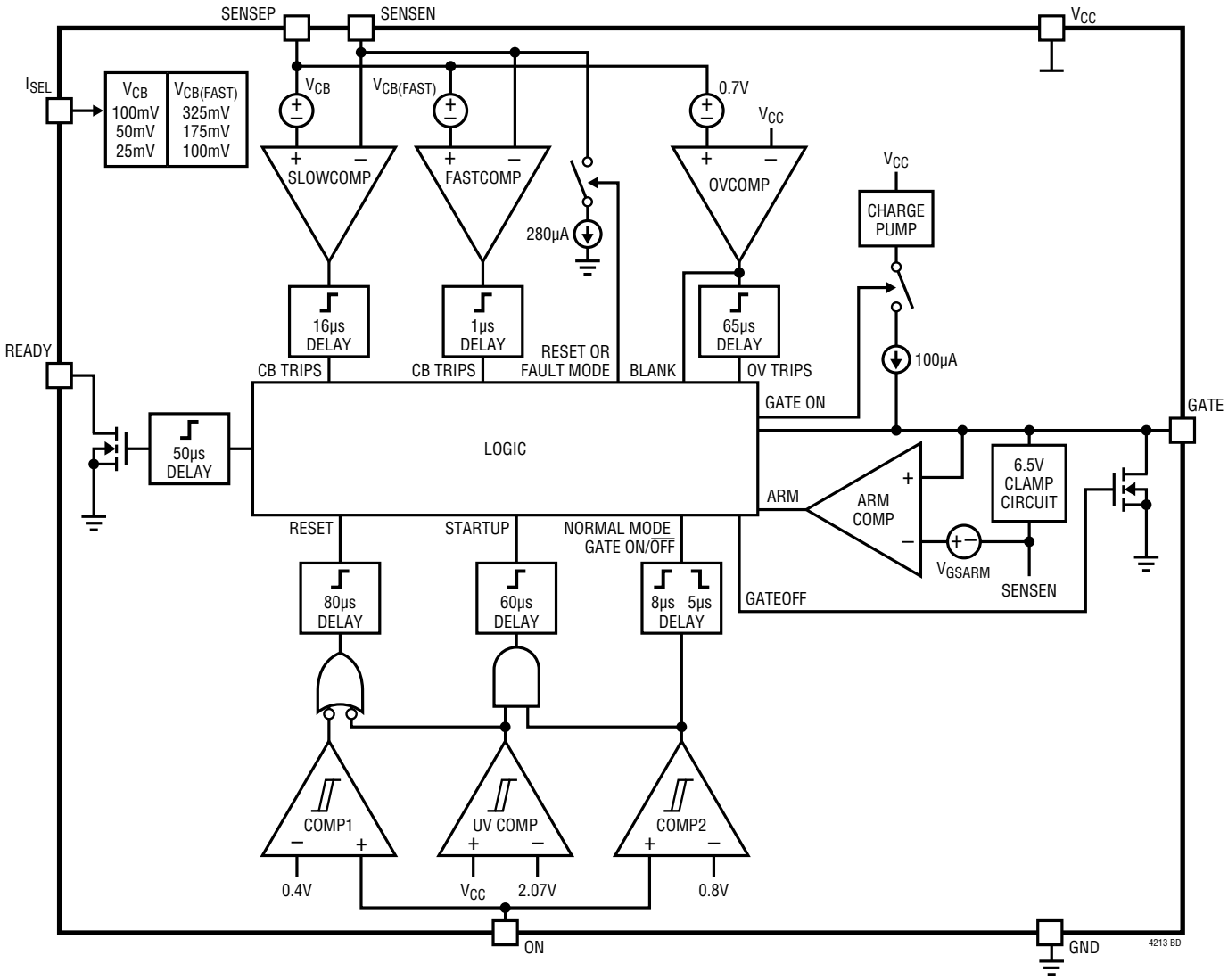
READY (Pin 1/Pin 4): READY Status Output. Open-drain output that goes high impedance when the external MOSFET is on and the circuit breaker is armed. Otherwise this pin pulls low.

SENSEN (Pin 6/Pin 7): Circuit Breaker Negative Sense Input. Connect this pin to the source of the external MOSFET. During reset or fault mode, the SENSEN pin discharges the output to ground with 280µA.

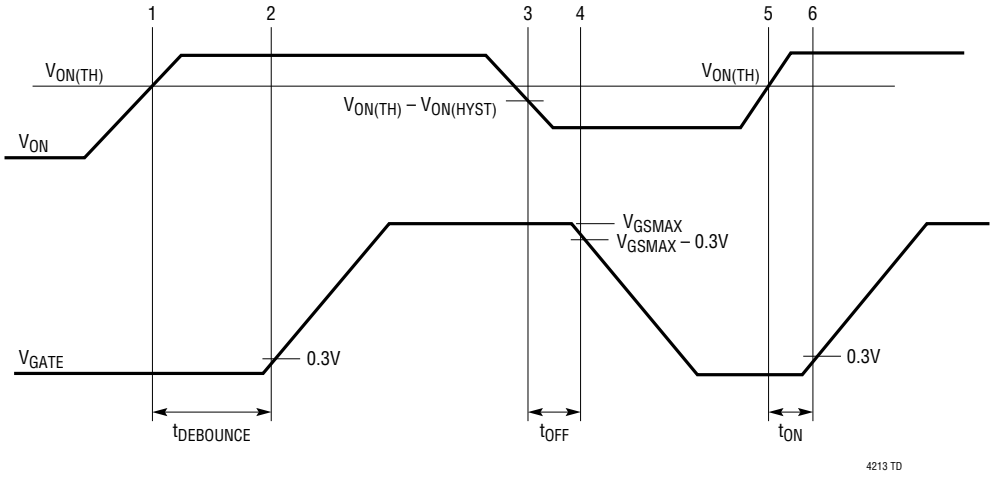
SENSEP (Pin 7/Pin 6): Circuit Breaker Positive Sense Input. Connect this pin to the drain of external N-channel MOSFET. The circuit breaker trips when the voltage across SENSEP and SENSEN exceeds V_{CB}. The input common mode range of the circuit breaker is from ground to V_{CC} + 0.2V when $V_{CC} < 2.5V$. For $V_{CC} \geq 2.5V$, the input common mode range is from ground to V_{CC} + 0.4V.

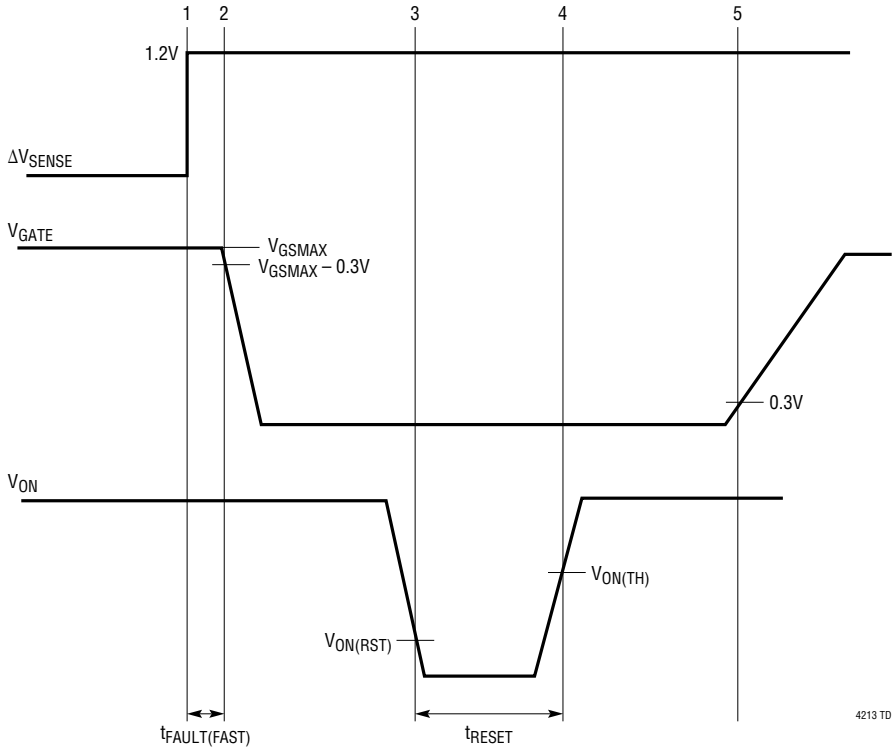
V_{CC} (Pin 8/Pin 5): Bias Supply Voltage Input. Normal operation is between 2.3V and 6V. An internal under-voltage lockout circuit disables the device when $V_{CC} < 2.07V$.

BLOCK DIAGRAM



TIMING DIAGRAM





OPERATION

Overview

The LTC4213 is an electronic circuit breaker (ECB) that senses load current with the the $R_{DS(ON)}$ of the external MOSFET instead of using an external sense resistor. This No R_{SENSE} method is less precise than R_{SENSE} method due to the variation of $R_{DS(ON)}$. However, the advantages are less complex, lower cost and reduce voltage and power loss in the switch path owing to the absence of a sense resistor. Without the external sense resistor voltage drop, the V_{OUT} improvement can be quite significant especially in the low voltage applications. The LTC4213 is designed to operate over a bias supply range from 2.3V to 6V. When bias supply voltage and the ON pin are sufficiently high, the GATE pin starts charging after an internal debounce delay of 60µs. During the GATE ramp-up, the circuit breaker is not armed until the external MOSFET is fully turned on. Once the circuit breaker is armed, the LTC4213 monitors the load current through the $R_{DS(ON)}$ of the external MOSFET.

Circuit Breaker Function

The LTC4213 provides dual level and dual response time circuit breaker functions for overcurrent protection.

The LTC4213 circuit breaker function block consists of two comparators, SLOWCOMP and FASTCOMP. The thresholds of SLOWCOMP and FASTCOMP are V_{CB} and $V_{CB(FAST)}$. The I_{SEL} pin selects one of the three settings:

1. V_{CB} = 25mV and $V_{CB(FAST)}$ = 100mV with I_{SEL} at GND
2. V_{CB} = 50mV and $V_{CB(FAST)}$ = 175mV with ISEL floating
3. V_{CB} = 100mV and $V_{CB(FAST)}$ = 325mV with I_{SEL} at V_{CC}

I_{SEL} can be stepped dynamically, such as to allow a higher circuit breaker threshold at startup and a lower threshold after supply current has settled. The inputs of the comparators are SENSEP and SENSEN pins. The voltage across the drain and source of the external MOSFET is sensed at SENSEP and SENSEN.

$$\Delta V_{SENSE} = V_{SENSEP} - V_{SENSEN} \quad (1)$$

When ΔV_{SENSE} exceeds the V_{CB} threshold but is less than $V_{CB(FAST)}$, the comparator SLOWCOMP trips the circuit breaker after a 16µs delay. If ΔV_{SENSE} is greater than $V_{CB(FAST)}$, the comparator FASTCOMP trips the circuit breaker in 1µs.

A severe short circuit condition can cause the load supply to dip substantially. This does not pose a problem for the LTC4213 as the input stages of the current limit comparators are common mode to ground.

APPLICATIONS INFORMATION

Figure 1 shows an electronic circuit breaker (ECB) application. An external auxiliary supply biases the V_{CC} pin and the internal circuitry. A V_{IN} load supply powers the load via an external MOSFET. The SENSEP and SENSEN pins sense the load current at the drain and source of the external MOSFET. In ECB applications, large input bypass capacitors are usually recommended for good transient performance.

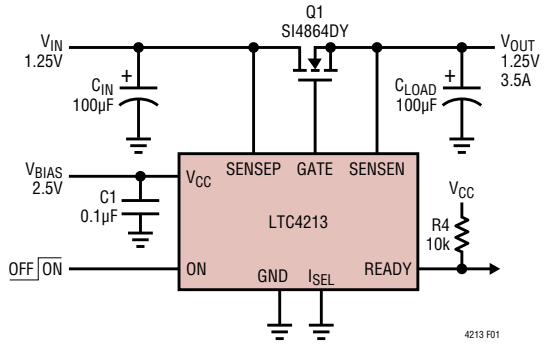


Figure 1. LTC4213 Electronic Circuit Breaker Application

Undervoltage Lockout

An internal undervoltage lockout (UVLO) circuit resets the LTC4213 if the V_{CC} supply is too low for normal operation. The UVLO comparator (UVCOMP) has a low-to-high threshold of 2.07V and 100mV of hysteresis. UVLO shares the glitch filters for both low-to-high transition (startup) and high-to-low transition (reset) with the ON pin comparators. Above 2.07V bias supply voltage, the LTC4213 starts if the ON pin conditions are met. Short, shallow bus bias supply transient dips below 1.97V of less than 80µs are ignored.

APPLICATIONS INFORMATION

ON Function

When V_{ON} is below comparator COMP1's threshold of 0.4V for 80µs, the device resets. The system leaves reset mode if the ON pin rises above comparator COMP2's threshold of 0.8V and the UVLO condition is met. Leaving reset mode, the GATE pin starts up after a $t_{DEBOUNCE}$ delay of 60µs. When ON goes below 0.76V, the GATE shuts off after a 5µs glitch filter delay. The output is discharged by the external load when V_{ON} is in between 0.4V to 0.8V. At this state, the ON pin can re-enable the GATE if V_{ON} exceeds 0.8V for more than 8µs. Alternatively, the device resets if the ON pin is brought below 0.4V for 80µs. Once reset, the GATE pin restarts only after the $t_{DEBOUNCE}$ 60µs delay at V_{ON} rising above 0.8V. To protect the ON pin from overvoltage stress due to supply transients, a series resistor of greater than 10k is recommended when the ON pin is connected directly to the supply. An external resistive divider at the ON pin can be used with COMP2 to set a supply undervoltage lockout value higher than the internal UVLO circuit. An RC filter can be implemented at the ON pin to increase the power-up delay time beyond the internal 60µs delay.

Gate Function

The GATE pin is held low in reset mode. 60µs after leaving reset mode, the GATE pin is charged up by an internal 100µA current source. The circuit breaker arms when $V_{GATE} > V_{SENSEN} + \Delta_{VGSARM}$. In normal mode operation, the GATE peak voltage is internally clamped to ΔV_{GSMAX} above the SENSEN pin. When the circuit breaker trips, an internal MOSFET shorts the GATE pin to GND, turning off the external MOSFET.

READY Status

The READY pin is held low during reset and at startup. It is pulled high by an external pull-up resistor 50µs after the circuit breaker arms. The READY pin pulls low if the circuit breaker trips or the ON pin is pulled below 0.76V, or V_{CC} drops below undervoltage lockout.

ΔV_{GSARM} and V_{GSMAX}

Each MOSFET has a recommended V_{GS} drive voltage where the channel is deemed fully enhanced and $R_{DS(ON)}$ is minimized. Driving beyond this recommended V_{GS} voltage yields a marginal decrease in $R_{DS(ON)}$. At start-up, the gate voltage starts at ground potential. The GATE ramps past the MOSFET threshold and the load current begins to flow. When V_{GS} exceeds ΔV_{GSARM}, the circuit breaker is armed and enabled. The chosen MOSFET should have a recommended minimum V_{GS} drive level that is lower than ΔV_{GSARM}. Finally, V_{GS} reaches a maximum at ΔV_{GSMAX}.

Trip and Reset Circuit Breaker

Figure 2 shows the timing diagram of V_{GATE} and V_{READY} after a fault condition. A tripped circuit breaker can be reset either by cycling the V_{CC} bias supply below UVLO threshold or pulling ON below 0.4V for $>t_{RESET}$. Figure 3 shows the timing diagram for a tripped circuit breaker being reset by the ON pin.

Calculating Current Limit

The fault current limit is determined by the $R_{DS(ON)}$ of the MOSFET and the circuit breaker voltage V_{CB}.

$$I_{LIMIT} = \frac{V_{CB}}{R_{DS(ON)}} \quad (2)$$

The $R_{DS(ON)}$ value depends on the manufacturer's distribution, V_{GS} and junction temperature. Short Kelvin-sense connections between the MOSFET drain and source to the LTC4213 SENSEP and SENSEN pins are strongly recommended.

For a selected MOSFET, the nominal load limit current is given by:

$$I_{LIMIT(NOM)} = \frac{V_{CB(NOM)}}{R_{DS(ON)(NOM)}} \quad (3)$$

The minimum load limit current is given by:

$$I_{LIMIT(MIN)} = \frac{V_{CB(MIN)}}{R_{DS(ON)(MAX)}} \quad (4)$$

The maximum load limit current is given by:

APPLICATIONS INFORMATION

$$I_{LIMIT(MAX)} = \frac{V_{CB(MAX)}}{R_{DS(ON)(MIN)}} \quad (5)$$

Most MOSFET data sheets have an $R_{DS(ON)}$ specification with typical and maximum values but no minimum value. Assuming a normal distribution with typical as mean, the minimum value can be estimated as:

$$R_{DS(ON)(MIN)} = 2 \bullet R_{DS(ON)(NOM)} - R_{DS(ON)(MAX)} \quad (6)$$

The LTC4213 gives higher gate drive than the manufacturer specified gate drive for $R_{DS(ON)}$ This gives a slightly lower $R_{DS(ON)}$ than specified. Operating temperature also modulates the $R_{DS(ON)}$ value.

Example Current Limit Calculation

An Si4410DY is used for current detection in a 5V supply system with the LTC4213 V_{CB} at 25mV (I_{SEL} pin grounded).

The $R_{DS(ON)}$ distribution for the Si4410DY is:

Typical $R_{DS(ON)} = 0.015\Omega = 100\%$

Maximum $R_{DS(ON)} = 0.02\Omega = 133.3\%$

Estimated MIN $R_{DS(ON)} = 2 \bullet 15 - 20 = 0.010\Omega = 66.7\%$

The $R_{DS(ON)}$ variation due to gate drive is:

$R_{DS(ON)}$ @ $4.5V_{GS} = 0.015\Omega = 100\%$ (spec. TYP)

$R_{DS(ON)}$ @ $4.8V_{GS} = 0.014\Omega = 93\%$ (MIN ΔV_{GSMAX})

$R_{DS(ON)}$ @ $7V_{GS} = 0.0123\Omega = 82\%$ (NOM ΔV_{GSMAX})

$R_{DS(ON)}$ @ $8V_{GS} = 0.012\Omega = 80\%$ (MAX ΔV_{GSMAX})

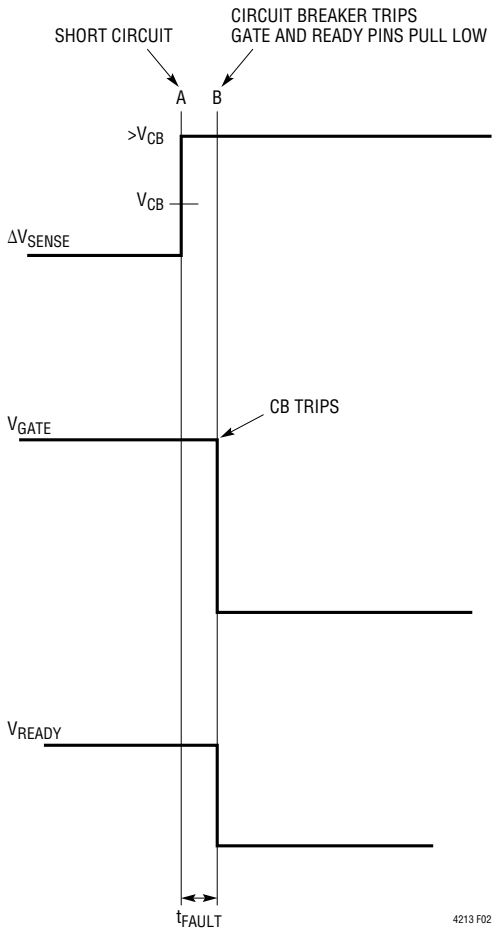


Figure 2. Short Circuit Fault Timing Diagram

APPLICATIONS INFORMATION

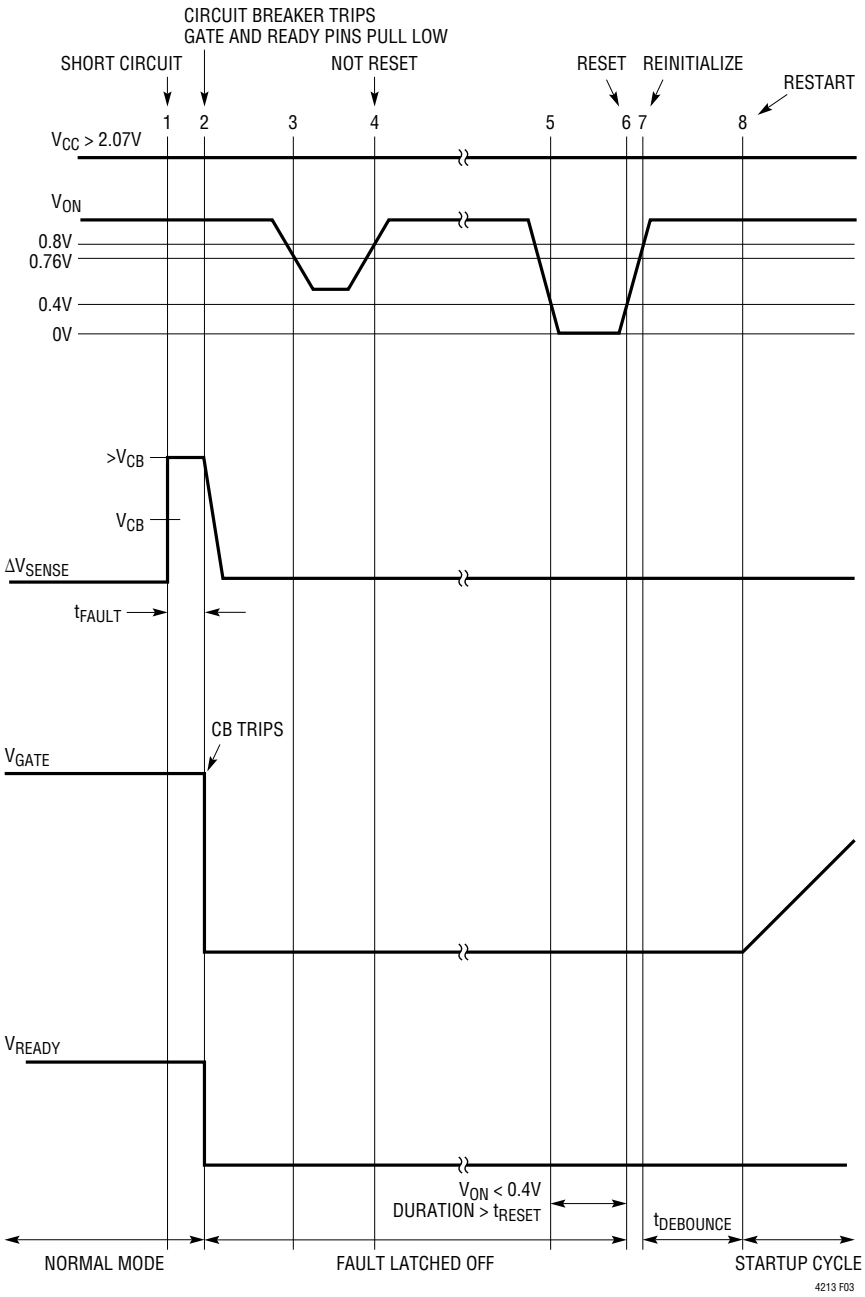


Figure 3. Resetting Fault Timing Diagram

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Operating temperature of 0° to 70°C.

$R_{DS(ON)}$ at 25°C = 100%

$R_{DS(ON)}$ at 0°C = 90%

$R_{DS(ON)}$ at 70°C = 120%

MOSFET resistance variation:

$R_{DS(ON)(NOM)}$ = 15m • 0.82 = 12.3mΩ

$R_{DS(ON)(MAX)}$ = 15m • 1.333 • 0.93 • 1.2 = 15m • 1.488 = 22.3mΩ

$R_{DS(ON)(MIN)}$ = 15m • 0.667 • 0.80 • 0.90 = 15m • 0.480 = 7.2mΩ

V_{CB} variation:

NOM V_{CB} = 25mV = 100%

MIN V_{CB} = 22.5mV = 90%

MAX V_{CB} = 27.5mV = 110%

The current limits are:

$I_{LIMIT(NOM)}$ = 25mV/12.3mΩ = 2.03A

$I_{LIMIT(MIN)}$ = 22.5mV/22.3mΩ = 1.01A

ILIMIT(MAX) = 27.5mV/7.2mΩ = 3.82A

For proper operation, the minimum current limit must exceed the circuit maximum operating load current with margin. So this system is suitable for operating load current up to 1A. From this calculation, we can start with the general rule for MOSFET $R_{DS(ON)}$ by assuming maximum operating load current is roughly half of the $I_{LIMIT(NOM)}$. Equation 7 shows the rule of thumb.

$$I_{OPMAX} = \frac{V_{CB(NOM)}}{2 \bullet R_{DS(ON)(NOM)}} \quad (7)$$

Note that the $R_{DS(ON)(NOM)}$ is at the LTC4213 nominal operating ΔV_{GSMAX} rather than at typical vendor spec. Table 1 gives the nominal operating ΔV_{GSMAX} at the various operating V_{CC}. From this table users can refer to the MOSFET's data sheet to obtain the $R_{DS(ON)(NOM)}$ value.

Table 1. Nominal Operating ΔV_{GSMAX} for Typical Bias Supply Voltage

V_{CC} (V)	ΔV_{GSMAX} (V)
2.3	4.3
2.5	5.0
2.7	5.6
3.0	6.5
3.3	7.0
5.0	7.0
6.0	7.0

Load Supply Power-Up after Circuit Breaker Armed

Figure 4 shows a normal power-up sequence for the circuit in Figure 1 where the V_{IN} load supply power-up after circuit breaker is armed. V_{CC} is first powered up by an auxiliary bias supply. V_{CC} rises above 2.07V at time point 1. V_{ON} exceeds 0.8V at time point 2. After a 60µs debounce delay, the GATE pin starts ramping up at time point 3. The external MOSFET starts conducting at time point 4. At time point 5, V_{GATE} exceed ΔV_{GSARM} and the circuit breaker is armed. After 50µs (t_{READY} delay), READY pulls high by an external resistor at time point 6. READY signals the V_{IN} load supply module to start its ramp. The load supply begins soft-start ramp at time point 7. The load supply ramp rate must be slow to prevent circuit breaker tripping as in Equation 8.

$$\frac{\Delta V_{IN}}{\Delta t} < \frac{I_{OPMAX} - I_{LOAD}}{C_{LOAD}} \quad (8)$$

Where I_{OPMAX} is the maximum operating current defined by Equation 7.

For illustration, V_{CB} = 25mV and $R_{DS(ON)}$ = 3.5mΩ at the nominal operating ΔV_{GSMAX}. The maximum operating current is 3.5A (refer to Equation 7). Assuming the load can draw a current of 2A at power-up, there is a margin of 1.5A available for C_{LOAD} of 100µF and V_{IN} ramp rate should be <15V/ms. At time point 8, the current through the MOSFET reduces after C_{LOAD} is fully charged.

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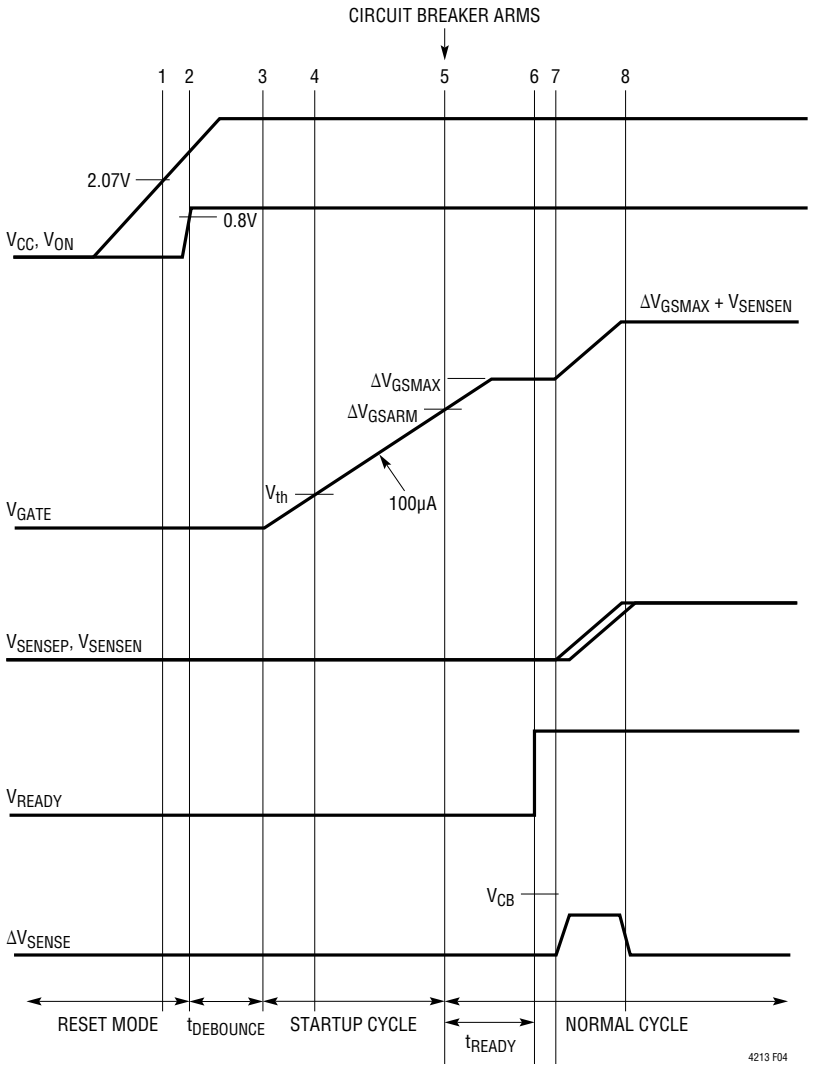

Figure 4. Load Supply Power-Up After Circuit Breaker Armed

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Load Supply Power-Up Before V_{CC}

Referring back to Figure 1, the V_{IN} load supply can also be powered up before V_{CC}. Figure 5 shows the timing diagram with the V_{IN} load supply active initially. An internal circuit ensures that the GATE pin is held low. At time point 1, V_{CC} clears UVLO and at time point 2, ON clears 0.8V. 60µs later at time point 3, the GATE is ramped up with 100µA. At time point 4, GATE reaches the external MOSFET threshold V_{TH} and V_{OUT} starts to ramp up. At time point 5, V_{SENSEN} is near its peak. At time point 6, the circuit breaker is armed and the circuit breaker can trip if $\Delta V_{SENSE} > V_{CB}$. At time point 7, the GATE voltage peaks. 50µs after time point 6, READY goes HIGH.

Start-up Problems

There is no current limit monitoring during output charging for the Figure 5 power-up sequence where the load supply is powered up before V_{CC}. This is because the GATE voltage is below ΔV_{GSARM} and the MOSFET may not reach the specified $R_{DS(ON)}$. The V_{IN} load supply should have sufficient capability to handle the inrush as the output charges up. For proper startup, the final

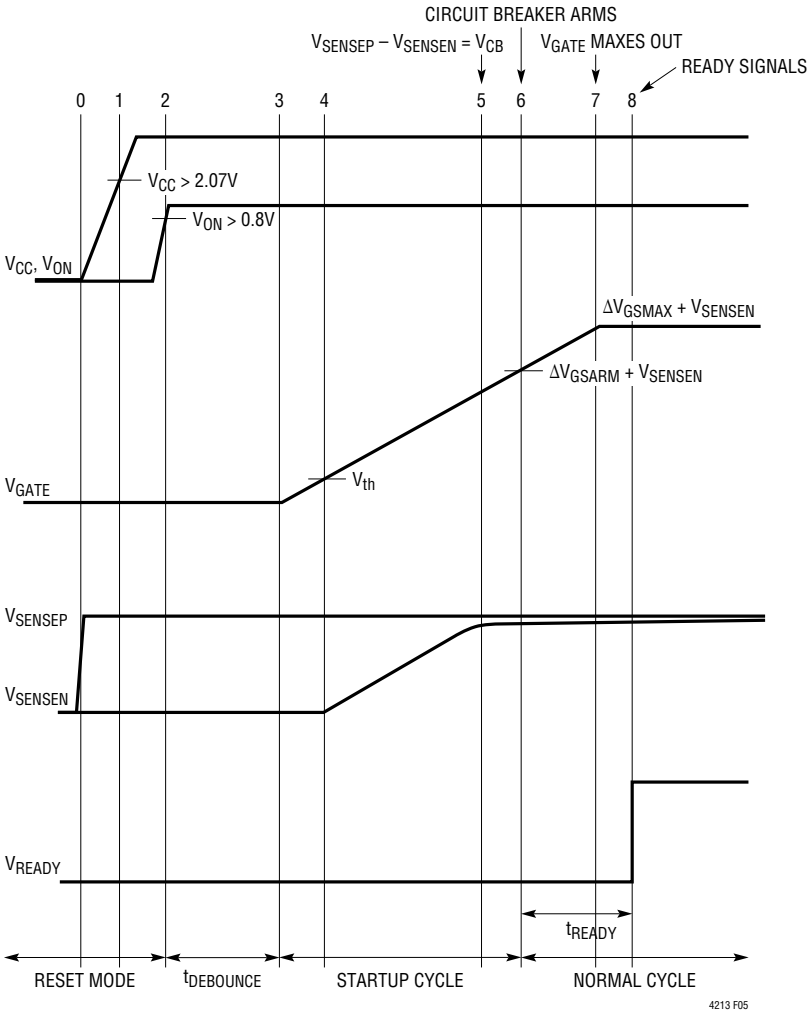

Figure 5. Load Supply Power-Up Before V_{CC}

APPLICATIONS INFORMATION

load at time point 6 should be within the circuit breaker limits. Otherwise, the system fails to start and the circuit breaker trips immediately after arming. In most applications additional external gate capacitance is not required unless C_{LOAD} is large and startup becomes problematic. If an external gate capacitor is employed, its capacitance value should not be excessive unless it is used with a series resistor. This is because a big gate capacitor without resistor slows down the GATE turn off during a fault. An alternative method would be a stepped I_{SEL} pin to allow a higher current limit during startup.

In the event of output short circuit or a severe overload, the load supply can collapse during GATE ramp up due to load supply current limit. The chosen MOSFET must withstand this possible brief short circuit condition before time point 6 where the circuit breaker is allowed to trip. Bench short circuit evaluation is a practical verification of a reliable design. To have current limit while powering a MOSFET into short circuit conditions, it is preferred that the load supply sequences to turn on after the circuit breaker is armed as described in an earlier section.

Power-Off Cycle

The system can be powered off by toggling the ON pin low. When ON is brought below 0.76V for 5µs, the GATE and READY pins are pulled low. The system resets when ON is brought below 0.4V for 80µs.

MOSFET Selection

The LTC4213 is designed to be used with logic (5V) and sub-logic (3V) MOSFETs for V_{CC} potentials above 2.97V with ΔV_{GSMAX} exceeding 4.5V. For a V_{CC} supply range between 2.3V and 2.97V, sub-logic MOSFETs should be used as the minimum ΔV_{GSMAX} is less than 4.5V.

The selected MOSFET V_{GS} absolute maximum rating should meet the LTC4213 maximum ΔV_{GSMAX} of 8V.

Other MOSFET criteria such as V_{BDSS}, I_{DMAX}, and $R_{DS(ON)}$ should be reviewed. Spikes and ringing above maximum operating voltage should be considered when choosing V_{BDSS}. I_{DMAX} should be greater than the current limit. The maximum operating load current is determined by the $R_{DS(ON)}$ value. See the Calculating Current Limit section for details.

Supply Requirements

The LTC4213 can be powered from a single supply or dual supply system. The load supply is connected to the SENSEP pin and the drain of the external MOSFET. In the single supply case, the V_{CC} pin is connected to the load supply, preferably with an RC filter. With dual supplies, V_{CC} is connected to an auxiliary bias supply V_{AUX} where V_{AUX} voltage should be greater or equal to the load supply voltage. The load supply voltage must be capable of sourcing more current than the circuit breaker limit. If the load supply current limit is below the circuit breaker trip current, the LTC4213 may not react when the output overloads. Furthermore, output overloads may trigger UVLO if the load supply has foldback current limit in a single supply system.

V_{IN} Transient and Overvoltage Protection

Input transient spikes are commonly observed whenever the LTC4213 responds to overload. These spikes can be large in amplitude, especially given that large decoupling capacitors are absent in hot swap environments. These short spikes can be clipped with a transient suppressor of adequate voltage and power rating. In addition, the LTC4213 can detect a prolonged overvoltage condition. When SENSEP exceeds V_{CC} + 0.7V for more than 65µs, the LTC4213's internal overvoltage protection circuit

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activates and the GATE pin pulls down and turns off the external MOSFET.

Typical Electronic Fuse Application for a Single Supply System

Figure 6 shows a single supply electronic fuse application. An RC filter at V_{CC} pin filters out transient spikes. An optional Schottky diode can be added if severe V_{CC} dips during a fault start-up condition is a concern. The use of the Schottky and RC filter combination is allowed if the load supply is above 2.9V and the total voltage drop towards the V_{CC} pin is less than 0.4V. The LTC4213's internal UVLO filter further rejects bias supply's transients of less than $t_{RESET.}$ During power-up, it is good engineering practice to ensure that V_{CC} is fully established before the ON pin enables the system at V_{ON} = 0.8V. In this application, the V_{CC} voltage reached final value approximately after a 5.3 • R_1 C_1 delay. This is followed by the ON pin exceeding 0.8V after a 0.17 • R_2C_2 delay. The GATE pin starts up after an internal $t_{DEBOUNCE}$ delay.

Typical Single Supply Hot Swap Application

A typical single supply hot swap application is shown in Figure 7. The $\overline{\text{RESET}}$ signal at the backplane is held low initially. When the PCB long edge makes contact the ON pin is held low (<0.4V) and the LTC4213 is kept in reset mode. When the short edge makes contact the V_{IN} load supply is connected to the card. The V_{CC} is biased via the RC filter. The V_{OUT} is pre-charged via R5. To power-up successfully, the R5 resistor value should be small enough to provide the load requirement and to overcome the 280µA current source sinking into the SENSEN pin. On the other hand, the R5 resistor value should be big enough avoiding big inrush current and preventing big short circuit current. When $\overline{\text{RESET}}$ signals high at backplane, C2 capacitor at the ON pin charges up via the R3/R2 resistive divider. When ON pin voltage exceeds 0.8V, the GATE pin begins to ramp up. When the GATE voltage peaks, the external MOSFET is fully turned on and the V_{IN}-to-V_{OUT} voltage drop reduces. In normal mode operation, the LTC4213 monitors the load current through the $R_{DS(ON)}$ of the external MOSFET.

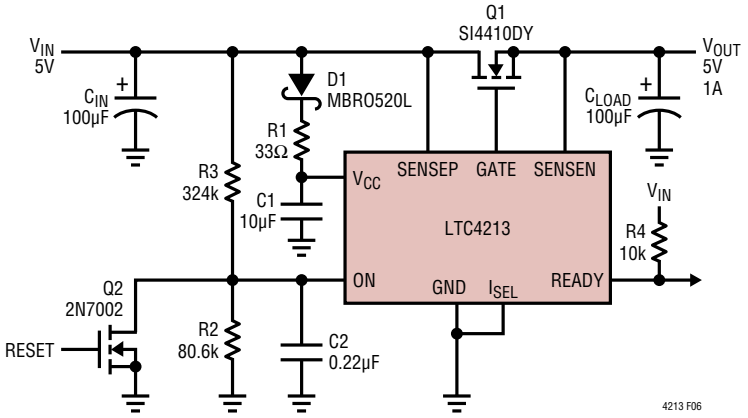
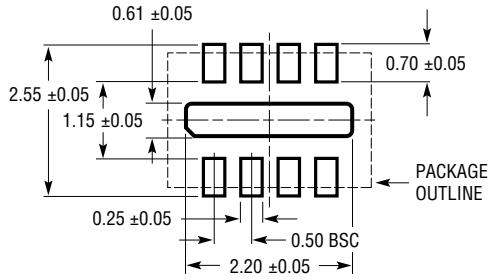


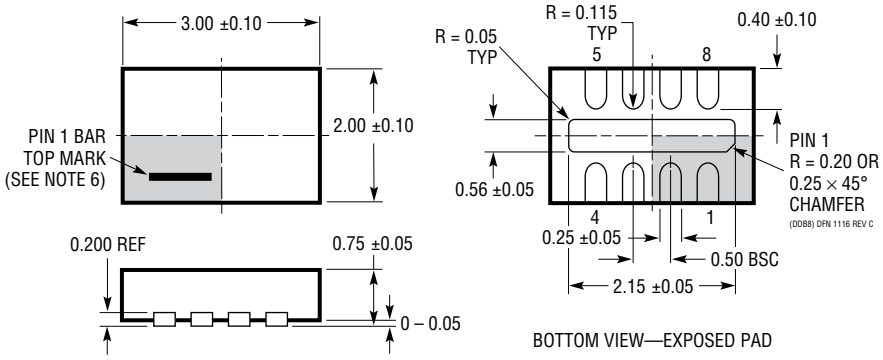
Figure 6. Single Supply Electronic Fuse

PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

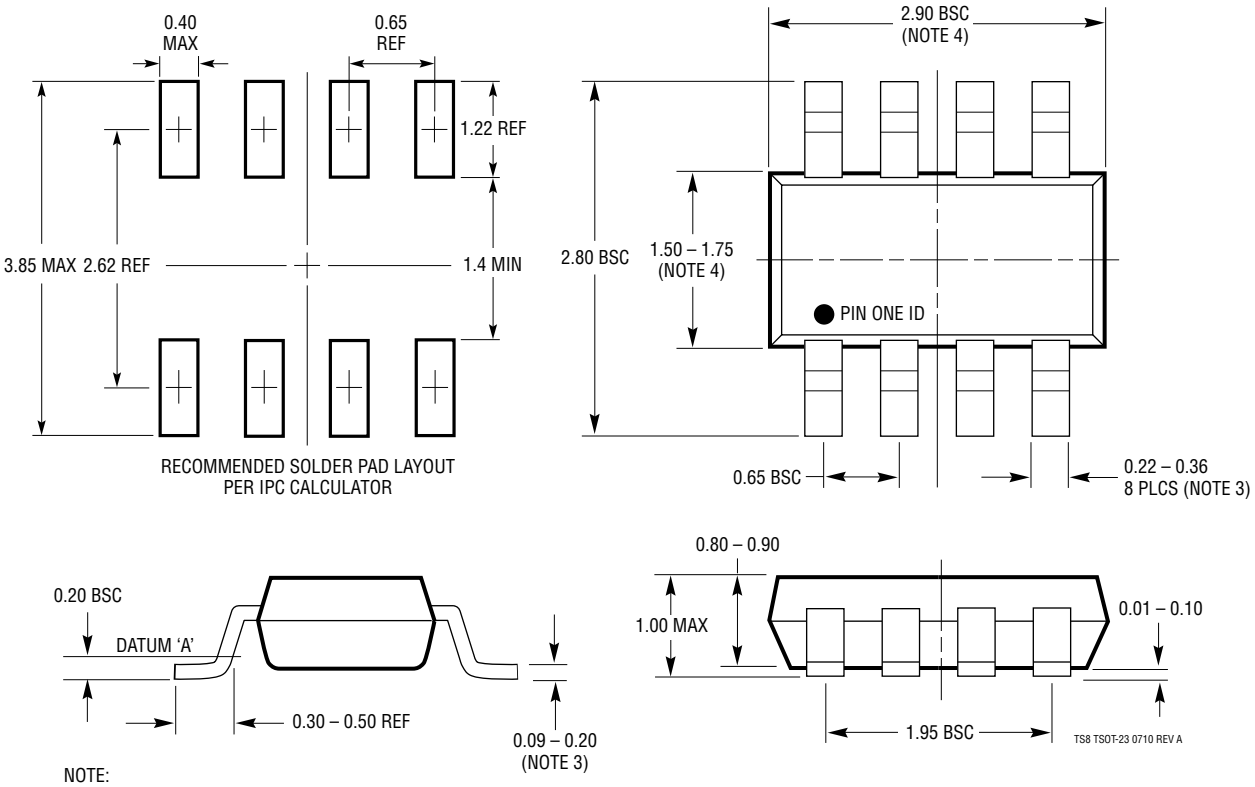


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637 Rev A)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/21	Added a new TSOT-23 (ThinSOT) package.	1
		Added the TSOT-23 pin configuration and the TSOT-23 order information.	2
		Updated Pin Functions section for TSOT-23.	7
		Removed pin number in the Block Diagram.	8
		Changed DDB package outline to Rev C.	19
		Added the TSOT-23 package Outline.	20
		Added part LTC4246 in the Related Parts table.	22

TYPICAL APPLICATION

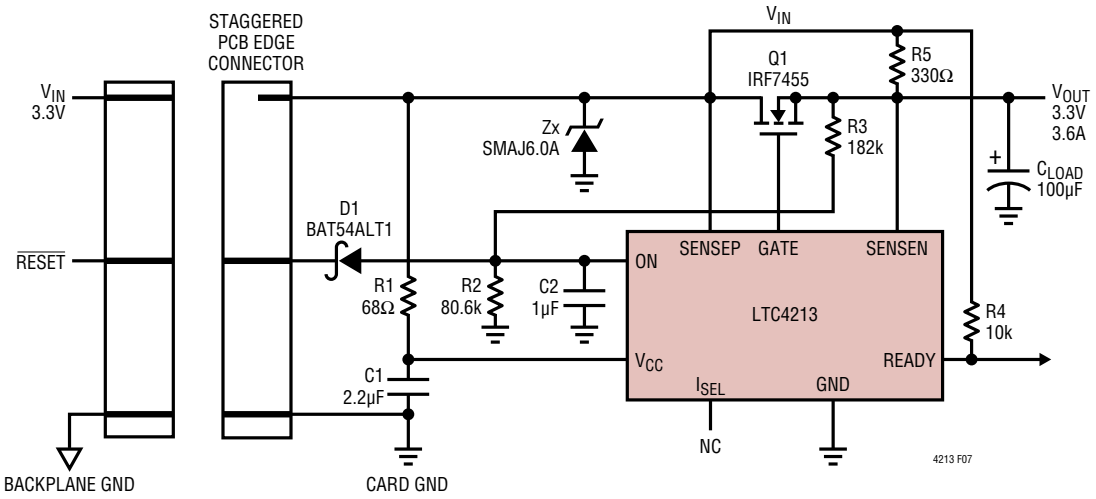


Figure 7. Single Supply Hot Board Insertion

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1421	Dual Channel, Hot Swap Controller	24-Pin, Operates from 3V to 12V and Supports –12V
LTC1422	Single Channel, Hot Swap Controller in SO-8	Operates from 2.7V to 12V, System Reset Output
LTC1642	Fault Protected, Hot Swap Controller	Operates up to 16.5V, Overvoltage Protection to 33V
LTC1643AL/ LTC1643AH	PCI Hot Swap Controllers	3.3V, 5V and ±12V Supplies
LTC1645	Dual Channel Hot Swap Controller	Operates from 1.2V to 12V, Power Sequencing
LTC1647	Dual Channel, Hot Swap Controller	Operates from 2.7V to 16.5V
LTC4210	Single Channel, Hot Swap Controller in SOT-23	Operates from 2.7V to 16.5V, Multifunction Current Control
LTC4211	Single Channel, Hot Swap Controller in MSOP	2.5V to 16.5V, Multifunction Current Control
LTC4216	Ultra Low Voltage Hot Swap Controller	Operates from 2.7V to 16.5V, Multifunction Current
LTC4221	Dual Channel, Hot Swap Controller	Protects Load Voltages from 0V to 6V
LTC4230	Triple Channel, Hot Swap Controller	1.7V to 16.5V, Multifunction Current Control
LTC4251	–48V Hot Swap Controller in SOT-23	–48V Hot Swap Controller, Active Current Limiting
LTC4252	–48V Hot Swap Controller in MSOP	Active Current Limiting with Drain Acceleration
LTC4253	–48V Hot Swap Controller and Sequencer	Active Current Limiting with Drain Acceleration and Three Sequenced Power Good Outputs
LTC4246	Octal Electronic Circuit Breaker	0V to 13.2V, 30mΩ R_{ON}, SPI Interface