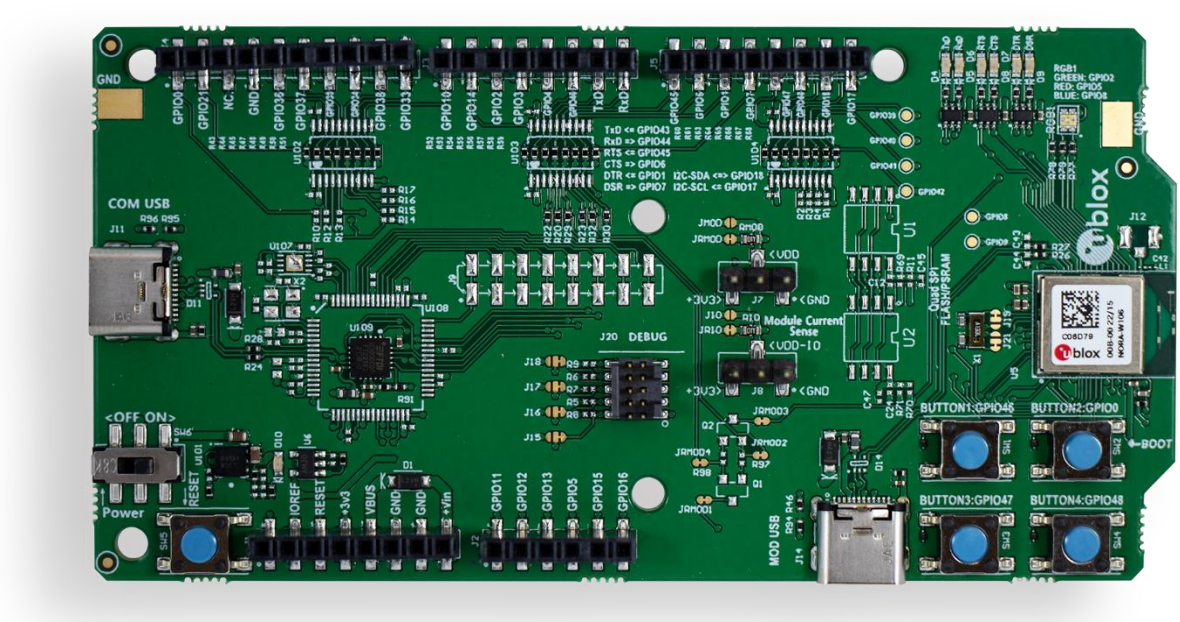
EVK-NORA-W10

Evaluation kit for NORA-W10 series modules

User guide



Abstract

The document describes how to set up and use the EVK-NORA-W101 and EVK-NORA-W106 evaluation kits for prototyping NORA-W10 open CPU, multiradio modules. It also describes the different options for debugging and the development capabilities included in the evaluation board.

Document information

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In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
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Mass production/ End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	**Document status**
EVK-NORA-W101	Early production information
EVK-NORA-W106	Early production information

☞ For information about the hardware, software, and status of the available product types, see the NORA-W10 data sheet [1].

Contents

1 Product description

1.1 Overview

The EVK-NORA-W10 evaluation kit provides stand-alone use of the NORA-W10 series module. This guide describes the hardware functionality of the EVK-NORA-W10 board and includes setup instructions for starting development.

All pins and interfaces supported on NORA-W10 series modules are conveniently accessed from the evaluation board. A simple USB connection provides the physical interface for the power, programming, and COM ports. A USB peripheral connector, reset button, and four other user buttons are available.

GPIO signals are available on headers that are compatible with the Arduino® form factor, which allows for the convenient use of existing Arduino shields. Current sense resistors allow for measuring current into the module and into the shield. For further information about the shields, visit the Arduino website [4].

Figure 1 shows the top view of the evaluation board.

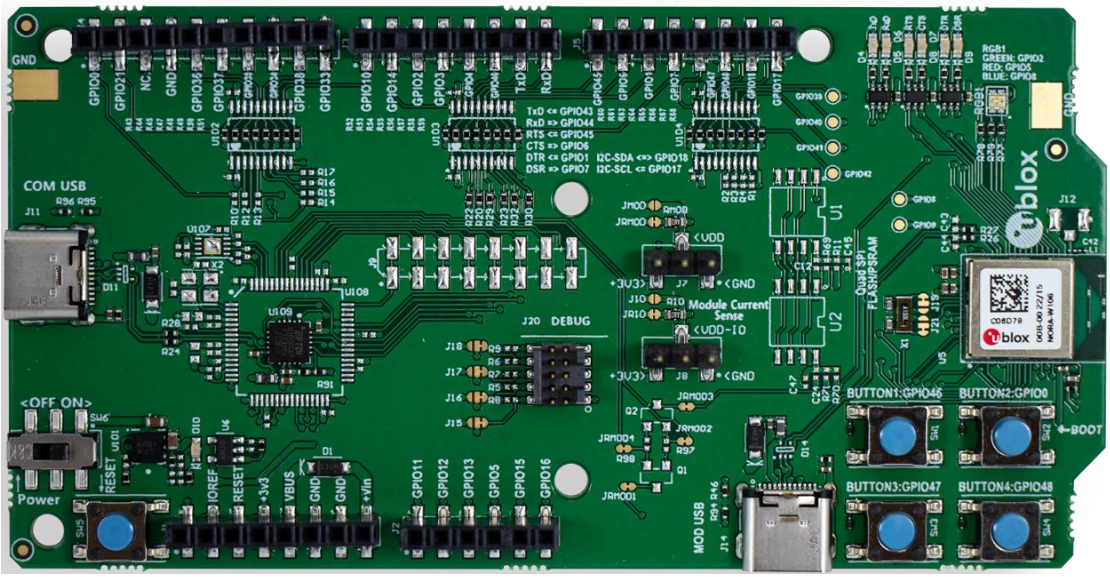

Figure 1: EVK-NORA-W10 evaluation board (top view)

1.2 Kit includes

1.2.1 EVK-NORA-W101

- EVK-NORA-W10 evaluation board with NORA-W101-00B module
- USB-C to USB-A adapter cable
- 2.4 GHz U.FL antenna

1.2.2 EVK-NORA-W106

- EVK-NORA-W10 evaluation board with NORA-W106-00B module
- USB-C to USB-A adapter cable
- A 2.4 GHz integrated antenna (external antenna not supplied)

1.3 Key features

NORA-W10 Open modules, based on SoC Espressif ESP32-S3, 2.4GHz Wi-Fi and Bluetooth® Low Energy, provide:

- IEEE 802.11 b/g/n protocol Wi-Fi subsystem
- Bluetooth® LE subsystem supporting Bluetooth 5 and Bluetooth mesh
- Xtensa® 32-bit LX7 dual core processor up to 240MHz operation
- Memory 384KB ROM and 512 KB SRAM
- Option for external SPI PSRAM for NORA-10x-00B version
- A QFN56 7x7 mm package
- EVK-NORA-W10 HW interfaces:
  - 3 UARTs, UART0 is the primary and must not be allocated to anything else
  - 32 GPIOs programmable
  - 4xSPI, the CS0 is reserved for internal flash memory
  - 2xI2C
  - 2xI2S
  - 2xUSB 2.0 full speed (OTG + serial /JTAG controller)
- Global certification

EVK-NORA-W10 boards provide:

- Evaluation board for NORA-W101 or NORA-W106 modules
- COM ports and debug ports over USB
- 32 GPIOs accessible on pin sockets and test points
- Buttons and status LEDs for user interaction
- Arduino compatible pin socket interface
- 32.768 kHz crystal
- USB peripheral connector
- Power input through USB-C or pin sockets
- Current measurement access points from pin headers and jumpers

1.4 Block diagram

Figure 2 shows the major interfaces and internal connections supported on the EVK-NORA-W10.

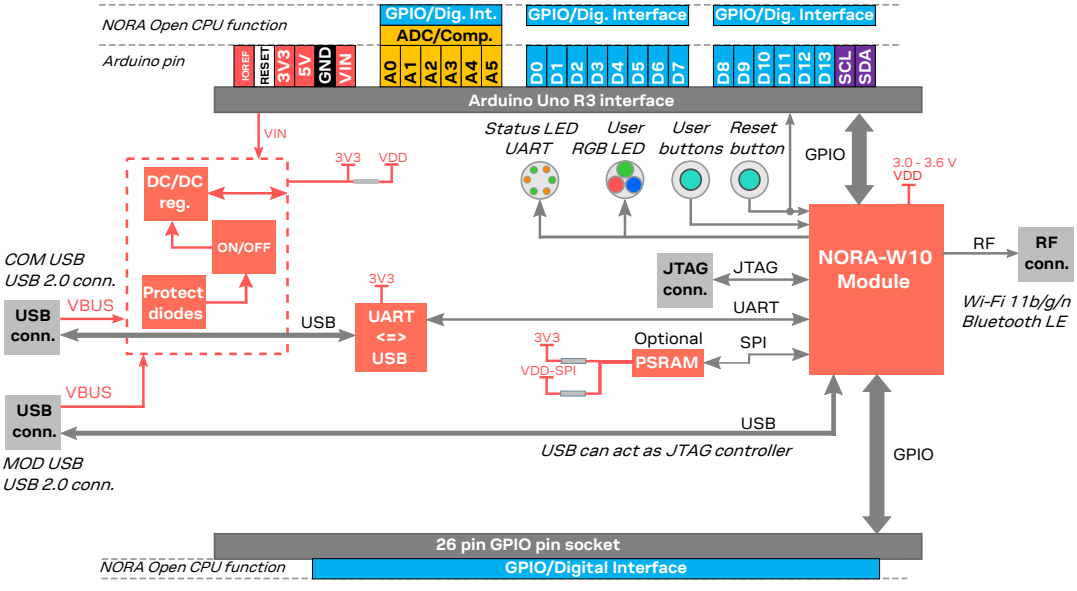

Figure 2: EVK-NORA-W10 block diagram

2 Setting up the evaluation board

The EVK-NORA-W10 is delivered without any software (open CPU) and the software must be developed by the user.

The following devices are applicable:

- EVK-NORA-W101
- EVK-NORA-W106

Connect the external power supply to the EVK as described in Powering the board. The green status LED (D10) is lit when the internal EVK 3.3 V supply is active.

⚠ Before powering up the EVK-NORA-W101, be sure to connect the 2.4 GHz antenna to the U.FL antenna connector (J12). Failing to do can cause module malfunction.

⚠ Observe that the inrush current when powering-up the EVK. The current level can be significantly higher than it is during normal operation.

The operating system installs the correct COM port drivers automatically. The drivers need to be installed only when you connect the unit to a new computer for the first time. For more information about the COM ports and their configuration, see the FTDI FT231XQ-R Datasheet [3].

Windows OS automatically assigns one COM port to the unit.

To view the assigned COM ports on Windows 10:

1. Open the **Control Panel** and click **Hardware and Sound**.
2. Click **Device Manager** in **Devices and Printers**. This opens the Device Manager window where you can view the assigned COM ports.

NORA-W10 open CPU module variants are used for developing custom software based on the Espressif IoT Development Framework (ESP-IDF) that provides a self-sufficient SDK and API for application development. Before compiling custom software, the ESP-IDF must be configured for use with the NORA-W10 open CPU variant. For information about setting up the ESP-IDF work environment, see the NORA-W10 system integration manual [2].

3 Hardware description

Design files for the EVK-NORA-W10 PCB are available from your local u-blox support team.

3.1 Overview

Figure 3 shows the physical location of the power switch, supported IO signals, LEDs, buttons, and connectors on the EVK-NORA-W10 board.

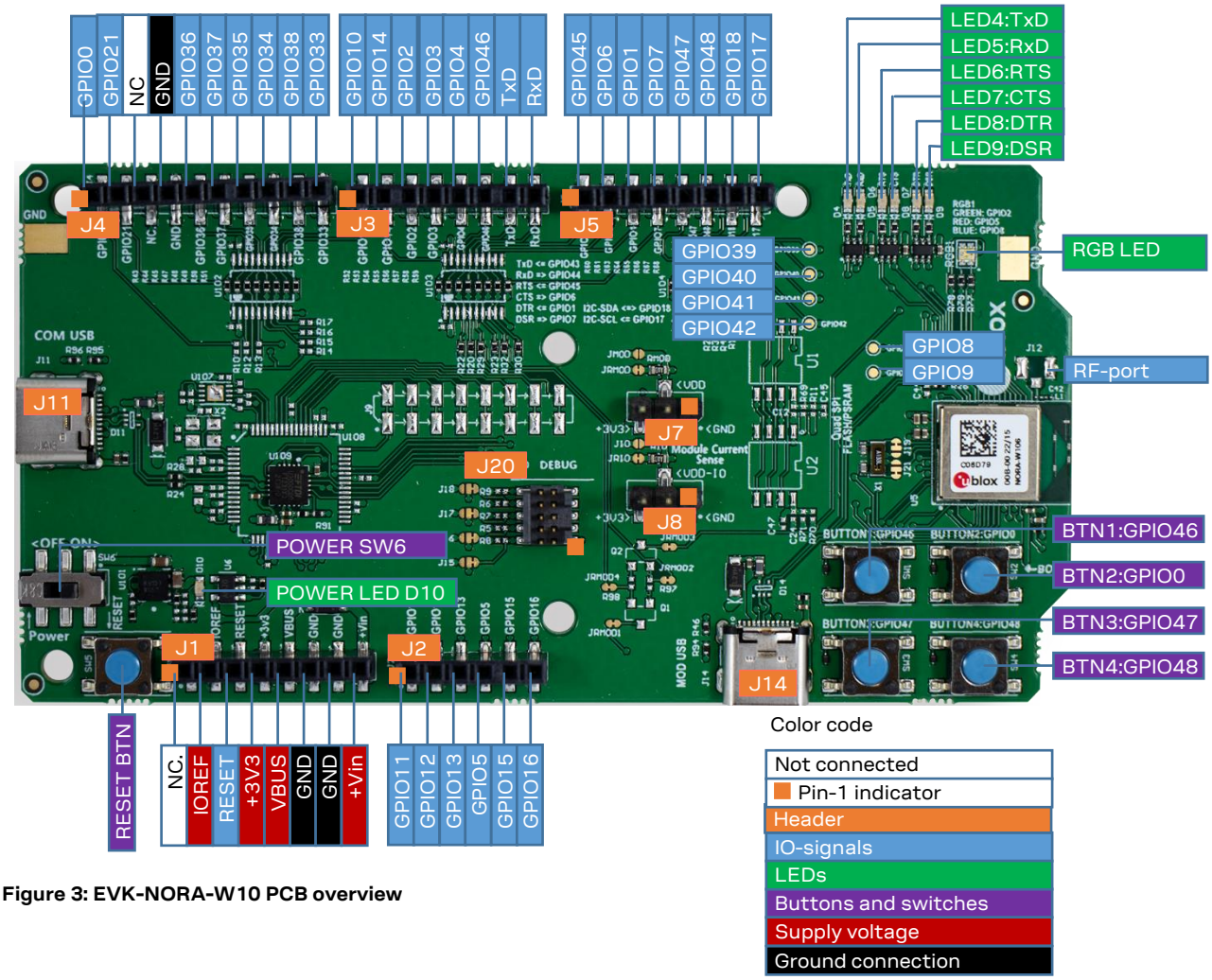

Figure 3: EVK-NORA-W10 PCB overview

3.2 Power

EVK-NORA-W10 can be supplied by three alternative sources:

- From the COM USB connector connected to the NORA-W10 COM port (UART0)
- from Module USB connector connected to the NORA-W10 USB interface+5 V [3.6–5.5 V]
- +Vin supply from the 2.54 mm pitch pin header (J1 pin 8)

Each of the three power sources are separated using a Schottky diode (D1 – D3, MBR120VLSFT3G). The diode prevents reverse voltage to any of the other supplies, which means that the power sources can be connected simultaneously. See Figure 4 and Figure 5.

⚠ Only if the power protection circuits are left intact can the USB be safely connected at the same time as external power. This makes programming of the module easier.

⚠ The EVK USB type C connectors are only capable of handling 5 V input, 12 V is not allowed.

3.2.1 Powering the board

Set the power switch (SW6) "ON" to extend the **VBUS** supply to the 3.3 V LDO regulator and power up the board. The LDO regulator powers the **+3V3, VDD** and **VDD-IO** power rails. The green LED (D1) is lit when power is applied. See also LEDs.

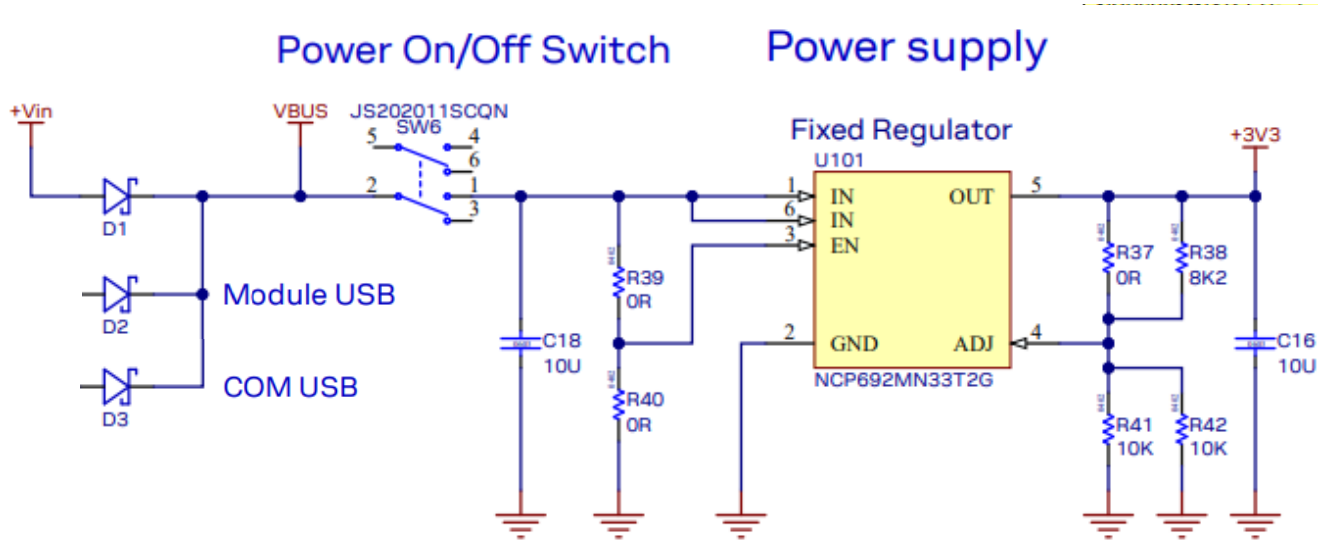

Figure 4: EVK schematic - power supply

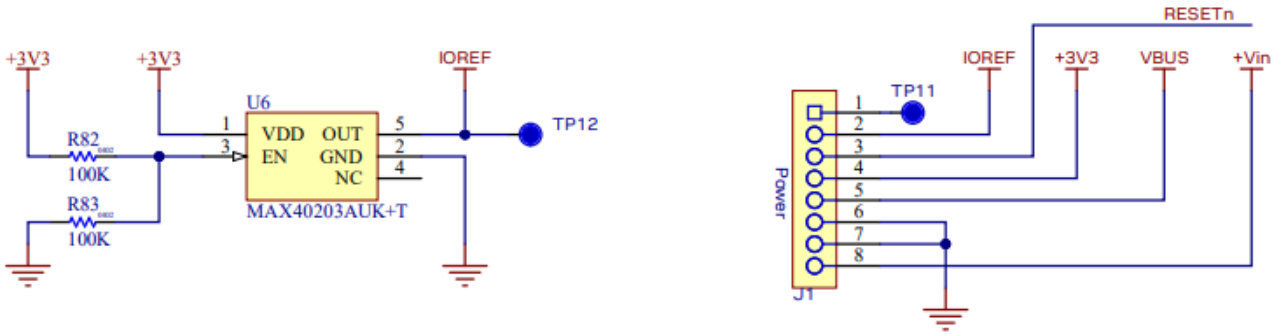

Figure 5: EVK schematic - IOREF separation

+3V3 (J1 pin 4) can supply external parts with up to 50 mA (max).

IOREF (J1 pin 2) is the external supply input to the IO voltage level shifters (optional). A protection diode (Maxim MAX40203AUK) with a voltage drop of around 30 mV at 100 mA separates **IOREF** from **+3V3**.

3.3 Reset

EVK-NORA-W10 provides a hardware reset to the NORA-W10 module. The Reset button (SW5) is connected to the module **RESETn** signal.

To enter bootloader mode, hold down the Boot button (SW2) during the USB power on.

To enter the programming mode, assert a reset in bootloader mode. See Figure 6 and Table 6.

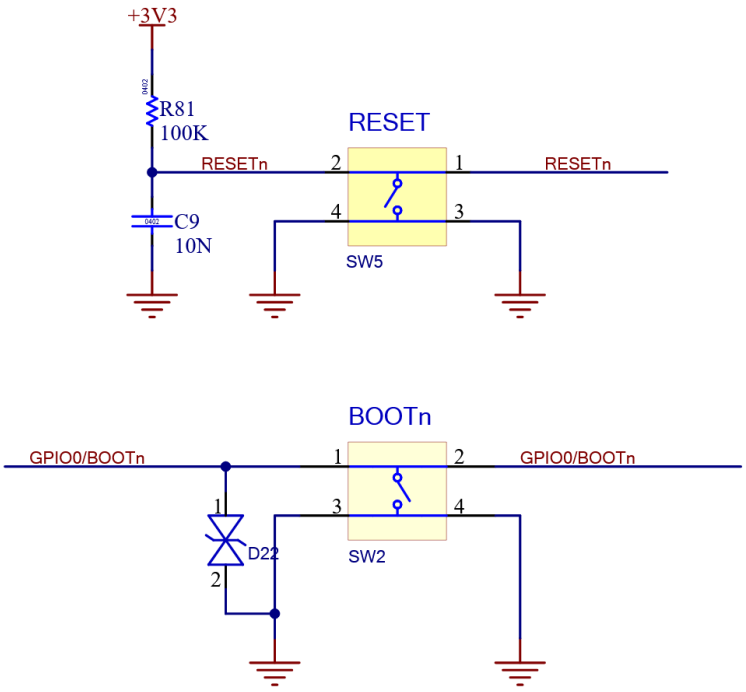

Figure 6: EVK schematic - reset and boot buttons

3.3.1 Automatic bootloader

The `esptool.py` flash tool supports automatic entry to the bootloader on the EVK-NORA-W10. The tool allows the board to be reset without the need to press the BOOT button. Connect the following pins to utilize this functionality:

- **RESETn** J1:3 to **GPIO6** (CTS) J5:2
- **GPIO0/BOOTn** J4:1 to **GPIO7** (DSR) J5:4

☞ It is not possible to use the Hardware Flow control or the DSR signals on the UART using this setup.

For more information about the tool, visit the GitHub esptool repository [5].

3.4 Buttons

In addition to the RESET button, the evaluation board also supports four user buttons that are active-low and connect to ground when pressed. The functionality of these buttons is controlled by the system software through the GPIO interface. The buttons and the associated GPIO signals are shown in Figure 7.

☞ The BOOTn button is multifunctional. Press the button when powering on the board to enter the boot mode. When the power cycle is complete, the button can then be used for other user functions in the software.

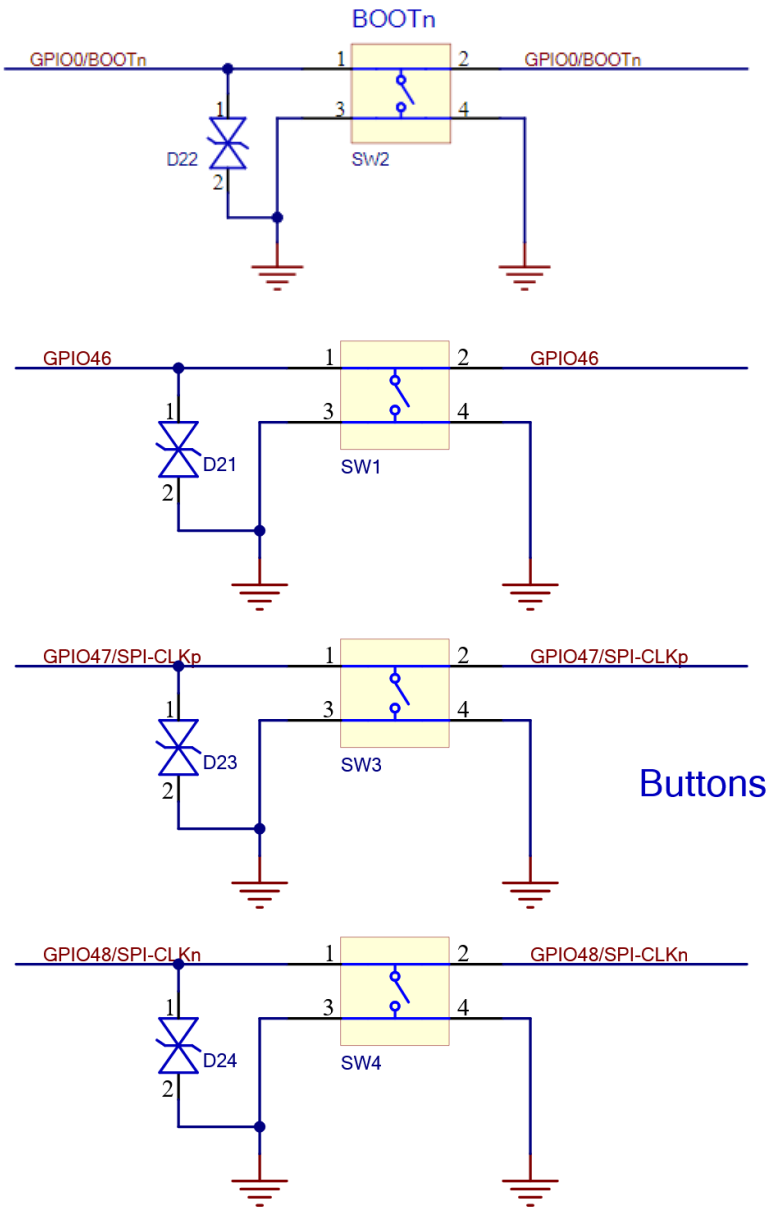

Figure 7: EVK schematic - user buttons

Table 1 describes the various user buttons and their relationship with the corresponding GPIO signals and protection diodes shown in Figure 7. For proper operation, the internal pull-up resistor of each NORA-W10 GPIO pin must be enabled.

Button	Switch	GPIO	Protection diode	Function
1	SW1	GPIO46	D21	No predefined function (software controlled)
2	SW2	GPIO0	D22	BOOTn
3	SW3	GPIO47	D23	No predefined function (software controlled)
4	SW4	GPIO48	D24	No predefined function (software controlled)
5	SW5	-	-	RESETn

Table 1: User button components

3.5 LEDs

EVK-NORA-W10 supports eight LEDs:

- **Power status** (D10): Indicates power on the board when lit (green)
- **UART0 status** (D4–D9): Indicates UART0 signal status under GPIO control, as shown in Table 3.
- **System status** (RGB1): Powered by **+3V3** and turned on by pulling the associated GPIO low. Disconnect each LED from the GPIO by removing resistors R78–R79, as shown in Table 2.

Table 2 describes the association between each RGB LED and respective GPIO. Having disconnected an RGB LED (R78-R79), the related signal can be optionally used for analog-to-digital conversion.

RGB LED	Associated GPIO	Comments
Red (pin1)	GPIO5/ADC1-CH4	Remove R77 to disconnect R-LED
Green (pin2)	GPIO2/ADC1-CH1	Remove R78 to disconnect G-LED
Blue (pin3)	GPIO8/ADC1-CH7	Remove R79 to disconnect B-LED

Table 2: RGB LED associated signals

Figure 8 shows the schematic for the System status (RGB1) LED. Figure 9 shows the schematic that includes the six UART0 status LEDs and buffers, U3, U4 and U7.

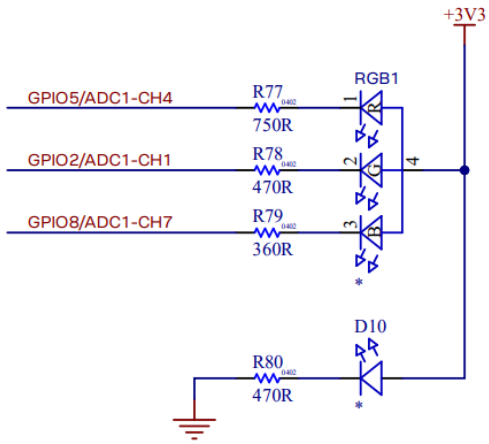

Figure 8: Schematic – RGB and power LED

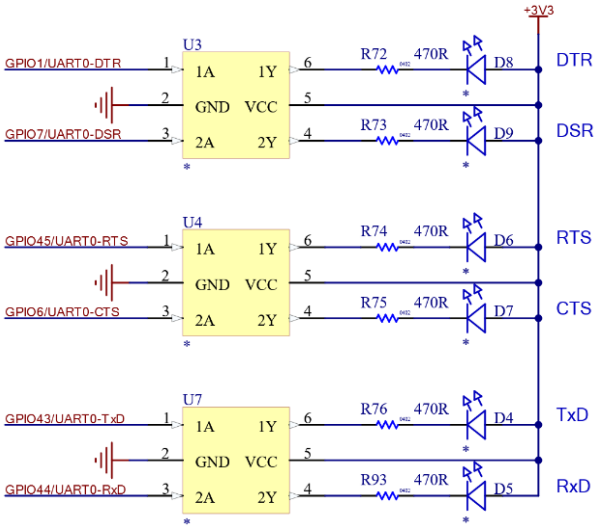

Figure 9: Schematic – UART0 status LEDs

Table 3 describes each of the UART0 LEDs and their relationship with corresponding pin sockets, GPIO, and serial UART0 signals.

LED	Color	GPIO	Pin socket	Comments
D4	Green	GPIO43/UART0-TxD	J3-7	UART0-TxD activity indicator
D5	Orange	GPIO44/UART0-RxD	J3-8	UART0-RxD activity indicator
D6	Green	GPIO45/UART0-RTS	J5-1	UART0-RTS activity indicator
D7	Orange	GPIO6/UART0-CTS	J5-2	UART0-CTS activity indicator
D8	Green	GPIO1/UART0-DTR	J5-3	UART0-DTR activity indicator
D9	Orange	GPIO7/UART0-DSR	J5-4	UART0-DSR activity indicator
D10	Green	-		Power ON indicator

Table 3: UART0 LEDs and associated signals

3.6 USB interfaces

There are two physical USB interfaces on the EVK: COM USB (J11) and a MOD USB (J14). The location of these connectors on the EVK-NORA-W10 PCB are shown in Figure 3.

3.6.1 COM USB interface

The COM USB interface (J11) is connected to a USB-to-UART0 converter (FTDI IC, U109). The FTDI IC U108 is not used in the design. Further on, the FTDI IC is via 1 kΩ resistors connected to the module (U5), see Figure 22. The current limiting resistors can be seen as a barrier to the FTDI IC allowing the use of the COM USB power function once an optional external UART0 is connected through the pin sockets J3 and J5. Only one UART0 interface at a time can be used. See UART0s at J3 and J4 in Figure 10.

The level shifters are by default bridged by 0 Ω resistors, but these can be activated by removing the 0 Ω resistors if necessary.

Table 4 shows the function and COM port connections for each module pin.

NORA-W10 pin name	NORA-W10 function	Resistor/Jumper enable	Interface IC function
G9	GPIO44/UART0-RxD	R20	FTDI-TxD
G8	GPIO43/UART0-TxD	R22	FTDI-RxD
F9	GPIO6/UART0-CTS	R23	FTDI-RTS
F8	GPIO45/UART0-RTS	R29	FTDI-CTS
E9	GPIO7/UART0-DSR	R30	FTDI-DTR
E8	GPIO1/UART0-DTR	R32	FTDI-DSR

Table 4: COM port connections

U103 and U104 are level shifters that by default are not mounted but are instead bypassed with 0 Ω resistors. When mounted, the level shifters allow the module to operate at a higher IOREF digital voltage level than +3V3 (through connectors J3 and J5). See Figure 10.

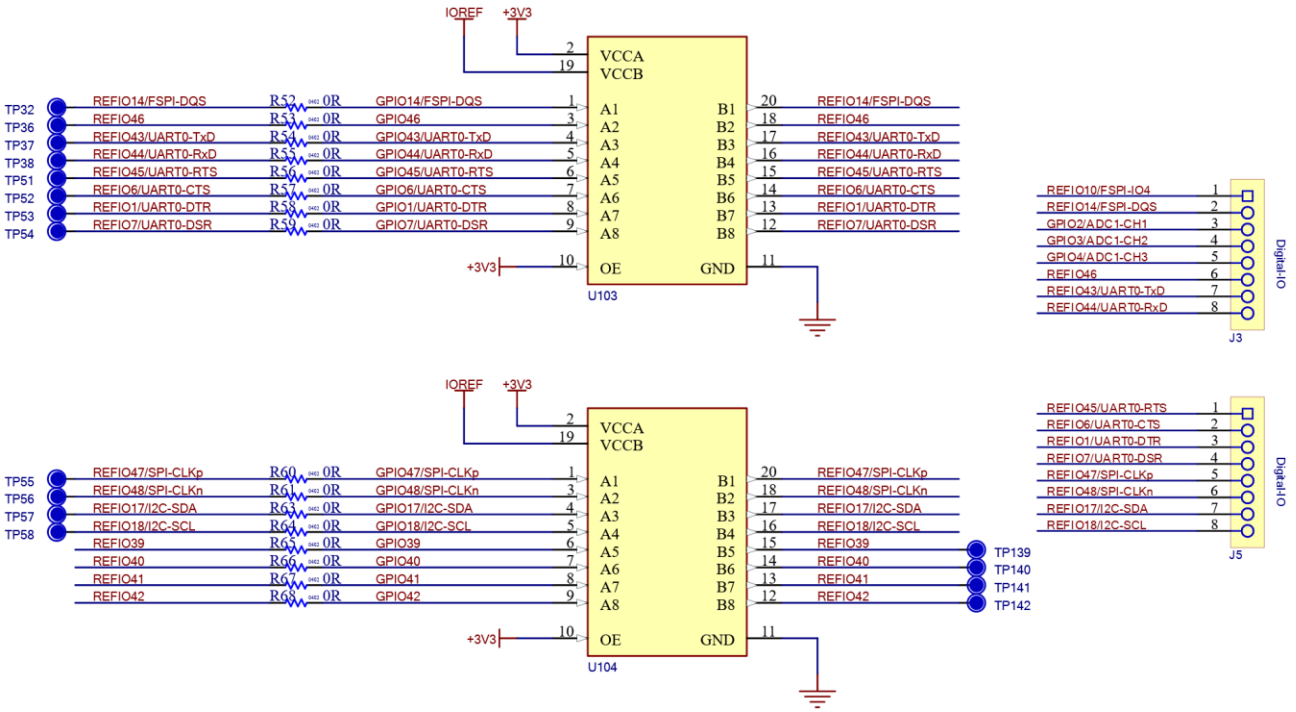

Figure 10: UART0 level shifters and pin socket

For easy serial communication with the NORA-W10 module, a computer can connect to the evaluation board to provide a single COM port through a single FTDI, USB-to-UART IC, as shown in Figure 11. The CBUS block is not used.

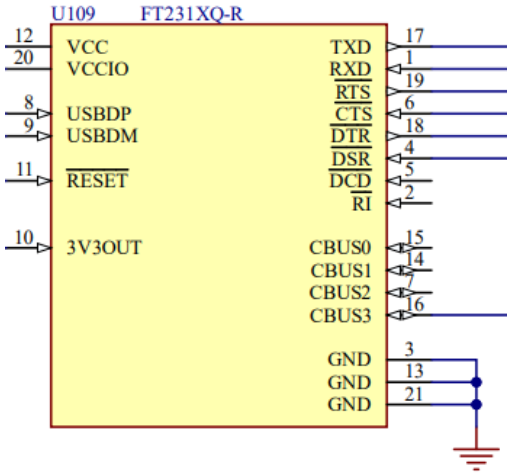

Figure 11: FTDI schematic, 1 port default

3.6.2 MOD USB interface

The MOD USB is directly connected to the module providing easy communication. A USB Serial/JTAG controller resides in NORA-W10, which allows it to act as an USB to serial converter as well as an USB to JTAG adapter for communication with CPU debug core. However, NORA-W10 is set to be used as a JTAG controller by default and this is currently the only option.

3.7 32.768 kHz low frequency clock

The evaluation board has a 32.768 kHz crystal connected to the NORA-W10 module that allows use of the external crystal option to source the RTC clock. The clock can otherwise be sourced from the slow internal RC oscillator or the divided clock of the internal fast RC oscillator.

If **GPIO15/ADC2-CH4** and **GPIO16/ADC2-CH5** are used, the crystal can be removed from the circuit by opening jumpers J19 and J21 and soldering across the normally open positions, as shown in Figure 12. This connects **XT-32k-p** and **XT-32k-n** to EVK pin socket J2, pin 5 and pin 6. See also GPIO jumpers and Table 6.

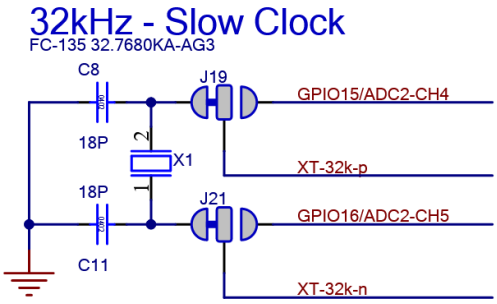

Figure 12: Schematic – 32 kHz crystal

3.8 Current-sensing headers

The evaluation board provides two current-sensing headers:

- J7 for power consumption measurement of the module **VDD** supply
- J8 for power consumption measurement of the module **VDD-IO** supply

Each of the 2.54 mm pitch 3-pin headers has two pins connected across a 1 Ω current-sense resistors, **RMOD** and **RIO** respectively, with the third connected to **GND**. The module **VDD** and **VDD-IO** supplies are sourced through these resistors. To measure current consumption, use a multimeter or other precise voltage measurement device to measure the voltage drop across pins 2 and 3. Current can also be measured directly by opening **JRMOD** or **JRIO** to remove the current-sense resistor from the circuit. Use an amperemeter in-series with the two voltage pins.

⚠ Pin 1 of J7 and J8 is connected to GND.

To bypass the current sense resistors, **RMOD** and **RIO**, solder the respective jumpers **JMOD** and **JIO**.

The default hardware configuration does not require any modification of the current-sense headers for the EVK-NORA-W10 to perform properly. See also Table 6.

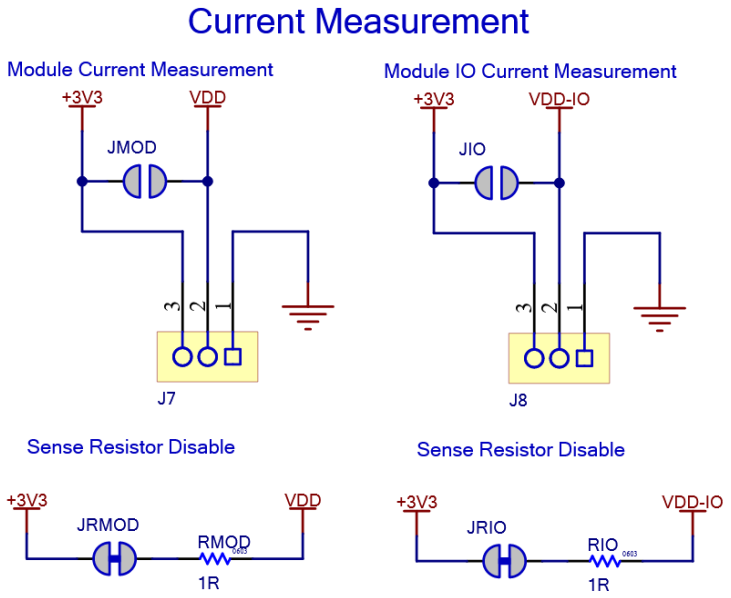

Figure 13: Current-sensing header circuits

3.9 JTAG debug interface

There is mainly one interface for debugging NORA-W10 using JTAG:

- An external debug unit can be attached to the J20 header connector for firmware programming and debug. J20 is implemented with a 2x5 header with 1.27 mm pitch. Figure 14 shows the physical layout of the connector.
- A USB serial/JTAG adapter, however default put in USB serial mode. See also MOD USB interface.

The CPU JTAG signals can either be routed to the USB Serial/JTAG Controller or the external JTAG adapter GPIO pads using eFuses. See also Table 6.

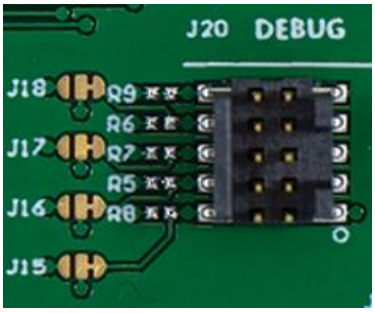

Figure 14: J20 physical layout

Figure 15 shows a schematic diagram of the JTAG debug interface.

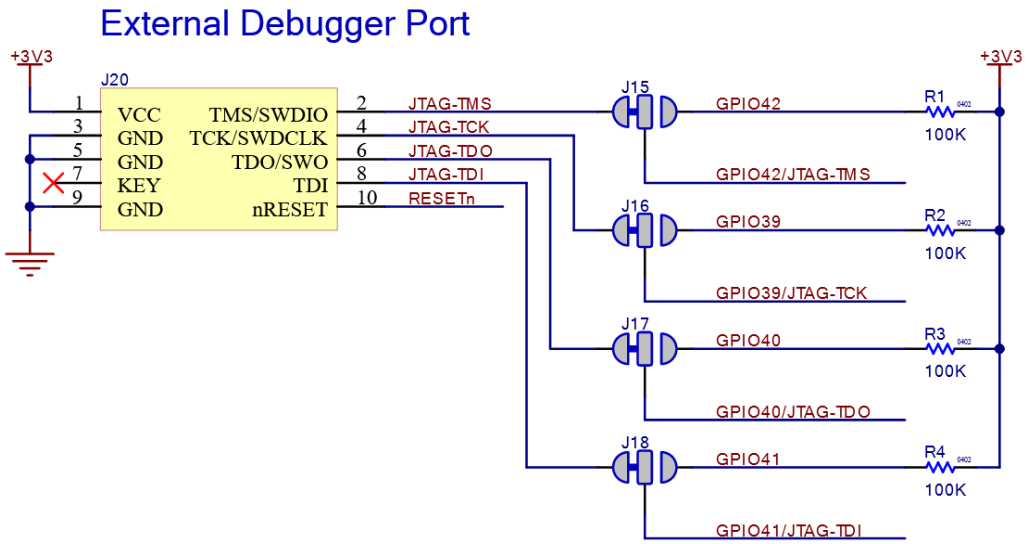

Figure 15: External JTAG debug interface

3.10 QSPI memory

3.10.1 External PSRAM

Valid for NORA-W10x-00B modules including embedded flash.

A Quad SPI PSRAM can optionally be mounted at position U1 on the EVK board. As an embedded flash memory already resides on the configured module, U2 must be left unmounted.

The PSRAM can be powered from either the **+3V3** or the internal **VDD-SPI** on the module. The **VDD-SPI** can supply 3.3 V – I_{memory} x 14 Ω. Fit either resistor R11 or R69 to select your preferred choice of power supply for the SPI PSRAM.

Figure 16 shows the schematic of the External SPI PSRAM circuit and its implementation on the EVK board.

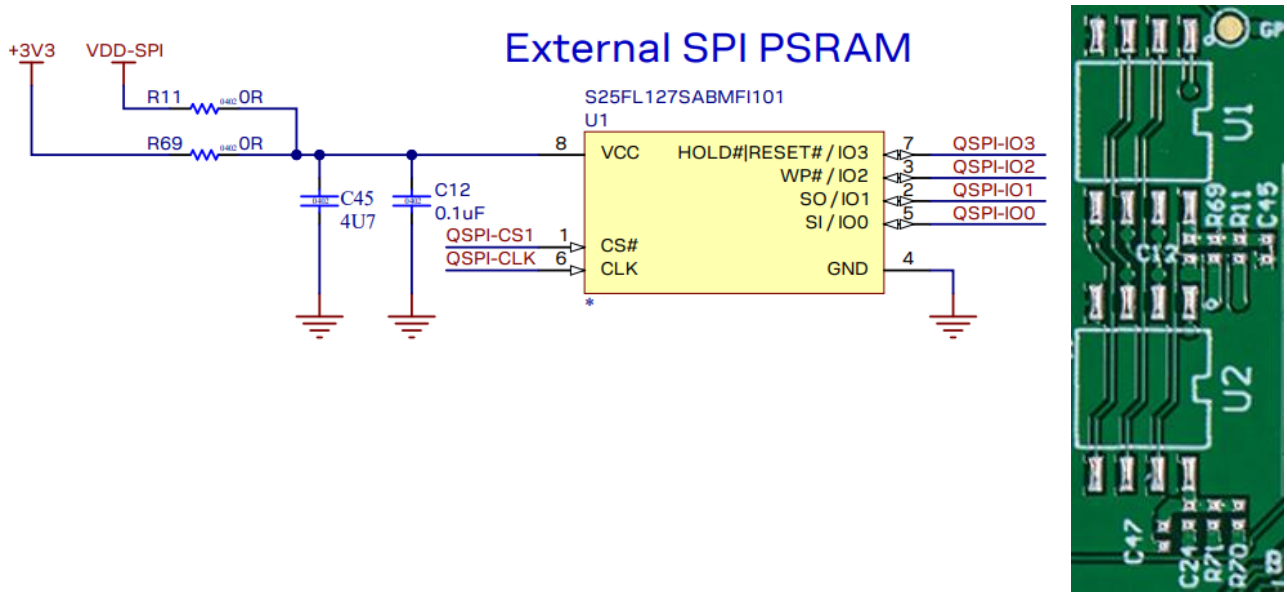

Figure 16: Quad PSRAM EVK - schematic (left) and EVK board view (right)

Table 5 shows the SPI functions for corresponding ESP32-S3 GPIOs and NORA-W10 pins.

Interface function	ESP32-S3 GPIO	NORA-W10 pin	Interface IC function
QSPI-CS1	26	E1	PSRAM chip select
QSPI-CLK	30	F1	SPIO clock
QSPI-IO3 HD	27	F2	SPIO Hold
QSPI-IO2 WP	28	D1	SPIO Write Protect
QSPI-IO1 Q	31	E2	SPIO Controller Input Peripheral
QSPI-IO0 D	32	D2	SPIO Controller Output

Table 5: Quad SPI interface signal overview for external PSRAM

3.11 Jumpers

The EVK-NORA-W10 printed circuit board (PCB) supports several solder-bridge jumpers for configuring GPIO functions. Most jumpers disconnect on-board components from the GPIO nets and subsequently eliminate interference generated by any external circuits attached to the (female) I/O sockets. The physical locations of the jumpers are shown in Figure 17. For a functional overview of the jumpers, see also Table 6.

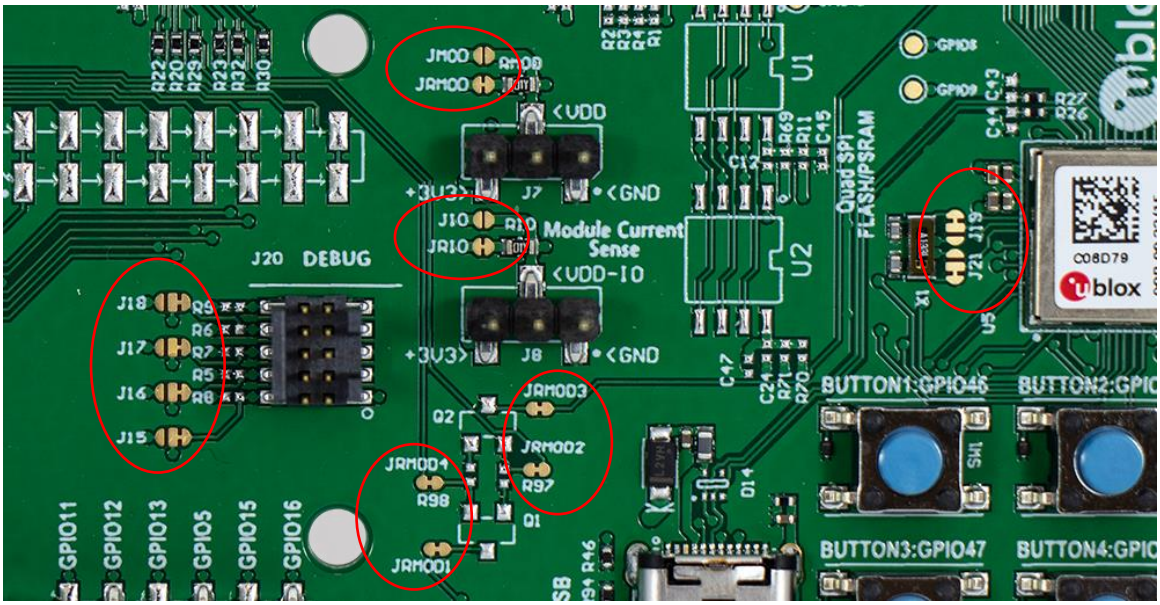

Figure 17: PCB jumper positions – highlighted in red

The physical location of some GPIO jumpers, test points, and other components are shown on the bottom side of the PCB, as shown in Figure 18. The test points are described in Table 7.

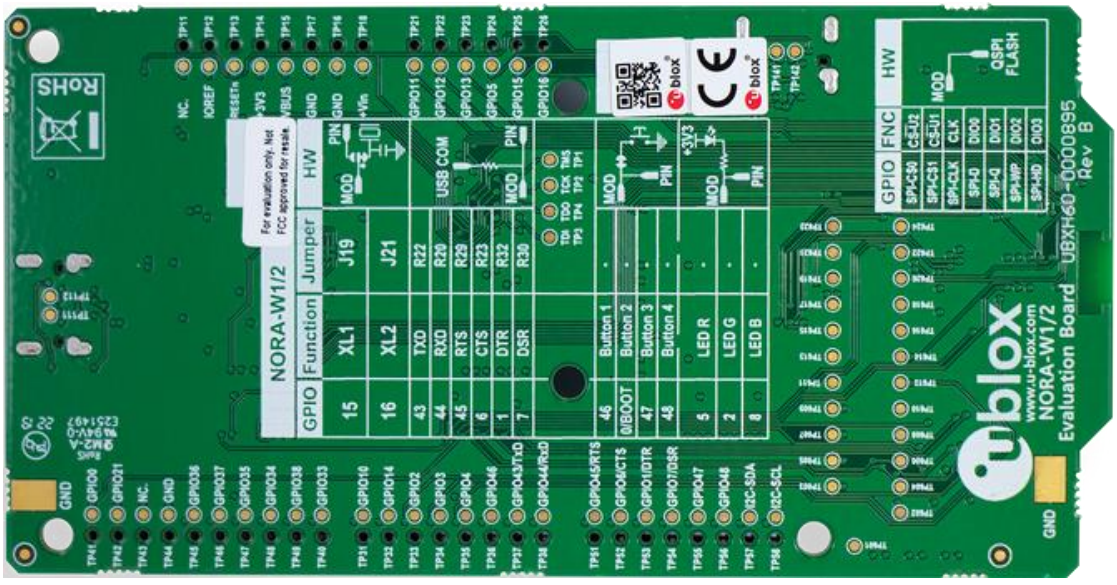

Figure 18: Legend for GPIO jumpers and test points (bottom view)

Table 6 shows the default configuration of “solder-bridge" jumpers. Choose alternative configurations by cutting the bridge and soldering the jumpers in the default positions.

Jumper	Jumper type	Default function	Alternate function
J15	Solder-bridge	Connected to J20 debug connector, JTAG-TMS	Cut and close to Test Point GPIO42
J16	Solder-bridge	Connected to J20 debug connector, JTAG-TCK	Cut and close to Test Point GPIO39
J17	Solder-bridge	Connected to J20 debug connector, JTAG-TDO	Cut and close to Test Point GPIO40
J18	Solder-bridge	Connected to J20 debug connector, JTAG-TDI	Cut and close to Test Point GPIO41
J19	Solder-bridge	Connected to 32KHz clock, XT-32k-p	Cut and close to J2 connector GPIO15
J21	Solder-bridge	Connected to 32KHz clock, XT-32k-n	Cut and close to J2 connector GPIO16
JMOD	Solder-bridge open	Open - VDD disconnects +3V3	Once shorted VDD connects to +3V3
JRMOD	Solder-bridge short	VDD connected to +3V3	Open – current sense resistor disabled
JIO	Solder-bridge open	Open – VDD-IO disconnects +3V3	Once shorted VDD-IO connects to +3V3
JRIO	Solder-bridge short	VDD-IO connected to +3V3	Open – current sense resistor disabled
JRMOD1	Solder-bridge short	Alternative RESET using UART-DTR and RTS instead of button SW5	Open – RESETn disconnected
JRMOD2	Solder-bridge short	GPIO1/UART0-DTR for RESET and BOOT	Open – GPIO1/UART0-DTR disconnected
JRMOD3	Solder-bridge short	Alternative BOOT using UART-DTR and RTS instead of button SW2	Open – GPIO0/BOOTn disconnected
JRMOD4	Solder-bridge short	GPIO45/UART0-RTS for RESET and BOOT	Open – GPIO45/UART0-RTS disconnected

Table 6: Solder-bridge jumper overview

* The test points that are not used are reserved for J6 (2 x 12 pin socket) SMD or the through-hole SMD version of J6. The connector can be mounted from both the top and bottom side of the board. TP601 is offset in the layout to avoid collision with adjacent 3.2 mm hole.

Table 7 describes the test points **TP601-TP624**. The function of the other test points are described in the adjacent layout text shown in Figure 18.

Test point	Function
TP601, 602, 604, 606, 608, 610, 611, 613	Not used*
TP603	REFIO39
TP605	REFIO40
TP607	REFIO41
TP609	REFIO42
TP612	GPIO8/ADC1-CH7
TP614	GPIO9/ADC1-CH8
TP615-TP624	Not used*

* The test points that are not used are reserved for J6 (2 x 12 pin socket) SMD or the through-hole SMD version of J6. The connector can be mounted from both the top and bottom side of the board. TP601 is offset in the layout to avoid collision with adjacent 3.2 mm hole.

Table 7: Test point description

3.12 Header pin-out

Figure 14 shows the 2.54 mm pitch sockets exposing the IO signals on the NORA-W10 module.

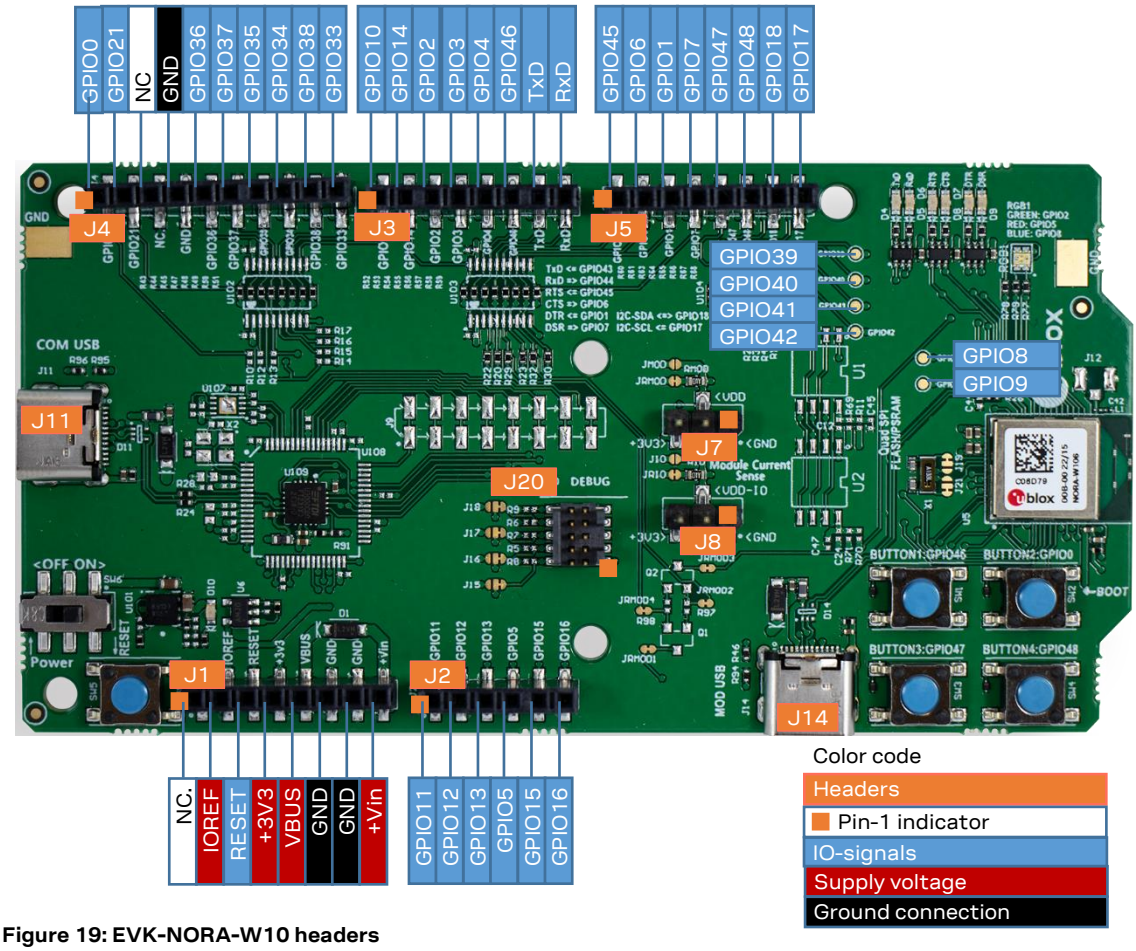

Figure 19: EVK-NORA-W10 headers

⚠ To enable the EVK-NORA-W10 I/O pins to handle 5 V signals the level shifters (U102 – U104, TI TXS0108EPWR) must be populated and **IOREF** must be supplied with +5 V. When using 3.3 V on the EVK-NORA-W10 I/O pins, the Arduino Uno® style shields must be configured to use the +3.3 V I/O voltage reference.

Table 8 - Table 13 show the pin assignments of each header.

Pin	Pin name	NORA-W10 pin	Function
1	NC.	-	No connection
2	IOREF	-	Level shifter supply voltage
3	RESETn	J3	ESP-GPIO/AIN6
4	+3V3	–	Supply
5	VBUS		Supply
6	GND		Ground
7	GND		Ground
8	+Vin		Supply

Table 8: Header J1, power

Pin	Pin name	NORA-W10 pin PT1/PT2	Function
1	GPIO11	G3	GPIO ADC2-CH0
2	GPIO12	G2	GPIO ADC2-CH1
3	GPIO13	A6	GPIO ADC2-CH2
4	GPIO5	J8	GPIO ADC1-CH4
5	GPIO15	C6	GPIO ADC2-CH4, XTAL-32K-P
6	GPIO16	B6	GPIO ADC2-CH5, XTAL-32K-N

Table 9: Header J2, analog IO

Pin	Pin name	NORA-W10 pin	Function
1	GPIO10	H3	FSPI-IO4
2	GPIO14	A5	FSPI-DQS
3	GPIO2	H8	ADC1-CH1
4	GPIO3	J9	ADC-CH2
5	GPIO4	D8	ADC1-CH3
6	GPIO46	H7	GPIO46
7	TxD	G8	GPIO43
8	RxD	G9	GPIO44

Table 10: Header J3, digital IO

Pin	Pin name	NORA-W10 pin	Function
1	GPIO0	F7	BOOTn
2	GPIO21	C8	GPIO21
3	NC.	–	No connection
4	GND	–	
5	GPIO36	B1	FSPI-CLK
6	GPIO37	C1	FSPI-Q
7	GPIO35	C2	FSPI-D
8	GPIO34	B3	FSPI-CS0
9	GPIO38	A2	FSPI-WP
10	GPIO33	D3	FSPIHD

Table 11: Header J4, digital IO

Pin	Pin name	NORA-W10 pin	Function
1	GPIO45	F8	RTS
2	GPIO6	F9	CTS
3	GPIO1	E8	DTR
4	GPIO7	E9	DSR
5	GPIO47	F3	SPICLK_P
6	GPIO48	E3	SPICLK_N
7	GPIO18	B4	SDA
8	GPIO17	A3	SCL

Table 12: Header J5, digital IO

Pin	Pin name	NORA-W10 pin	Function
1	+3V3	-	Supply
2	JTAG-TMS	H2	GPIO42 if J15 is changed
3	GND	-	Ground
4	JTAG-TCK	J2	GPIO-39 if J16 is changed
5	GND	-	Ground
6	JTAG-TDO	G1	GPIO40 if J17 is changed
7	NC.	-	No connection
8	JTAG-TDI	H1	GPIO41 if J18 is changed
9	GND	-	Ground
10	RESET	J3	Module reset

Table 13: Header J20, External JTAG debug port

Appendix

A Schematics

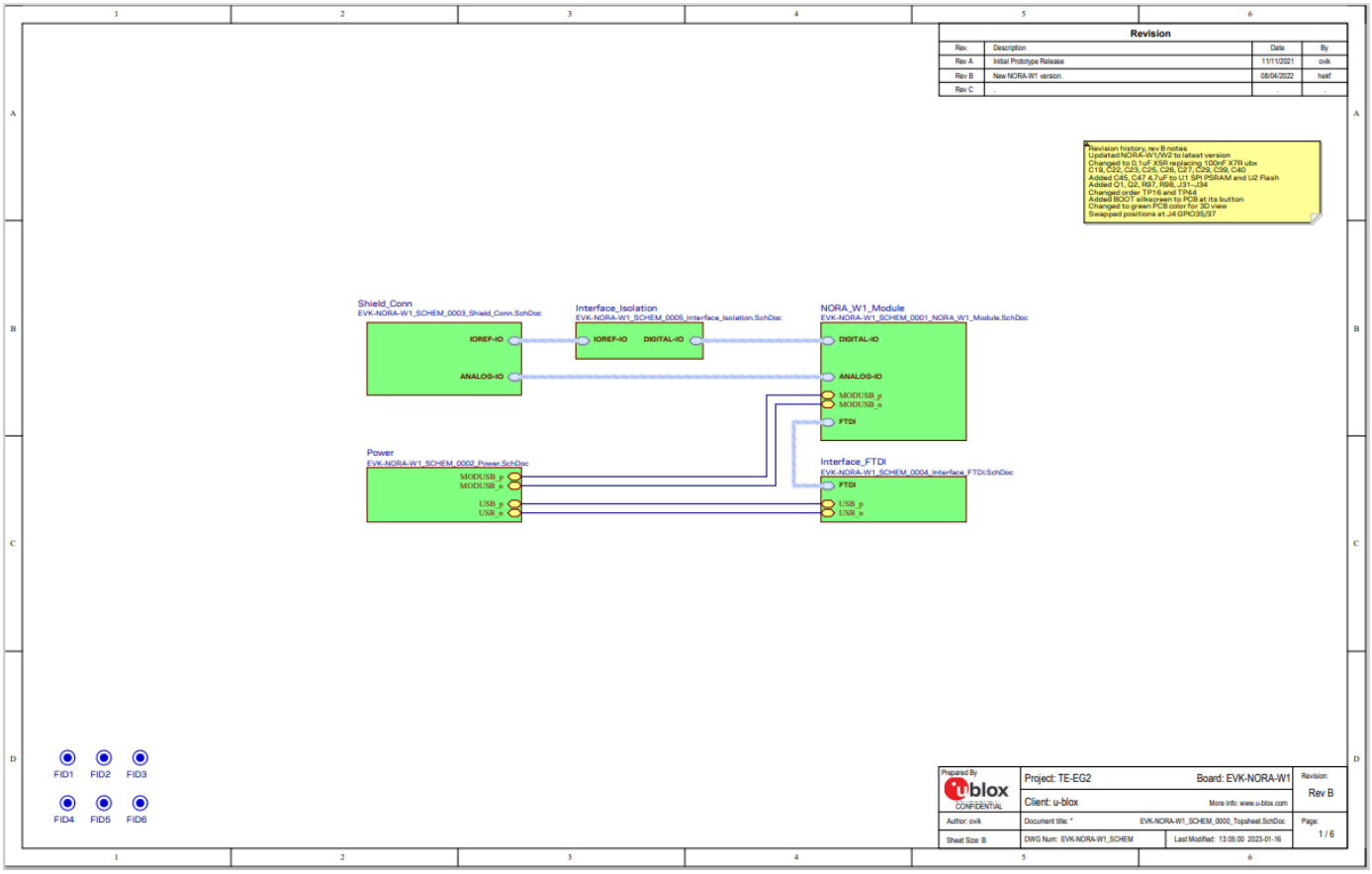

Figure 20: Top page

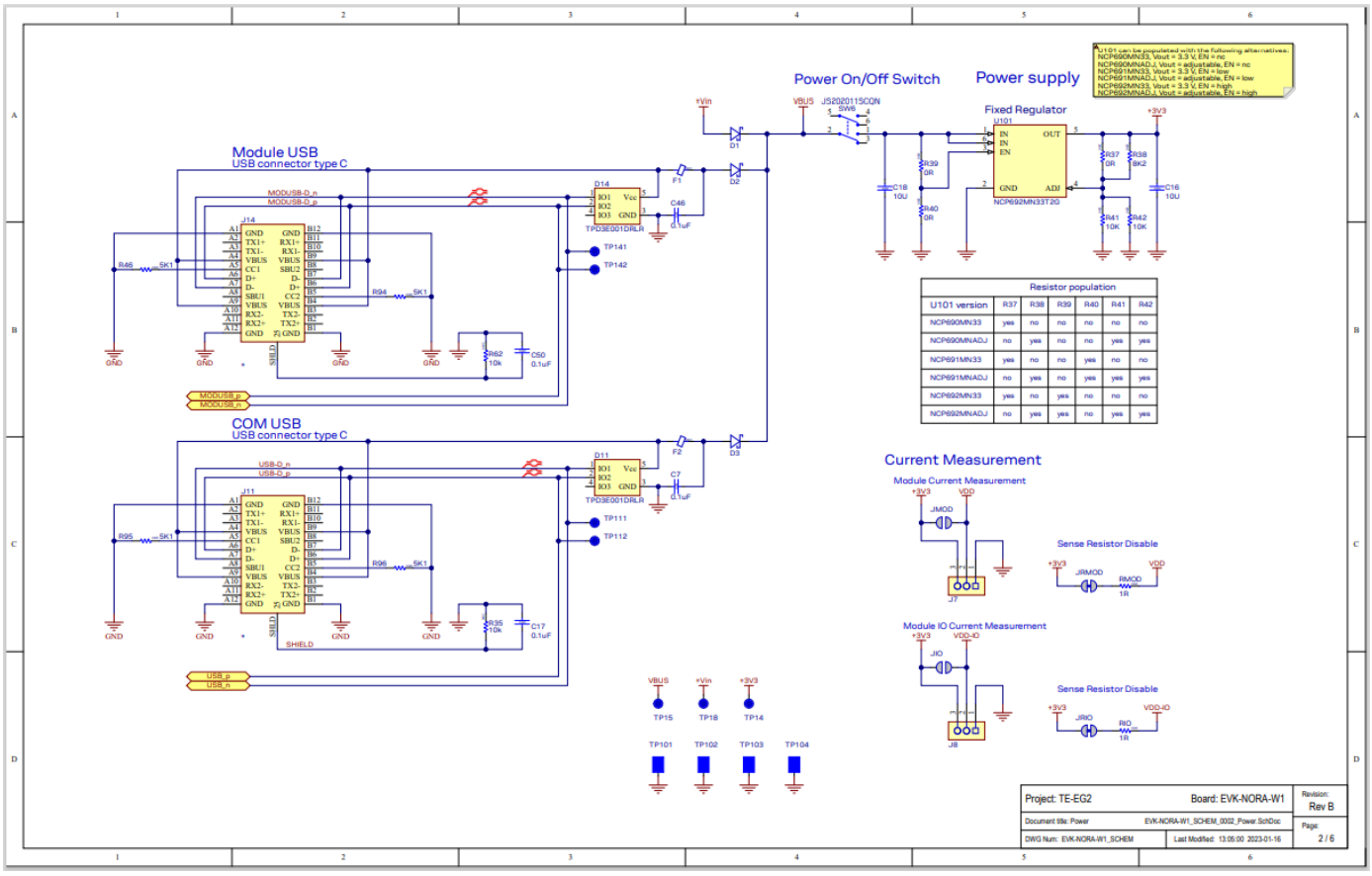

Figure 21: Power

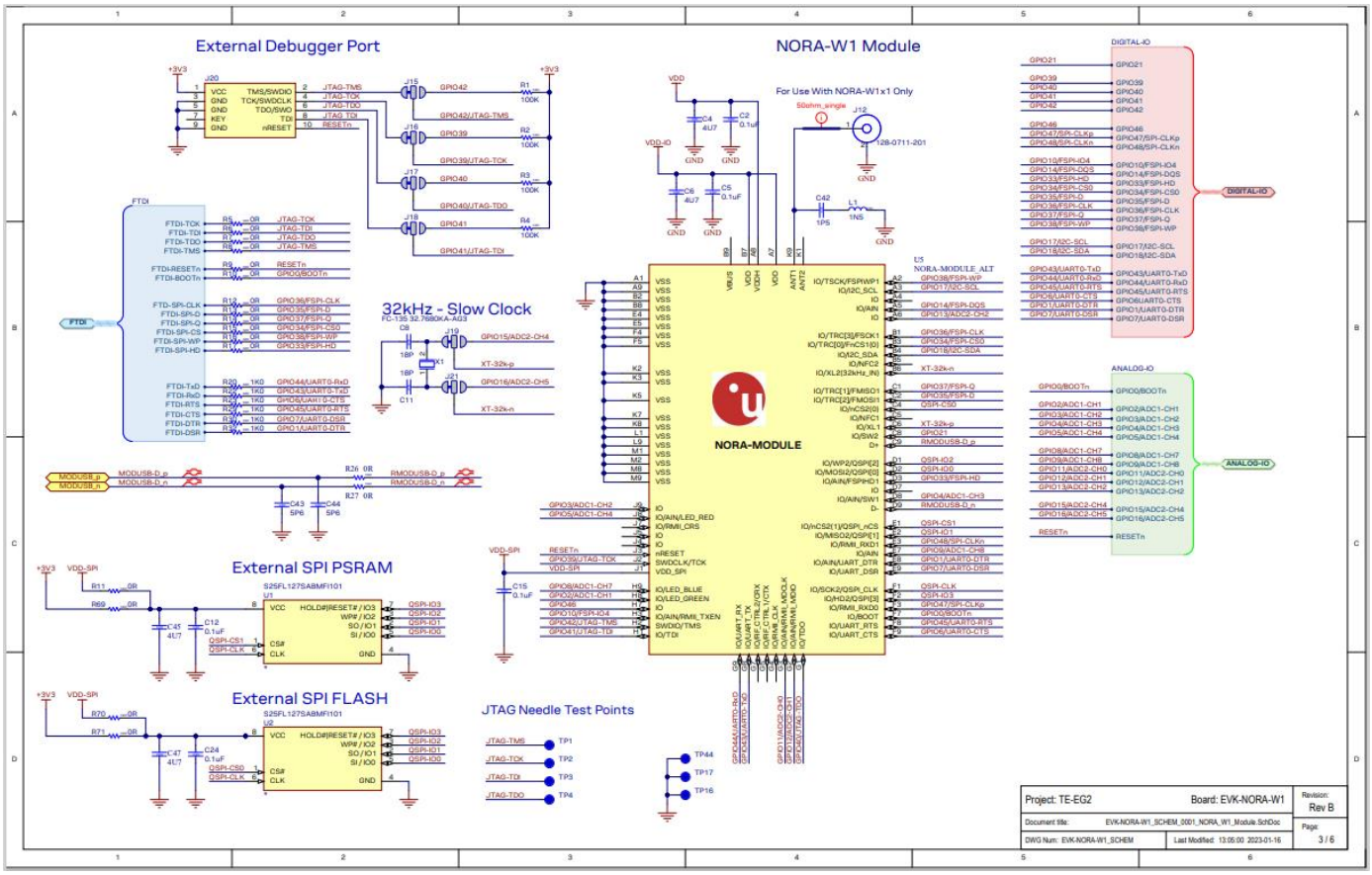

Figure 22: NORA-W1 module

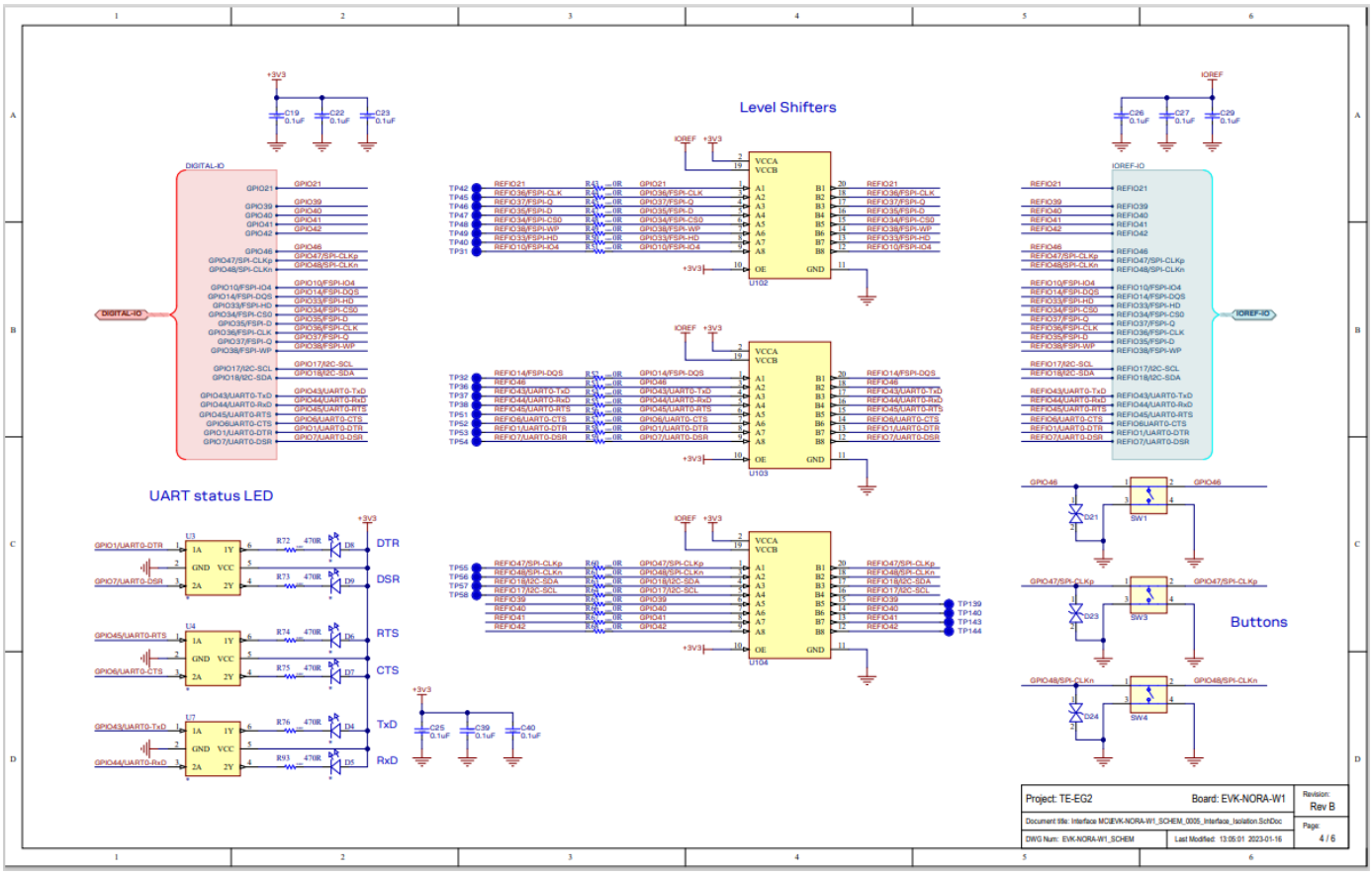

Figure 23: Interface Isolation

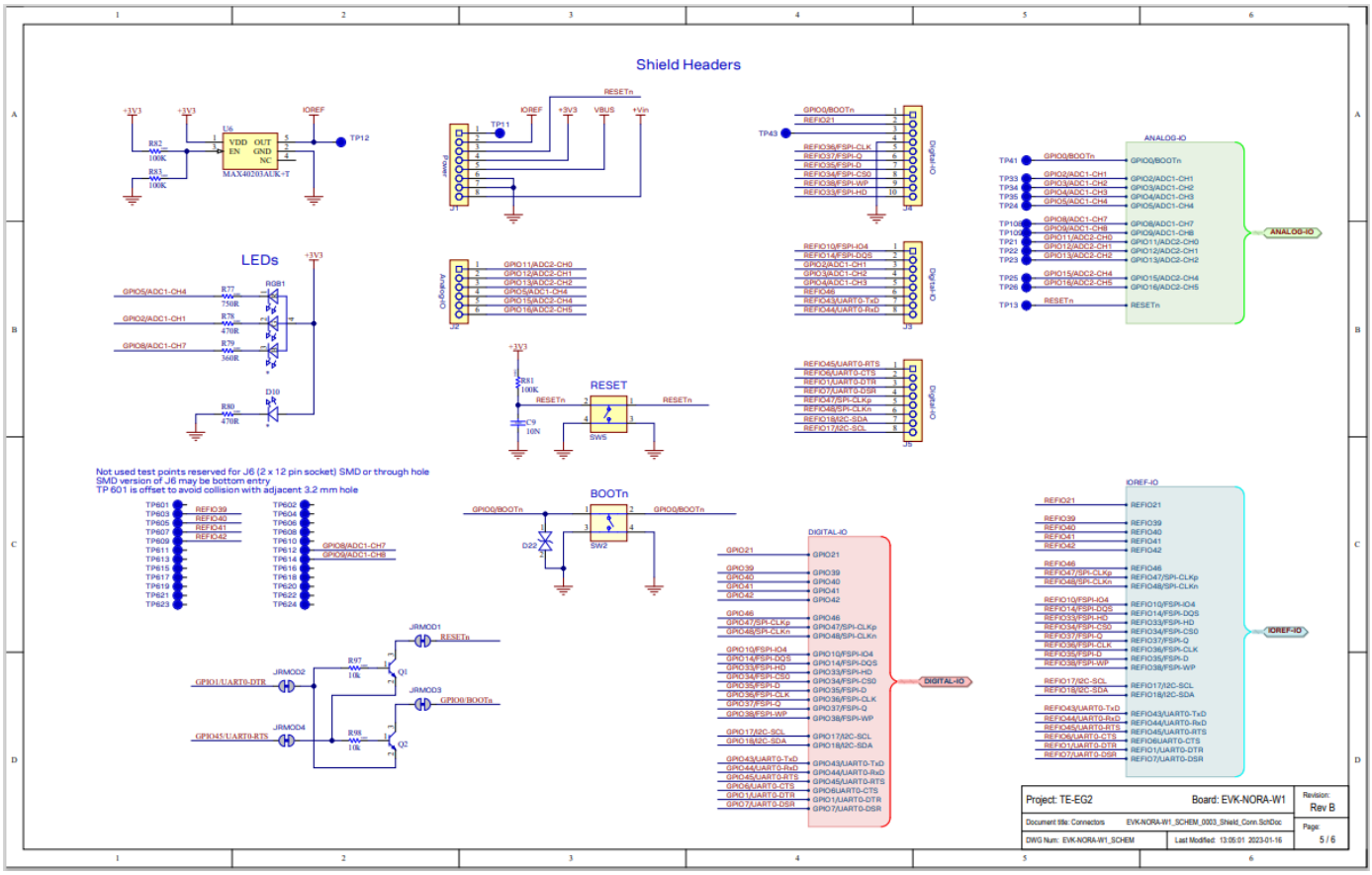

Figure 24: Shield connectors

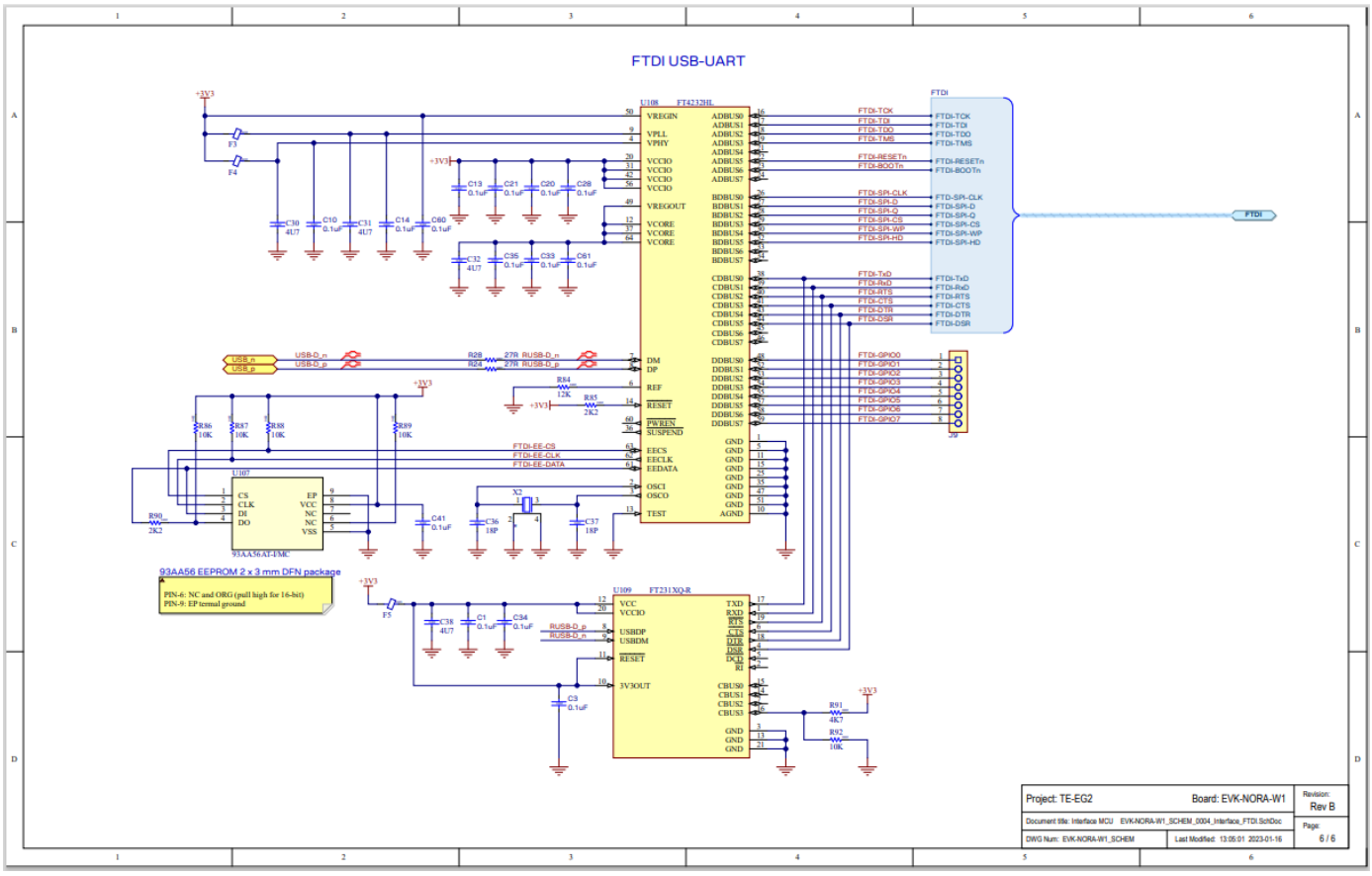

Figure 25: Interface FTDI

B Assembly drawings

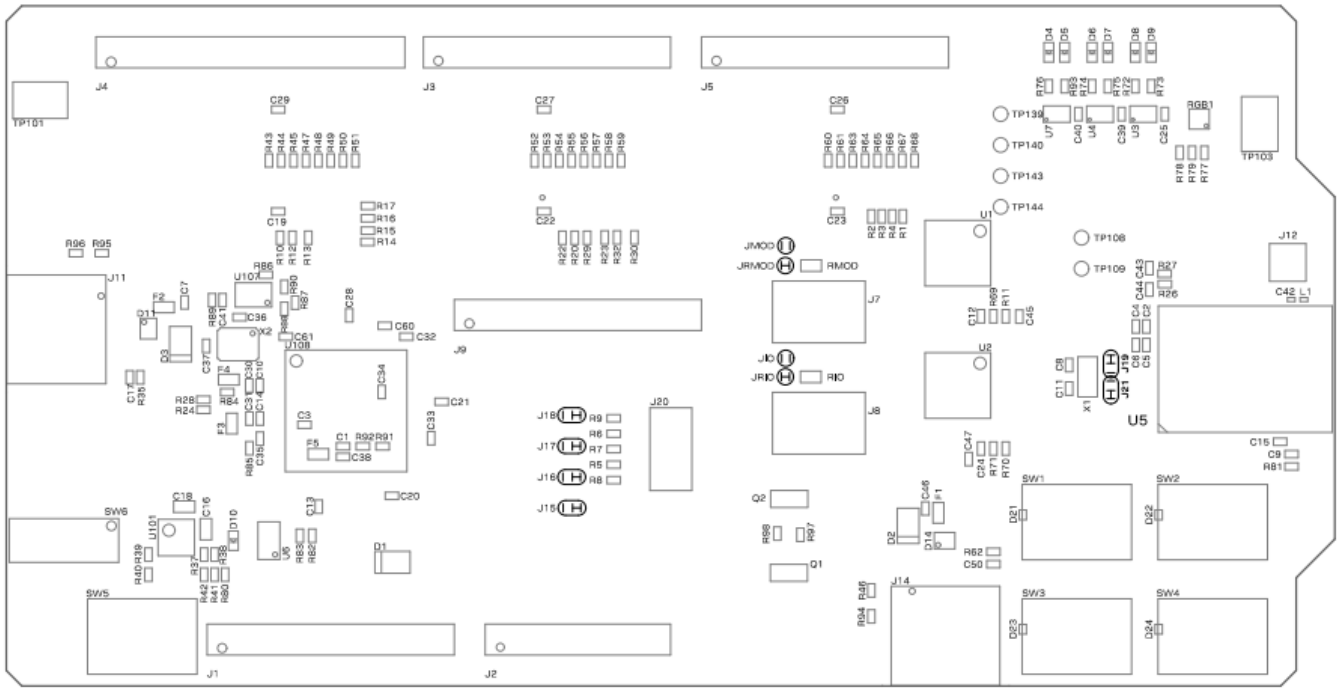

Figure 26: Top layer

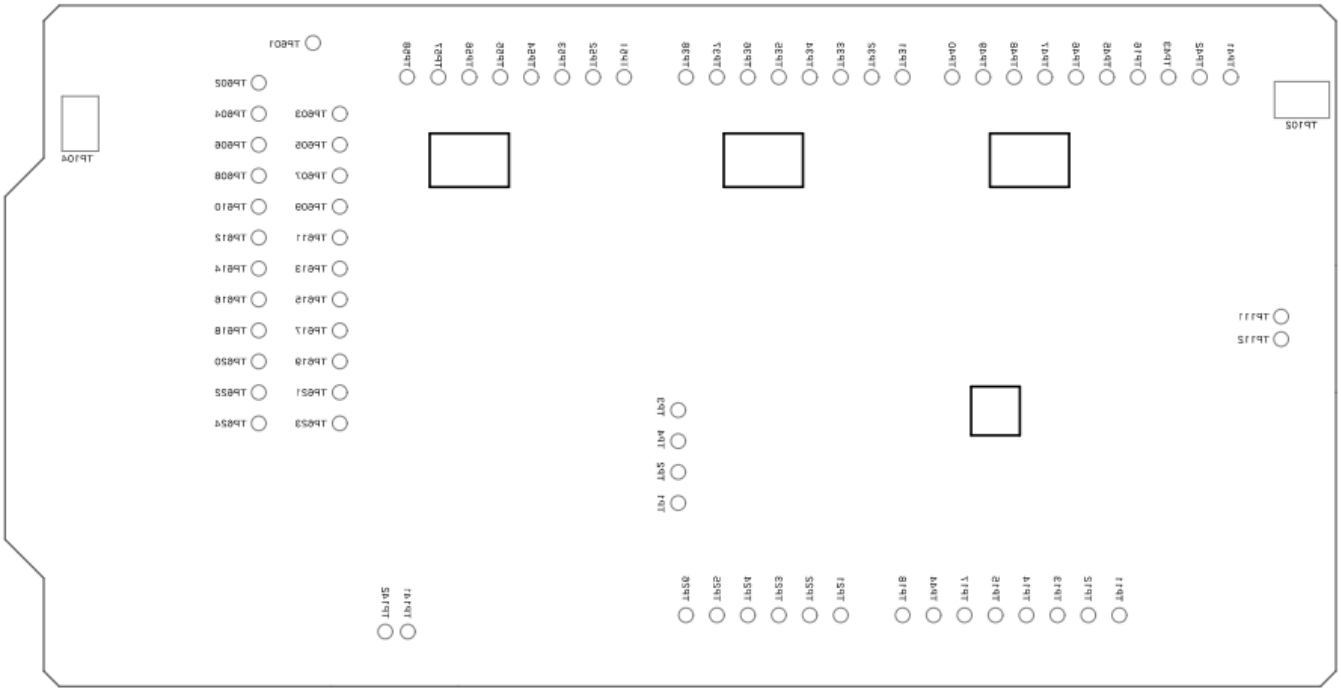

Figure 27: Bottom layer

C Glossary

Abbreviation	Definition
CPU	Central Processing Unit
CTS	Clear To Send
DC	Direct Current
DC-DC	DC to DC converter
DFU	Device Firmware Update
EVK	Evaluation Kit
FICR	Factory Information Configuration Register
GPIO	General Purpose Input / Output
LDO	Low Drop-Out voltage regulator
LE	Low Energy
LED	Light Emitting Diode
LF	Low Frequency
LiPo	Lithium-Polymer battery
NCS	nRF Connect SDK
NFC	Near-Field Communications
QSPI	Quad Serial Peripheral Interface
RC	Resistor-Capacitor network
RTS	Request To Send
RXD	Receive data signal
SES	SEGGER Embedded Studio
SIG	Special Interest Group
SoC	System on Chip
SPI	Serial Peripheral Interface
TXD	Transmit data signal
UICR	User Information Configuration Register
USB	Universal Serial Bus

Table 14: Explanation of the abbreviations and terms used

Related documentation

[1] NORA-W10 data sheet, UBX-21036702
[2] NORA-W10 system integration manual, UBX-22005601
[3] FTDI FT231XQ-R Datasheet, FT231X (ftdichip.com)
[4] Arduino website, https://www.arduino.cc
[5] https://github.com/espressif/esptool

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	29-May-2022	ovik, hekf	Initial release for EVK-NORA-W10 PT2
R02	22-Jul-2022	hekf	Editorial changes in all chapters. Added hardware Overview and updated Setting up the evaluation board. Removed unused components in figures showing top-side, board layout. Described limitations for expanding the internal flash memory of the module with Quad SPI PSRAM in QSPI memory. Revised Buttons, LEDs, Jumpers, and Header pin-out with other miscellaneous changes throughout the document.
R03	14-Oct-2022	hekf	Added Key features and JTAG debug interface section. Replaced product image on cover page. Added Block diagram, Solder-bridge jumper overview, Automatic bootloader description, and table data describing available test points in the Jumpers section. Included other miscellaneous changes throughout the document.
R04	22-Mar-2023	hekf	Added description of external memories in section QSPI memory and EVK-NORA-W10 block diagram. Added Schematics and Assembly drawings.
R05	13-Apr-2023	hekf	Updated document to Early production information: Added section, External PSRAM. Updated Block diagram. Updated USB interfaces. Added schematics and layout in Appendix. Added callout to show header J11 in Header pin-out. Other minor editorial changes.

Contact

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