High Frequency, Automotive AEC-Q100 Oscillator



Features

- AEC-Q100 with extended temperature range (-55°C to 125°C)
- Frequencies between 115.2 MHz and 137 MHz accurate to 6 decimal points
- 100% pin-to-pin drop-in replacement to quartz-based XO
- Excellent total frequency stability as low as ±20 ppm
- Industry best G-sensitivity of 0.1 PPB/G
- Low power consumption of 4.9 mA typical at 1.8 V
- Standby mode for longer battery life
- LVCMOS/LVTTL compatible output
- Industry-standard packages: 2.0 x 1.6, 2.5 x 2.0, 3.2 x 2.5, 5.0 x 3.2, 7.0 x 5.0 mm x mm
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Electrical Characteristics

Table 1. Electrical Characteristics

Applications

- Automotive, extreme temperature and other high-rel electronics
- Infotainment systems, collision detection devices, and in-vehicle networking
- Powertrain control

Related products for automotive applications.

For aerospace and defense applications SiTime recommends using only Endura[™] SiT8945.



All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and nominal supply voltage.

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition
				Frequ	ency Rang	e
Output Frequency Range	f	115.20	-	137	MHz	Refer to Tables 13 to 15 for the exact list of supported frequencies
			F	requency \$	Stability an	d Aging
Frequency Stability	F_stab	-20	-	+20	ppm	Inclusive of Initial tolerance at 25°C, 1 st year aging at 25°C, and
		-25	-	+25	ppm	variations over operating temperature, rated power supply voltage and load (15 pF ±10%).
		-30	-	+30	ppm	
		-50	-	+50	ppm	
			0	perating T	emperatur	eRange
Operating Temperature	T_use	-40	-	+85	°C	AEC-Q100 Grade 3
Range (ambient)		-40	-	+105	°C	AEC-Q100 Grade 2
		-40	-	+125	°C	AEC-Q100 Grade 1
		-55	-	+125	°C	Extended cold, AEC-Q100 Grade1
			Supply	Voltage an	d Current	Consumption
Supply Voltage	Vdd	1.62	1.8	1.98	V	All voltages between 2.25 V and 3.63 V including 2.5 V, 2.8 V, 3.0 V
		2.25	-	3.63	V	and 3.3 V are supported. Contact SiTime for 1.5 V support
Current Consumption	ldd	I	6	8	mA	No load condition, f = 125 MHz, Vdd = 2.25 V to 3.63 V
		I	4.9	6	mA	No load condition, f = 125 MHz, Vdd = 1.62 V to 1.98 V
Standby Current	I_std	-	2.6	-	μΑ	Vdd = 2.8 V to 3.3 V, \overline{ST} = Low, Output is weakly pulled down
		-	1.4	-	μΑ	Vdd = 2.5 V, \overline{ST} = Low, Output is weakly pulled down
		-	0.6	-	μΑ	Vdd = 1.8 V, \overline{ST} = Low, Output is weakly pulled down
			LV	CMOS Out	tput Charac	cteristics
Duty Cycle	DC	45	-	55	%	
Rise/Fall Time	Tr, Tf	-	1.5	3	ns	Vdd = 2.25 V - 3.63 V, 20% - 80%
		-	1.2	2.5	ns	Vdd = 1.8 V, 20% - 80%
Output High Voltage	VOH	90%	-	-	Vdd	IOH = -4 mA (Vdd = 3.0 V or 3.3 V) IOH = -3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOH = -2 mA (Vdd = 1.8 V)
Output Low Voltage	VOL	-	_	10%	Vdd	IOL = 4 mA (Vdd = 3.0 V or 3.3 V) IOL = 3 mA (Vdd = 2.8 V and Vdd = 2.5 V) IOL = 2 mA (Vdd = 1.8 V)



Table 1. Electrical Characteristics (continued)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Condition	
				Input C	haracteris	tics	
Input High Voltage	VIH	70%	-	-	Vdd	Pin 1, OE or ST	
Input Low Voltage	VIL	-	-	30%	Vdd	Pin 1, OE or ST	
Input Pull-up Impedance	Z_in	-	100	-	kΩ	Pin 1, OE logic high or logic low, or \overline{ST} logic high	
		2	-	-	MΩ	Pin 1, ST logic low	
			:				
Startup Time	T_start	-	-	5.5	ms	Measured from the time Vdd reaches its rated minimum value	
Enable/Disable Time	T_oe	-	-	130	ns	f = 115.20 MHz. For other frequencies, T_oe = 100 ns + 3 * cycles	
Resume Time	T_resume	-	-	5	ms	Measured from the time ST pin crosses 50% threshold	
			Input CharacteristicsVddPin 1, OE or \overline{ST} -30%VddPin 1, OE or \overline{ST} 100-k Ω Pin 1, OE or \overline{ST} M Ω Pin 1, OE logic high or logic low, or \overline{ST} M Ω Pin 1, \overline{ST} logic lowStartup and Resume Timing-5.5ms-130nsf = 115.20 MHz. For other frequencies, T-5msMeasured from the time ST pin crossesJitter1.62.5psf = 125 MHz, 2.25 V to 3.63 V1.83psf = 125 MHz, 1.8 V1220psf = 125 MHz, Vdd = 2.5 V, 2.8 V, 3.0 V or1430psf = 125 MHz, Vdd = 1.8 V0.7-psf = 125 MHz, Integration bandwidth = 90				
RMS Period Jitter	T_jitt	-	1.6	2.5	ps	f = 125 MHz, 2.25 V to 3.63 V	
		-	1.8	3	ps	f = 125 MHz, 1.8 V	
Peak-to-peak Period Jitter	T_pk	-	12	20	ps	f = 125 MHz, Vdd = 2.5 V, 2.8 V, 3.0 V or 3.3 V	
		-	14	30	ps	f = 125 MHz, Vdd = 1.8 V	
RMS Phase Jitter (random)	T_phj	-	0.7	-	ps	f = 125 MHz, Integration bandwidth = 900 kHz to 7.5 MHz	
		-	1.5	-	ps	f = 125 MHz, Integration bandwidth = 12 kHz to 20 MHz	

Table 2. Pin Description

Pin	Symbol	Functionality		
Output Enal		Output Enable	H ^[1] : specified frequency output L: output is high impedance. Only output driver is disabled.	OI
1	OE/ ST /NC	Standby	H ^[1] : specified frequency output L: output is low (weak pull down). Device goes to sleep mode. Supply current reduces to I_std.	
		No Connect	Any voltage between 0 and Vdd or Open ^[1] : Specified frequency output. Pin 1 has no function.	
2	GND	Power	Electrical ground ^[2]	Fig
3	OUT	Output	Oscillator output	
4	VDD	Power	Power supply voltage ^[2]	



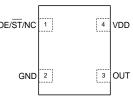


Figure 1. Pin Assignments

Notes:

1. In OE or ST mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.

2. A capacitor of value 0.1 μF or higher between Vdd and GND is required.



Table 3. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	C°
Vdd	-0.5	4	V
Electrostatic Discharge	-	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	-	260	°C
Junction Temperature ^[3]	-	150	С°

Note:

3. Exceeding this temperature for extended period of time may damage the device.

Table 4. Thermal Consideration^[4]

Package	θJA, 4 Layer Board (°C/W)	θJA, 2 Layer Board (°C/W)	θJC, Bottom (°C/W)
7050	142	273	30
5032	97	199	24
3225	109	212	27
2520	117	222	26
2016	152	252	36

Note:

4. Refer to JESD51 for θ JA and θ JC definitions, and reference layout used to determine the θ JA and θ JC values in the above table.

Table 5. Maximum Operating Junction Temperature^[5]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature		
85°C	93°C		
105°C	113°C		
125°C	133°C		

Note:

5. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 6. Environmental Compliance

Parameter	Condition/Test Method	
Mechanical Shock	MIL-STD-883F, Method2002	
Mechanical Vibration	MIL-STD-883F, Method2007	
Temperature Cycle	JESD22, Method A104	
Solderability	MIL-STD-883F, Method2003	
Moisture Sensitivity Level	MSL1 @ 260°C	



Test Circuit and Waveform

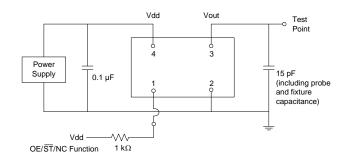


Figure 2. Test Circuit^[6]

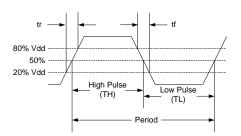
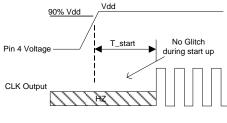


Figure 3. Waveform^[6]

Note:

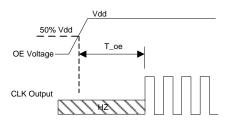
6. Duty Cycle is computed as Duty Cycle =TH/Period.

Timing Diagrams



T_start: Time to start from power-off

Figure 4. Startup Timing (OE/ ST Mode)^[7]

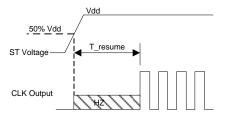


T_oe: Time to re-enable the clock output

Figure 6. OE Enable Timing (OE Mode Only)

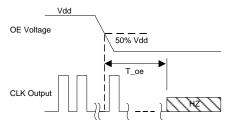
Note:

7. SiT8925 has "no runt" pulses and "no glitch" output during startup or resume.



T_resume: Time to resume from \overline{ST}

Figure 5. Standby Resume Timing (ST Mode Only)



T_oe: Time to put the output in High Z mode

Figure 7. OE Disable Timing (OE Mode Only)



Performance Plots^[8]

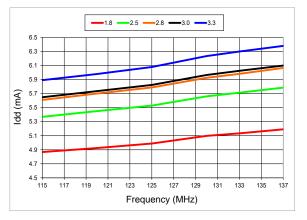
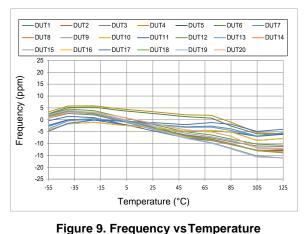


Figure 8. Idd vs Frequency



-1.8 V -2.5 V -2.8 V -3.0 V -3.3 V 55 54 53 52

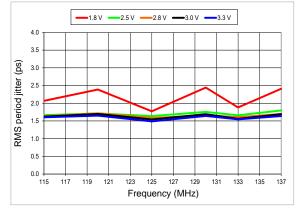


Figure 10. RMS Period Jitter vs Frequency

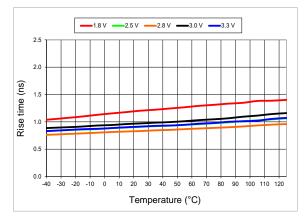
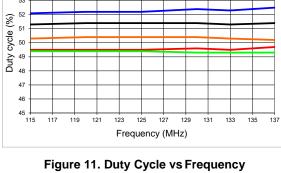


Figure 12. 20%-80% Rise Time vs Temperature



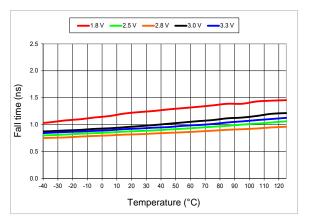


Figure 13. 20%-80% Fall Time vs Temperature



Performance Plots^[8]

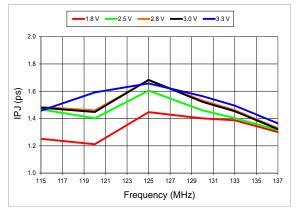


Figure 14. RMS Integrated Phase Jitter Random (12 kHz to 20 MHz) vs Frequency^[9]

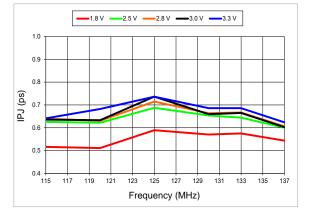


Figure 15. RMS Integrated Phase Jitter Random (900 kHz to 20 MHz) vs Frequency^[9]

Notes:

8. All plots are measured with 15 pF load at room temperature, unless otherwise stated.

9. Phase noise plots are measured with Agilent E5052B signal source analyzer.

Programmable Drive Strength

The SiT8925 includes a programmable drive strength feature to provide a simple, flexible tool to optimize the clock rise/fall time for specific applications. Benefits from the programmable drive strength feature are:

- Improves system radiated electromagnetic interference (EMI) by slowing down the clock rise/fall time.
- Improves the downstream clock receiver's (RX) jitter by decreasing (speeding up) the clock rise/fall time.
- Ability to drive large capacitive loads while maintaining full swing with sharp edge rates.

For more detailed information about rise/fall time control and drive strength selection, see the SiTime Application Notes section.

EMI Reduction by Slowing Rise/Fall Time

Figure 16 shows the harmonic power reduction as the rise/fall times are increased (slowed down). The rise/fall times are expressed as a ratio of the clock period. For the ratio of 0.05, the signal is very close to a square wave. For the ratio of 0.45, the rise/fall times are very close to near-triangular waveform. These results, for example, show that the 11th clock harmonic can be reduced by 35 dB if the rise/fall edge is increased from 5% of the period to 45% of the period.

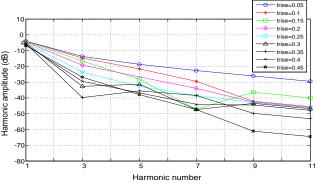


Figure 16. Harmonic EMI reduction as a Function of Slower Rise/Fall Time

Jitter Reduction with Faster Rise/Fall Time

Power supply noise can be a source of jitter for the downstream chipset. One way to reduce this jitter is to speed up the rise/fall time of the input clock. Some chipsets may also require faster rise/fall time in order to reduce their sensitivity to this type of jitter. Refer to the Rise/Fall Time Tables (Table 7 to Table 11) to determine the proper drive strength.

High Output Load Capability

The rise/fall time of the input clock varies as a function of the actual capacitive load the clock drives. At any given drive strength, the rise/fall time becomes slower as the output load increases. As an example, for a 3.3 V SiT8925 device with default drive strength setting, the typical rise/fall time is 0.46 ns for 5 pF output load. The typical rise/fall time slows down to 1 ns when the output load increases to 15 pF. One can choose to speed up the rise/fall time to 0.72 ns by then increasing the driven strength setting on the SiT8925 to "F".

The SiT8925 can support up to 30 pF in maximum capacitive loads with up to 3 additional drive strength settings. Refer to the Rise/Tall Time Tables (Table 7 to 11) to determine the proper drive strength for the desired combination of output load vs. rise/fall time.

SiT8925 Drive Strength Selection

Tables 7 through 11 define the rise/fall time for a given capacitive load and supply voltage.

- 1. Select the table that matches the SiT8925 nominal supply voltage (1.8 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V)
- 2. Select the capacitive load column that matches the application requirement (5 pF to 30 pF)
- **3.** Under the capacitive load column, select the desired rise/fall times.
- 4. The left-most column represents the part number code for the corresponding drive strength.
- **5.** Add the drive strength code to the part number for ordering purposes.

Calculating Maximum Frequency

Based on the rise and fall time data given in Tables 7 through 11, the maximum frequency the oscillator can operate with guaranteed full swing of the output voltage over temperature as follows:

Max Frequency =
$$\frac{1}{5 \text{ x Trf}_{20/80}}$$

where $\mathsf{Trf}_\mathsf{20}/\mathsf{80}$ is the typical value for 20%-80% rise/fall time.

Example 1

Calculate f_{MAX} for the following condition:

- Vdd = 3.3 V (Table 11)
- Capacitive Load: 30 pF
- Desired Tr/f time = 1.46 ns (rise/fall time part number code = U)

Part number for the above example: SiT8925BAE12-18E-137.000000

Drive strength code is inserted here. Default setting is "-"



Rise/Fall Time (20% to 80%) vs CLOAD Tables^[10]

Table 7. Vdd = 1.8 V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)					
Drive Strength\ C _{LOAD}	5 pF	15 pF			
Т	0.93	n/a			
E	0.78	n/a			
U	0.70	1.48			
F or "-": default	0.65	1.30			

Table 9. Vdd = 2.8 V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)					
Drive Strength \ C _{LOAD}	5 pF	15 pF	30 pF		
R	1.29	n/a	n/a		
В	0.97	n/a	n/a		
T or "-": default	0.55	1.12	n/a		
E	0.44	1.00	n/a		
U	0.34	0.88	n/a		
F	0.29	0.81	1.48		

Table 11. Vdd = 3.3 V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)					
Drive Strength $\ C_{LOAD}$	5 pF	15 pF	30 pF		
R	1.16	n/a	n/a		
В	0.81	n/a	n/a		
T or "-": default	0.46	1.00	n/a		
E	0.33	0.87	n/a		
U	0.28	0.79	1.46		
F	0.25	0.72	1.31		

Note:

10. "n/a" indicates that the resulting rise/fall time from the respective combination of the drive strength and output load does not provide rail-to-rail swing and is not available.

Table 8. Vdd = 2.5 V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)					
Drive Strength $\ C_{LOAD}$	5 pF	15 pF			
R	1.45	n/a			
В	1.09	n/a			
T or "-": default	0.62	1.28			
E	0.54	1.00			
U	0.43	0.96			
F	0.34	0.88			

Table 10. Vdd = 3.0 V Rise/Fall Times for Specific CLOAD

Rise/Fall Time Typ (ns)					
Drive Strength $\ C_{LOAD}$	5 pF	15 pF	30 pF		
R	1.22	n/a	n/a		
В	0.89	n/a	n/a		
T or "-": default	0.51	1.00	n/a		
E	0.38	0.92	n/a		
U	0.30	0.83	n/a		
F	0.27	0.76	1.39		



Pin 1 Configuration Options (OE, \overline{ST} , or NC)

Pin 1 of the SiT8925 can be factory-programmed to support three modes: Output enable (OE), Standby (\overline{ST}) or No Connect (NC). These modes can also be programmed with the Time Machine II using Field Programmable Oscillators.

Output Enable (OE) Mode

In the OE mode, applying logic Low to the OE pin only disables the output driver and puts it in Hi-Z mode. The core of the device continues to operate normally. Power consumption is reduced due to the inactivity of the output. When the OE pin is pulled High, the output is typically enabled in <1 μ s.

Standby (ST) Mode

In the \overline{ST} mode, a device enters into the standby mode when Pin 1 pulled Low. All internal circuits of the device are turned off. The current is reduced to a standby current, typically in the range of a few μ A. When \overline{ST} is pulled High, the device goes through the "resume" process, which can take up to 5 ms.

No Connect (NC) Mode

In the NC mode, the device always operates in its normal mode and outputs the specified frequency regardless of the logic level on pin 1.

Table 12 below summarizes the key relevant parameters in the operation of the device in OE, \overline{ST} , or NC mode.

	OE	ST	NC
Active current 125 MHz (max. 1.8 V)	6 mA	6 mA	6 mA
OE disable current (max. 1.8 V)	4 mA	N/A	N/A
Standby current (typical 1.8 V)	N/A	0.6 uA	N/A
OE enable time at 115 MHz (max)	130 ns	N/A	N/A
Resume time from standby (max, all frequency)	N/A	5 ms	N/A
Output driver in OE disable/standby mode	High Z	Weak pull-down	N/A

Table 12. OE vs. ST vs. NC

Output on Startup and OE Enable

The SiT8925 comes with gated output. Its clock output is accurate to the rated frequency stability within the first pulse from initial device startup.

In addition, the SiT8925 supports "no runt" pulses and "no glitch" output during startup or when the device output driver is enabled as shown in the waveform captures in Figure 17 and Figure 18.



Figure 17. Startup Waveform vs. Vdd

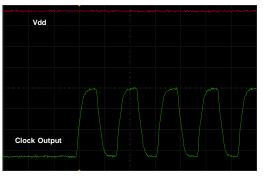
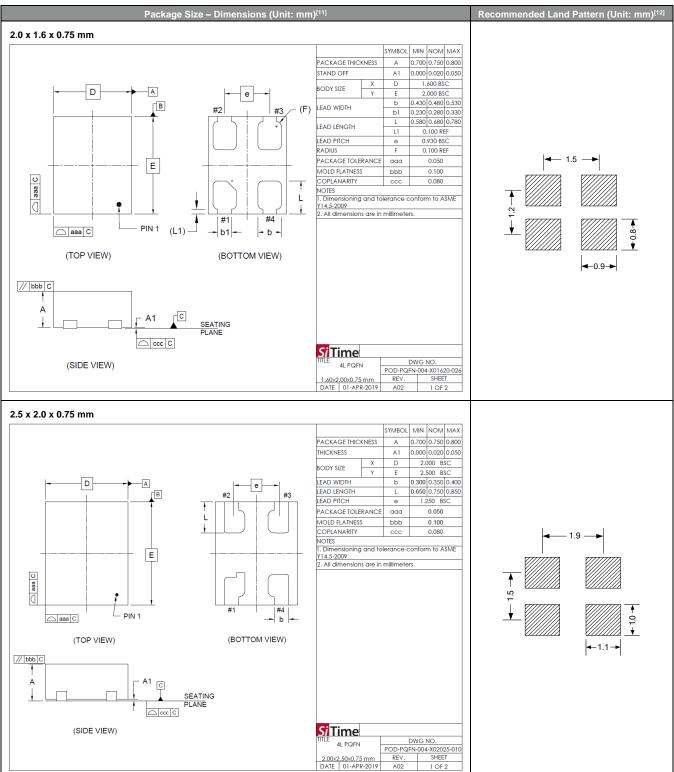


Figure 18. Startup Waveform vs. Vdd (Zoomed-in View of Figure 17)

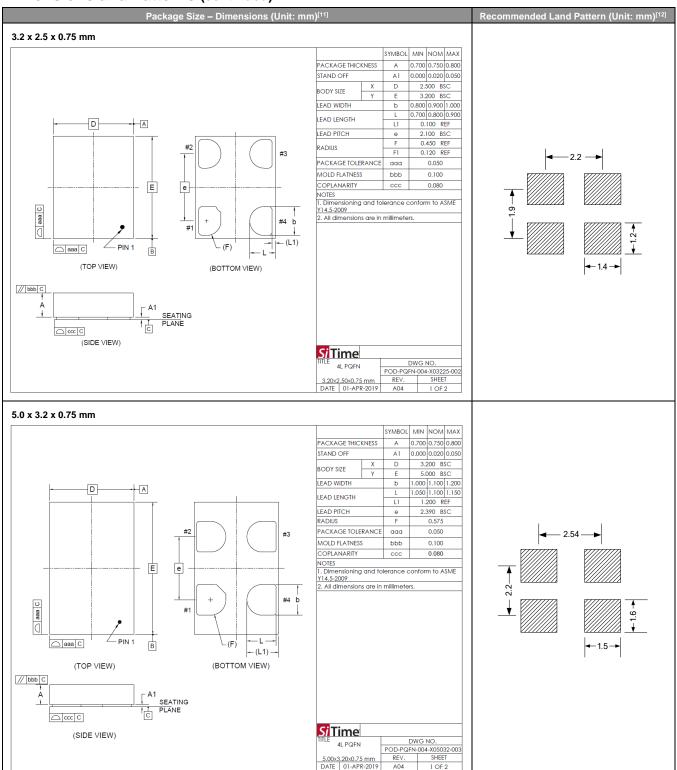


Dimensions and Patterns



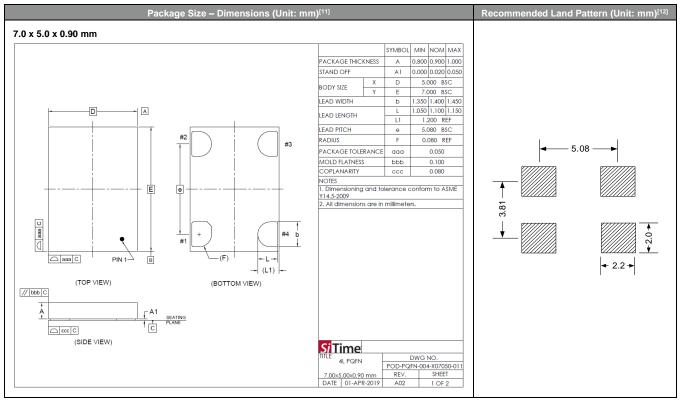


Dimensions and Patterns (continued)





Dimensions and Patterns (continued)



Notes:

- 11. Top marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
- 12. A capacitor of value 0.1 μF or higher between Vdd and GND is required.



Ordering Information

The following part number guide is for reference only. To customize and build an exact part number, use the SiTime Part Number Generator.

SiT8925	5BA-12	2-18E	-125.	123456D
Part Family "SiT8925" Revision Letter "B" is the revision Temperature Range "I" -40°C to 85°C, AEC-Q100 Grade3 "E" -40°C to 105°C, AEC-Q100 Grade2 "A" -40°C to 125°C, AEC-Q100 Grade1 "M" -55°C to 125°C, Ext. cold AEC-Q100 Grade1 "M" -55°C to 125°C, Ext. cold AEC-Q100 Grade1 "Cutput Drive Strength "-" Default (datasheet limits) See Tables 7 to 11 for rise/fall times "R" "E"				Packing Method "T": 12 mm Tape & Reel, 3 ku reel "Y": 12 mm Tape & Reel, 1 ku reel "D": 8 mm Tape & Reel, 1 ku reel "E": 8 mm Tape & Reel, 1 ku reel Blank for Bulk Frequency Refer to the Supported Frequency Tables Below Feature Pin "E" for Output Enable "S" for Standby "N" for No Connect Supply Voltage ^[13] "18" for 1.8 V "25" for 2.5 V
"B" "U" "T" "F" Package Size				"28" for 2.8 V "30" for 3.0 V "33" for 3.3 V "XX" for 2.5 V -10% to 3.3 V +10%
 "7" 2.0 x 1.6 mm "1" 2.5 x 2.0 mm "2" 3.2 x 2.5 mm "3" 5.0 x 3.2 mm "8" 7.0 x 5.0 mm 				Frequency Stability "1" for ±20 ppm "2" for ±25 ppm "8" for ±30 ppm "3" for ±50 ppm

Note:

13. The voltage portion of the SiT8925 part number consists of two characters that denote the specific supply voltage of the device. The SiT8925 supports either 1.8 V ±10% or any voltage between 2.25 V and 3.63 V. In the 1.8 V mode, one can simply insert 18 in the part number. In the 2.5 V to 3.3 V mode, two digits such as 18, 25 or 33 can be used in the part number to reflect the desired voltage. Alternatively, "XX" can be used to indicate the entire operating voltage range from 2.25 V to 3.63 V.

Table 13. Supported Frequencies (-40°C to +85°C)^[14]

Frequency Range		
Min. Max.		
115.200000 MHz	137.000000 MHz	

Table 14. Supported Frequencies (-40°C to +105°C or -40°C to +125°C)^[14, 15]

Frequency Range				
Min.	Max.			
115.194001 MHz	117.810999 MHz			
118.038001 MHz	118.593999 MHz			
118.743001 MHz	122.141999 MHz			
122.705001 MHz	123.021999 MHz			
123.348001 MHz	137.000000 MHz			

Table 15. Supported Frequencies (-55°C to +125°C)^[14, 15]

Frequency Range			
Min.	Max.		
119.342001 MHz	120.238999 MHz		
120.262001 MHz	121.169999 MHz		
121.243001 MHz	121.600999 MHz		
123.948001 MHz	137.000000 MHz		

Notes:

14. Any frequency within the min and max values in the above tables are supported with 6 decimal places of accuracy.

15. Please contact SiTime for frequencies that are not listed in the tables above.



Table 16. Ordering Codes for Supported Tape & Reel Packing Method

Device Size	16 mm T&R (3 ku)	16 mm T&R (1 ku)	12 mm T&R (3 ku)	12 mm T&R (1 ku)	8 mm T&R (3 ku)	8 mm T&R (1 ku)
2.0 x 1.6 mm	-	-	-	-	D	E
2.5 x 2.0 mm	-	-	-	-	D	E
3.2 x 2.5 mm	-	-	-	-	D	E
5.0 x 3.2 mm	-	-	Т	Y	-	-
7.0 x 5.0 mm	Т	Y	-	-	-	-



Table 17. Additional Information

Document	Description	Download Link	
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer	
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	http://www.sitime.com/products/field-programmable-oscillators	
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library/manufacturing-notes-sitime-products	
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability	
Performance Reports	Additional performance data such as phase noise, cur- rent consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report	
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes	
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes	

Table 18. Revision History

Revision	Release Date	Change Summary
0.1	28-May-2015	Final production release
1.3	18-Mar-2016	Added the industrial temperature "-40°C to ±85°C" option Added support for ±20 ppm frequency stability Added 12 and 16 mm T&R information to Table 16
1.5	16-Feb-2018	Changed Clock Generator to SOT23 Oscillator
1.6	18-Jul-2018	Added Standby mode option Removed center lines from the package drawings Revised description of temperature range options Updated logo and company address, links and other page layout changes
1.7	22-May-2019	Updated package dimensions Revised startup time specification
1.71	14-Sep-2020	Added more detailed info for the Standby mode
1.72	1-Jan-2023	Updated company disclaimer, links, references and icons

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Supplemental Information

The Supplemental Information section is not part of the datasheet and is for informational purposes only.



Best Reliability

Silicon is inherently more reliable than quartz. Unlike quartz suppliers, SiTime has in-house MEMS and analog CMOS expertise, which allows SiTime to develop the most reliable products. Figure 1 shows a comparison with quartz technology.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal[™] process, which eliminates foreign particles and improves long term aging and reliability
- World-class MEMS and CMOS design expertise



Figure 1. Reliability Comparison^[1]

Best Aging

Unlike quartz, MEMS oscillators have excellent long term aging performance which is why every new SiTime product specifies 10-year aging. A comparison is shown in Figure 2.

Why is SiTime Best in Class:

- SiTime's MEMS resonators are vacuum sealed using an advanced EpiSeal[™] process, which eliminates foreign particles and improves long term aging and reliability
- Inherently better immunity of electrostatically driven MEMS resonator

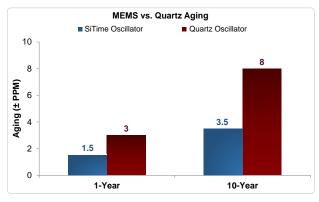


Figure 2. Aging Comparison^[2]

Best Electro Magnetic Susceptibility (EMS)

SiTime's oscillators in plastic packages are up to 54 times more immune to external electromagnetic fields than quartz oscillators as shown in Figure 3.

Why is SiTime Best in Class:

- Internal differential architecture for best common mode noise rejection
- Electrostatically driven MEMS resonator is more immune to EMS

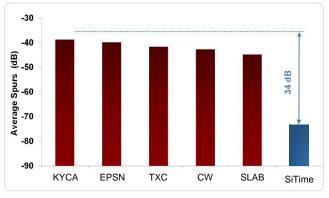


Figure 3. Electro Magnetic Susceptibility (EMS)^[3]

Best Power Supply Noise Rejection

SiTime's MEMS oscillators are more resilient against noise on the power supply. A comparison is shown in Figure 4.

Why is SiTime Best in Class:

- On-chip regulators and internal differential architecture for common mode noise rejection
- MEMS resonator is paired with advanced analog CMOS IC

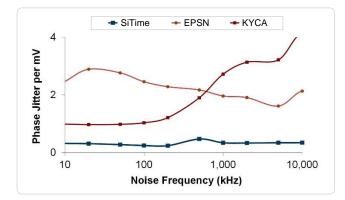


Figure 4. Power Supply Noise Rejection^[4]



Best Vibration Robustness

High-vibration environments are all around us. All electronics, from handheld devices to enterprise servers and storage systems are subject to vibration. Figure 5 shows a comparison of vibration robustness.

Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than quartz
- Center-anchored MEMS resonator is the most robust design

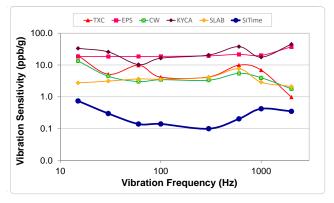


Figure 5. Vibration Robustness^[5]

Figure labels:

- TXC = TXC
- Epson = EPSN
- Connor Winfield = CW
- Kyocera = KYCA
- SiLabs = SLAB
- SiTime = EpiSeal MEMS

Best Shock Robustness

SiTime's oscillators can withstand at least 50,000 g shock. They all maintain their electrical performance in operation during shock events. A comparison with quartz devices is shown in Figure 6.

Why is SiTime Best in Class:

- The moving mass of SiTime's MEMS resonators is up to 3000 times smaller than guartz
- Center-anchored MEMS resonator is the most robust design

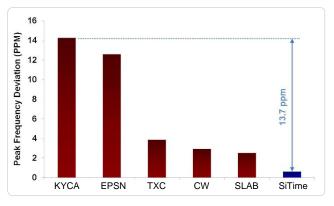


Figure 6. Shock Robustness^[6]



Notes:

- 1. Data source: Reliability documents of named companies.
- 2. Data source: SiTime and quartz oscillator devices datasheets.
- 3. Test conditions for Electro Magnetic Susceptibility (EMS):
 - According to IEC EN61000-4.3 (Electromagnetic compatibility standard)
 - Field strength: 3 V/m
 - Radiated signal modulation: AM 1 kHz at 80% depth
 - Carrier frequency scan: 80 MHz 1 GHz in 1% steps
 - Antenna polarization: Vertical
 - DUT position: Center aligned to antenna

Devices used in this test:

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	SiTime	SiT9120AC-1D2-33E156.250000	MEMS + PLL
EPSN	Epson	EG-2102CA156.2500M-PHPAL3	Quartz, SAW
TXC	TXC	BB-156.250MBE-T	Quartz, 3 rd Overtone
CW	Conner Winfield	P123-156.25M	Quartz, 3 rd Overtone
KYCA	AVX Kyocera	KC7050T156.250P30E00	Quartz, SAW
SLAB	SiLab	590AB-BDG	Quartz, 3 rd Overtone + PLL

4. 50 mV pk-pk Sinusoidal voltage.

Devices used in this test:

Label	Manufacturer	Part Number	Technology
EpiSeal MEMS	SiTime	SiT8208AI-33-33E-25.000000	MEMS + PLL
NDK	NDK	NZ2523SB-25.6M	Quartz
КҮСА	AVX Kyocera	KC2016B25M0C1GE00	Quartz
EPSN	Epson	SG-310SCF-25M0-MB3	Quartz

5. Devices used in this test:

same as EMS test stated in Note 3.

- 6. Test conditions for shock test:
 - MIL-STD-883F Method 2002
 - Condition A: half sine wave shock pulse, 500-g, 1ms
 - Continuous frequency measurement in 100 µs gate time for 10 seconds

Devices used in this test:

- same as EMS test stated in Note 3.
- 7. Additional data, including setup and detailed results, is available upon request to qualified customer. Please contact productsupport@sitime.com.