

## 4.5A Dual High-Speed Power MOSFET Drivers with Enable

### Features

- Enable Functions for Each Driver
- High Peak Output Current: 4.5A
- Wide Supply Voltage Operating Range: 4.5V to 25V
- High Capacitive Load Drive Capability 1800pF in 12ns (typical)
- Short Delay Times: 36ns (typical)
- Matched Rise/Fall Times
- Low Output Impedance: 1.6  $\Omega$  (typical)
- Low Supply Current
- Over-temperature Protection
- Under-voltage Lockout (UVLO)
- Non-overlapped Drive Tech
- Input withstands negative inputs up to 5V
- Available in Green SOP8, DIP8 and DFN8 Packages

### Applications

- Switch Mode Power Supplies
- Power MOSFET Drivers
- Pulse Transformer Drivers
- Line Drivers
- CCD Driver
- Class D Switching Amplifiers

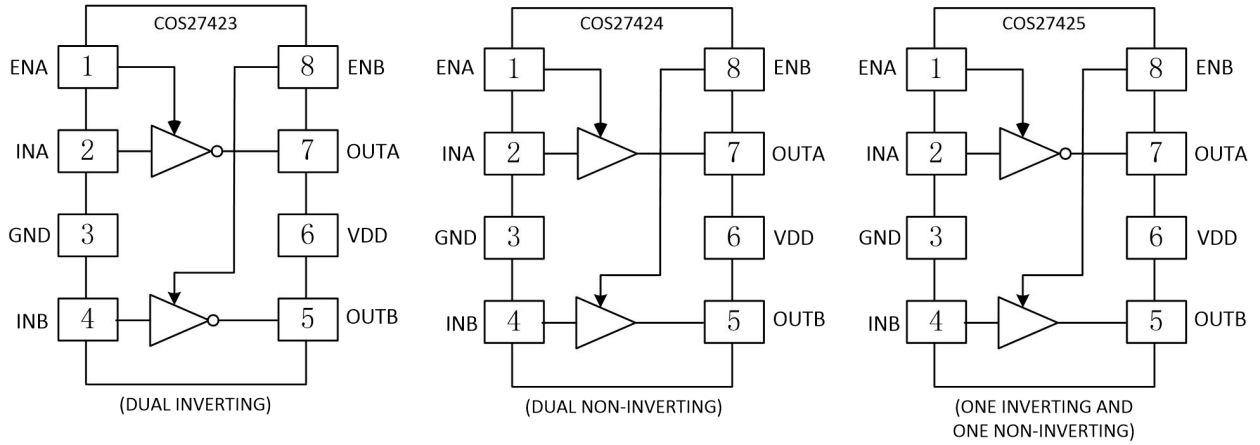
### General Description

The COS27423/4/5 are matched dual power MOSFET drivers. Unique circuit design enables high speed operation capable of delivering peak currents of 4.5A into 1800pF capacitive loads. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. Dynamic switching losses are minimized with non-overlapped drive techniques. These devices are highly latch-up resistant within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin.

The COS27423/4/5 inputs can be driven directly from either TTL or CMOS (1.8V to 25V). In addition, the 300mV of built-in hysteresis provides noise immunity and allows the device to be driven from slow rising or falling waveforms. The COS27423/4/5 provides enable functions (EN) to control the operation of the driver applications. ENA and ENB are implemented on pins 1 and 8 which were previously left unused in the industry standard pin-out. They are internally pulled up to  $V_{DD}$  for active high logic and can be left open for standard operation.

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### 1. Pin Configuration and Functions



COS27423: Outputs out of phase with inputs

COS27424: Outputs in phase with inputs

COS27425: Output A: out of phase with input A;  
Output B: in phase with input B

Figure 1. Pin Diagram

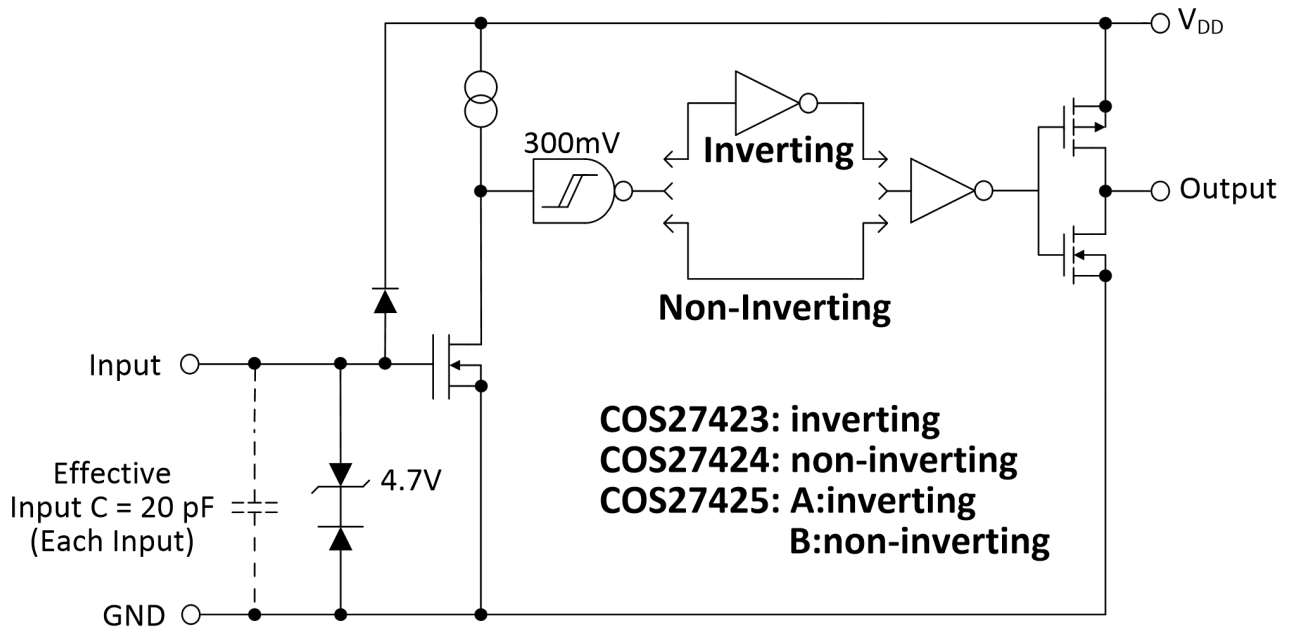


Figure 2. Functional Block Diagram

### Pin Description

Pin	Name	Description
1	ENA	Enable driver A
2	IN A	Input A
3	GND	Ground
4	In B	Input B
5	OUT B	Output of Channel B
6	VDD	Power Supply
7	OUT A	Output of Channel A
8	ENB	Enable driver B
-	PAD	Exposed Metal Pad for DFN Packaging

### Function Table

ENABLE		INPUTS		COS27423		COS27424		COS27425	
ENA	ENB	INA	INB	$\overline{\text{OUTA}}$	$\overline{\text{OUTB}}$	OUTA	OUTB	$\overline{\text{OUTA}}$	OUTB
H	H	L	L	H	H	L	L	H	L
H	H	L	H	H	L	L	H	H	H
H	H	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	L	H
L	L	X	X	L	L	L	L	L	L

## 1.1 Inputs A and B

MOSFET driver inputs A and B are high-impedance, TTL/CMOS compatible inputs. These inputs also have 300mV of hysteresis between the high and low thresholds that prevents output glitching even when the rise and fall time of the input signal is very slow. If not used, both inputs should be tied to either  $V_{DD}$  or GND. They should not be left floating.

## 1.2 Ground (GND)

Ground is the device return pin. The Ground pin(s) should have a low-impedance connection to the bias supply source return. High peak current flows out the Ground pin(s) when the capacitive load is being discharged.

## 1.3 Output A and B

MOSFET driver outputs A and B are low-impedance, CMOS push-pull style outputs. The pull-down and pullup devices are of equal strength, making the rise and fall times equivalent. The output A/B state when the device is disabled will be LOW regardless of the input state.

## 1.4 Supply Input (VDD)

The VDD input is the bias supply for the MOSFET driver and is rated for 4.5V to 25V with respect to the Ground pin. The VDD input should be bypassed with local ceramic capacitors. The value of these capacitors should be chosen based on the capacitive load that is being driven. A value of 1.0  $\mu$ F is suggested.

## 1.5 Exposed Metal Pad

The exposed metal pad of the DFN-S package is not internally connected to any potential. Therefore, this pad can be connected to a ground plane or other copper plane on a Printed Circuit Board (PCB), to aid in heat removal from the package.

## 1.6 Enable A and B

Enable input for the driver A/B with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to  $V_{DD}$  with 100 k $\Omega$  resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.

## 2. Product Specification

### 2.1 Absolute Maximum Ratings <sup>(1)</sup>

Parameter	Min	Max	Unit
DC supply voltage $V_s$		26	V
Operating junction temperature	-40	+125	$^{\circ}$ C
Storage temperature	-55	+150	$^{\circ}$ C
Maximum input voltage	GND-5	VDD+0.3	V

(1) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

### 2.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance	155(SOP8) 125(DIP8) 118(FDN8,2x2)	$^{\circ}$ C/W

## 2.3 Recommended Operating Conditions

Parameter	Rating	Unit
DC Supply Voltage	4.5V ~ 25V	V
Operating ambient temperature	-40 to +125	°C

## 2.4 Electrical Characteristics

(Typical values are tested at  $T_A=25\text{ }^\circ\text{C}$ ,  $V_{DD}=18\text{V}$ )

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>INPUT</b>						
Input Signal High Threshold	$V_{IH}$		1.8			V
Input Signal Low Threshold	$V_{IL}$				0.7	V
Input Signal Hysteresis	$V_{HYS}$			0.3		V
Input Current	$I_{IN}$	$0\text{V} \leq V_{IN} \leq V_{DD}$			$\pm 1$	$\mu\text{A}$
<b>OUTPUT</b>						
High Output Voltage $V_{OH}$	$V_{OH}$	DC Test	$V_{DD} - 0.025$			V
Low Output Voltage	$V_{OL}$	DC Test			0.025	V
Pull-Up Resistance	$R_{OH}$	Source Current = 10mA		1.6		$\Omega$
Pull-Down Resistance	$R_{OL}$	Sink Current = -10mA		1.5		$\Omega$
Peak Output Current	$I_{PK}$	$10\text{V} \leq V_{DD} \leq 24\text{V}$		4.5		A
<b>ENABLE</b>						
High-level Input Voltage	$V_{IHEN}$		1.7	2.4	2.9	V
Low-level Input Voltage	$V_{ILEN}$		1.1	1.8	2.2	V
Hysteresis	$V_{HYSEN}$		0.15	0.3	0.9	V
Enable Impedance	$R_{EN}$		90	100	110	k $\Omega$

<b>POWER SUPPLY</b>						
Power Supply Current	$I_{CC}$	$V_{INA}=V_{INB}=3V$		0.9		mA
		$V_{INA}=V_{INB}=0V$		0.5		
Operating Voltage Range	$V_{DD}$		4.5		25	V
Under-Voltage Lockout ON Threshold				3.7	4.1	V
Under-Voltage Lockout Hysteresis				0.5		V
<b>SWITCHING CHARACTERISTICS</b>						
Rise Time	$t_R$	$C_L = 1800pF$ , See Figure 3		12		ns
Fall Time	$t_F$	$C_L = 1800pF$ , See Figure 3		12		ns
Turn-On Delay Time	$t_{D1}$	Non-inverting Input		36		ns
		Inverting Input		35		ns
Turn-On Delay Time	$t_{D2}$	Non-inverting Input		36		ns
		Inverting Input		35		ns
<b>OVER-TEMPERATURE PROTECTION</b>						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Threshold Hysteresis				25		°C

### 3. Application Information

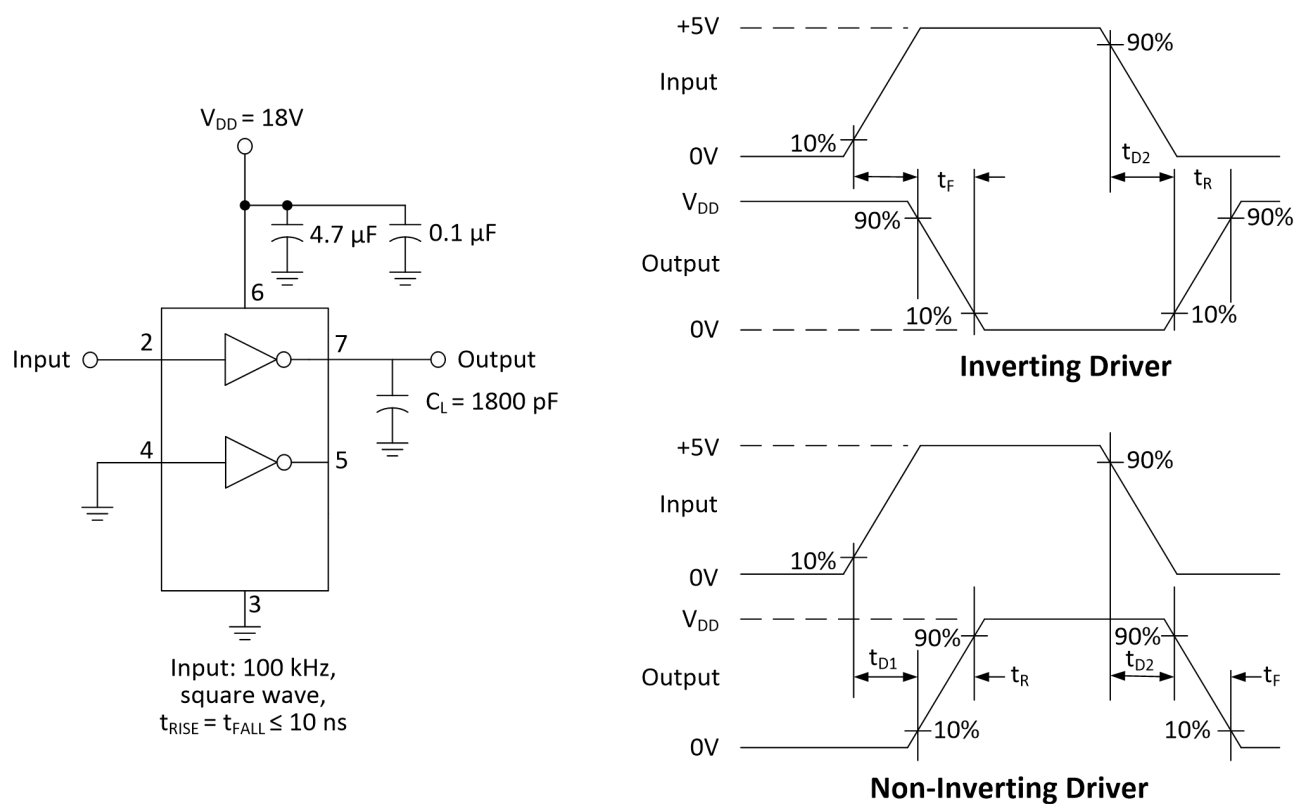


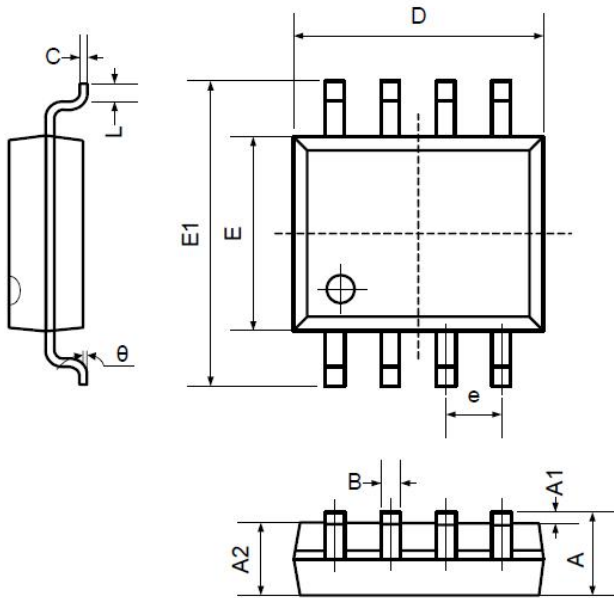
Figure 3. Switching Time Test Circuit

### 4. Package and Ordering Information

Model	Order Number	Package	Package Option	Marking Information
COS27423	COS27423SR	SOP-8	Tape and Reel, 4000	COS27423SR
	COS27423FR	DFN-8	Tape and Reel, 4000	COS27423FR
	COS27423DR	DIP-8	Tube 50	COS27423DR
COS27424	COS27424SR	SOP-8	Tape and Reel, 4000	COS27424SR
	COS27424FR	DFN-8	Tape and Reel, 4000	COS27424FR
	COS27424DR	DIP-8	Tube 50	COS27424DR
COS27425	COS27425SR	SOP-8	Tape and Reel, 4000	COS27425SR
	COS27425FR	DFN-8	Tape and Reel, 3000	COS27425FR
	COS27425DR	DIP-8	Tube 50	COS27425DR

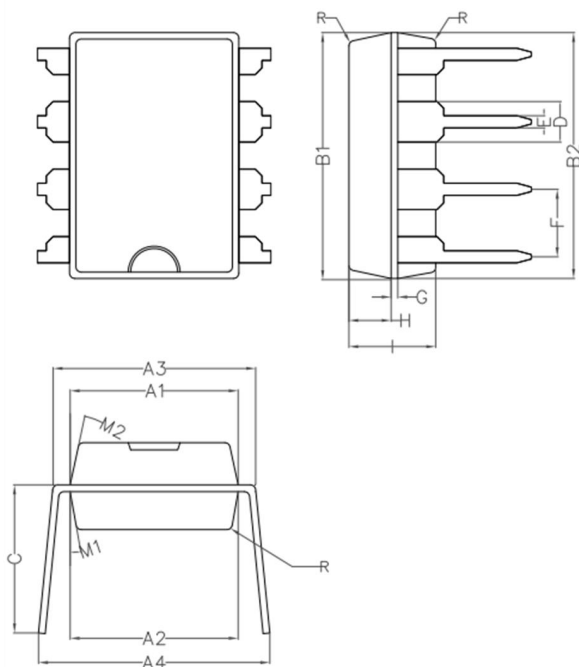
## 5. Package Information

### 5.1 SOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

### 5.2 DIP8 (Package Outline Dimensions)



Symbol	Min	Non	Max
A1	6.28	6.33	6.38
A2	6.33	6.38	6.43
A3	7.52	7.62	7.72
A4	7.80	8.40	9.00
B1	9.15	9.20	9.25
B2	9.20	9.25	9.30
C		5.57	
D		1.52	
E	0.43	0.45	0.47
F		2.54	
G		0.25	
H	1.54	1.59	1.64
I	3.22	3.27	3.32
R		0.20	
M1	9°	10°	11°
M2	11°	12°	13°