

General Description

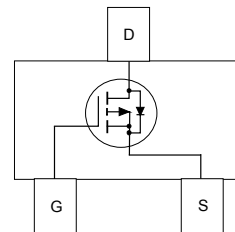
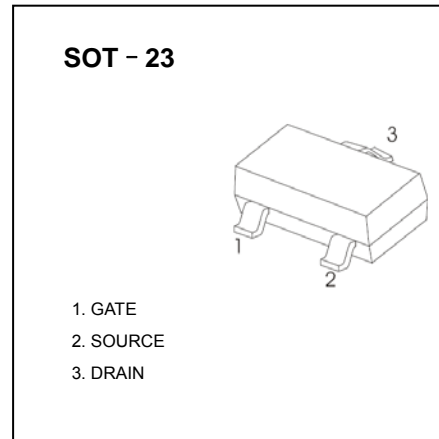
This P-Channel 1.8V specified MOSFET uses Fairchild's advanced low voltage PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load switch
- Battery protection

Features

- -2.6 A, -12 V. $R_{DS(ON)} = 40\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
 $R_{DS(ON)} = 50\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
 $R_{DS(ON)} = 80\text{ m}\Omega @ V_{GS} = -1.8\text{ V}$
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- SuperSOT™ -3 provides low $R_{DS(ON)}$ and 30% higher power handling capability than SOT23 in the same footprint



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	-12	V
V _{GSS}	Gate-Source Voltage	±8	V
I _D	Drain Current – Continuous (Note 1a) – Pulsed	-2.6	A
		-10	
P _D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
Thermal Characteristics			
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = –250 μA	–12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C		–3		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = –10 V, V _{GS} = 0 V			–1	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 8 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –8 V, V _{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = –250 μA	–0.4	–0.6	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C		2.5		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = –4.5 V, I _D = –2.6 A V _{GS} = –2.5 V, I _D = –2.3 A V _{GS} = –1.8 V, I _D = –1.8 A		30 39 54	40 50 80	mΩ
I _{D(on)}	On–State Drain Current	V _{GS} = –4.5 V, V _{DS} = –5 V	–10			A
g _{FS}	Forward Transconductance	V _{DS} = –5 V, I _D = –2.6 A		10		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = –6 V, V _{GS} = 0 V,		1138		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		454		pF
C _{rss}	Reverse Transfer Capacitance			302		pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = –6 V, I _D = –1 A,		11	20	ns
t _r	Turn–On Rise Time	V _{GS} = –4.5 V, R _{GEN} = 6 Ω		10	20	ns
t _{d(off)}	Turn–Off Delay Time			38	61	ns
t _f	Turn–Off Fall Time			35	56	ns
Q _g	Total Gate Charge	V _{DS} = –6 V, I _D = –2.6 A,		12	17	nC
Q _{gs}	Gate–Source Charge	V _{GS} = –4.5 V		2		nC
Q _{gd}	Gate–Drain Charge			3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain–Source Diode Forward Current				–0.42	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –0.42 (Note 2)		–0.6	–1.2	V

Notes:

- R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

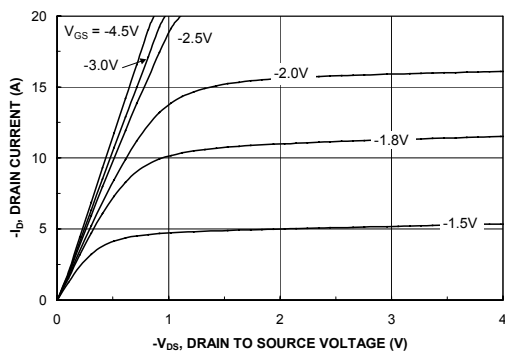


Figure 1. On-Region Characteristics.

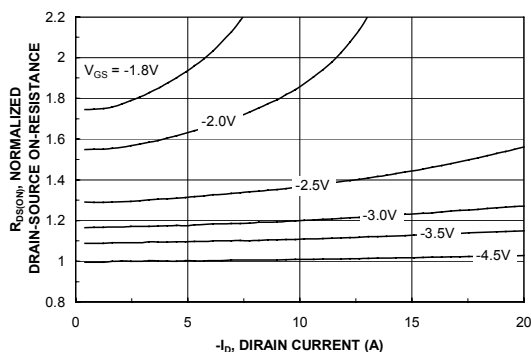


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

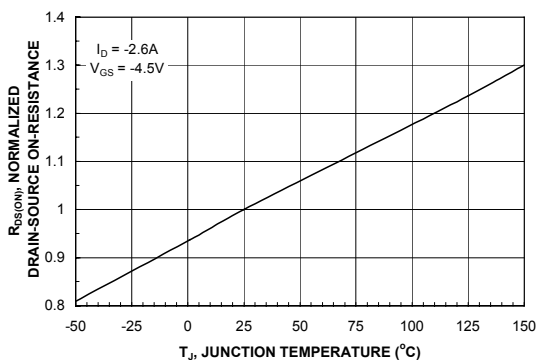


Figure 3. On-Resistance Variation with Temperature.

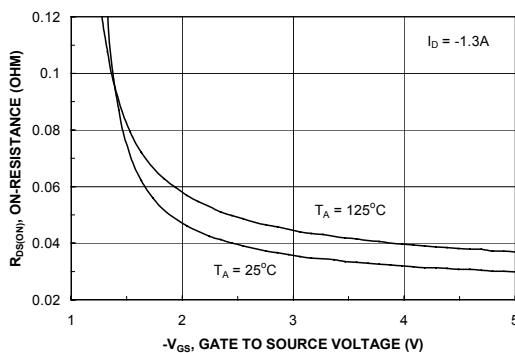


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

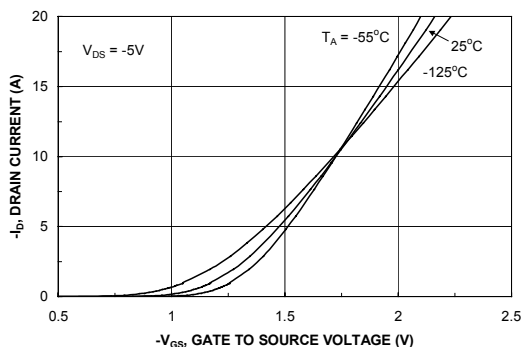


Figure 5. Transfer Characteristics.

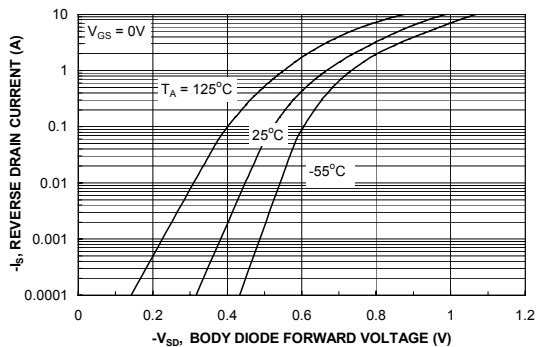


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

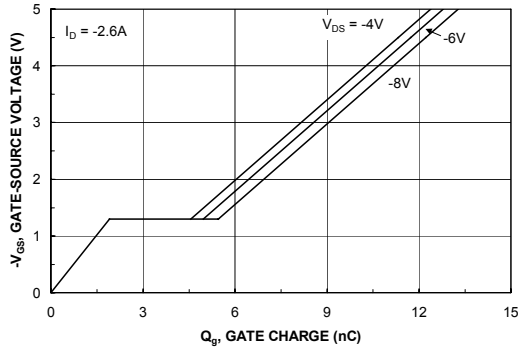


Figure 7. Gate Charge Characteristics.

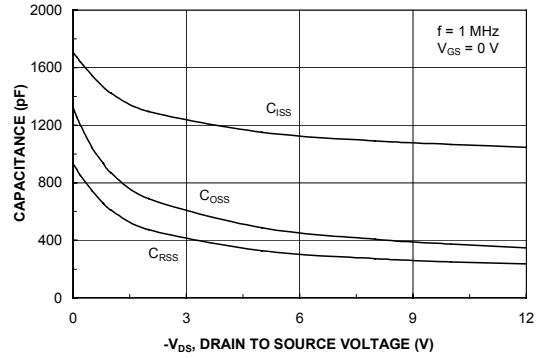


Figure 8. Capacitance Characteristics.

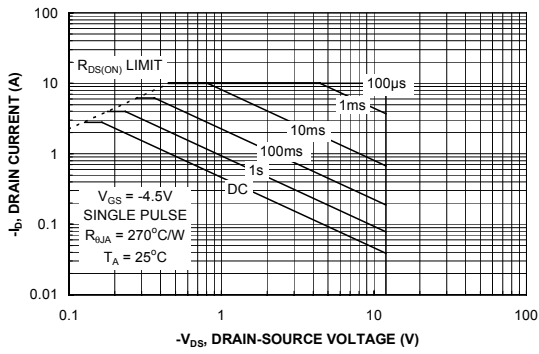


Figure 9. Maximum Safe Operating Area.

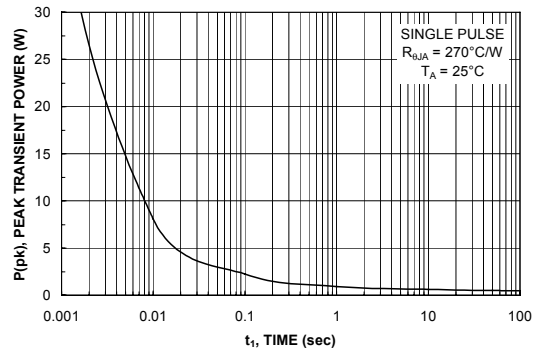


Figure 10. Single Pulse Maximum Power Dissipation.

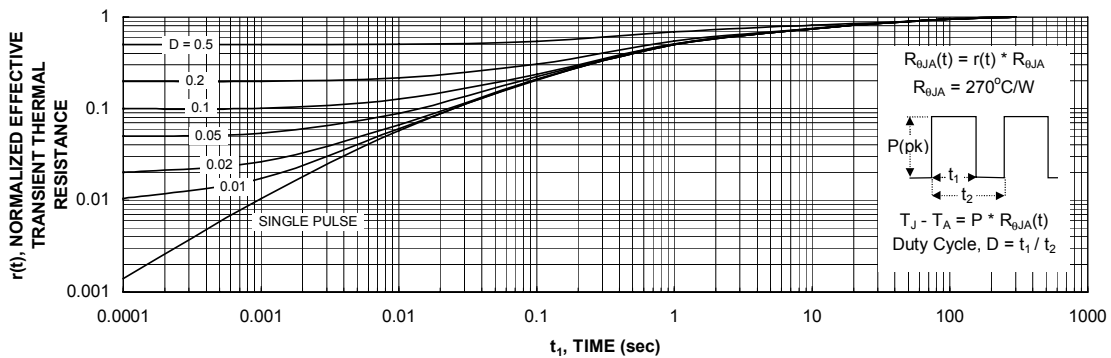
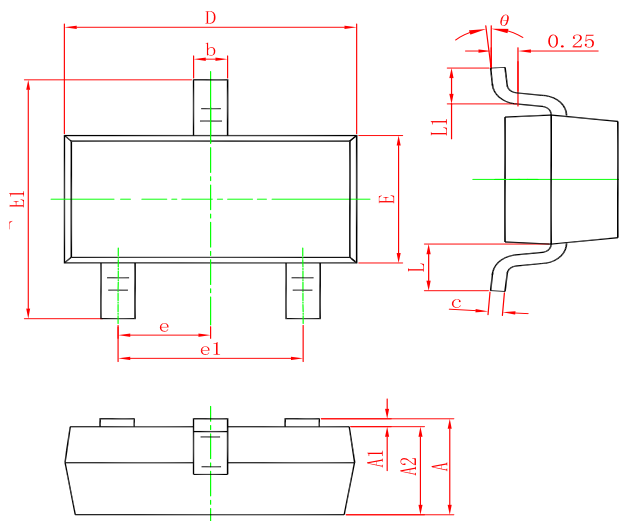


Figure 11. Transient Thermal Response Curve.

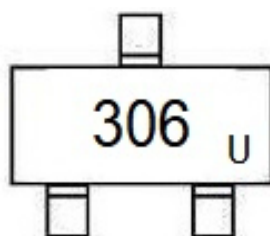
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

SOT-23 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDN306P	SOT-23	3000	Tape and reel