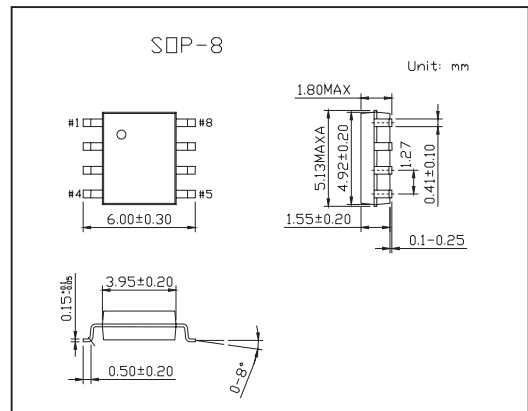


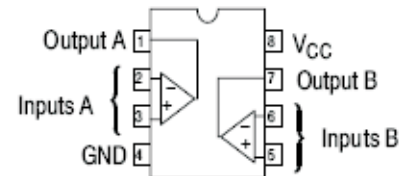
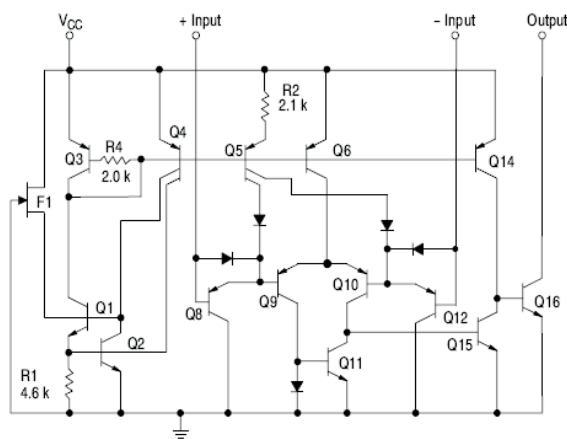
# Low Power Low Offset Voltage Dual Comparators

## ■ Features

- Wide Single-Supply Range: 2.0 V to 32 V
- Split-Supply Range:  $\pm 1.0$  V to  $\pm 16$  V
- Very Low Current Drain Independent of Supply Voltage: 0.4 mA
- Low Input Bias Current: 25 nA
- Low Input Offset Current: 5.0 nA
- Low Input Offset Voltage: 5.0 mV (max)
- Input Common Mode Range to Ground Level
- Differential Input Voltage Range Equal to Power Supply Voltage



## ■ Representative Schematic Diagram



## ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V <sub>CC</sub>	+32 or $\pm 16$	V
Input Differential Voltage Range	V <sub>IDR</sub>	32	V
Input Common Mode Voltage Range	V <sub>ICR</sub>	-0.3 to +32	V
Output Short Circuit-to-Ground	I <sub>SC</sub>	Continuous	mA
Output Sink Current*	I <sub>SINK</sub>	20	
Power Dissipation @ $T_A = 25^\circ\text{C}$	P <sub>D</sub>	570	mW
Derate above $25^\circ\text{C}$	1/R $\theta$ JA	5.7	mW/°C
Operating Ambient Temperature Range	T <sub>A</sub>	-40 to 105	°C
Maximum Operating Junction Temperature	T <sub>J(max)</sub>	150	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
ESD Protection at any Pin	V <sub>esd</sub>	2000	V
- Human Body Model			
- Machine Model			

\* The maximum output current may be as high as 20 mA, independent of the magnitude of V<sub>CC</sub>, output short circuits to V<sub>CC</sub> can cause excessive heating and eventual destruction.

**■ Electrical Characteristics ( $V_{CC} = 5.0\text{ V}$ ,  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ , unless otherwise noted.)**

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Input Offset Voltage*1	$V_{IO}$	$T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		$\pm 1.0$	$\pm 5.0$ 9.0	mV
Input Offset Current	$I_{IO}$	$T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		$\pm 5.0$	$\pm 50$ $\pm 150$	nA
Input Bias Current *2	$I_{IB}$	$T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		25	250 400	nA
Input Common Mode Voltage Range *2	$V_{ICR}$	$T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$	0 0		$V_{CC} - 1.5$ $V_{CC} - 2.0$	V
Voltage Gain	$AV_{OL}$	$R_L \geq 15\text{ k}\Omega$ , $V_{CC} = 15\text{ V}$ , $T_A = 25^{\circ}\text{C}$	50	200		V/mV
Large Signal Response Time		$V_{in} = \text{TTL Logic Swing}$ , $V_{ref} = 1.4\text{ V}$ , $V_{RL} = 5.0\text{ V}$ , $R_L = 5.1\text{ k}\Omega$ , $T_A = 25^{\circ}\text{C}$		300		ns
Response Time *4	tTLH	$V_{RL} = 5.0\text{ V}$ , $R_L = 5.1\text{ k}\Omega$ , $T_A = 25^{\circ}\text{C}$		1.3		$\mu\text{ s}$
Input Differential Voltage *5	$V_{ID}$	All $V_{in} \geq GND$ or V-Supply (if used)			$V_{CC}$	V
Output Sink Current	$I_{SINK}$	$V_{in} \geq 1.0\text{ V}$ , $V_{in+} = 0\text{ V}$ , $V_O \leq 1.5\text{ V}$ , $T_A = 25^{\circ}\text{C}$	6.0	16		mA
Output Saturation Voltage	$V_{OL}$	$V_{in} \geq 1.0\text{ V}$ , $V_{in+} = 0$ , $I_{SINK} \leq 4.0\text{ mA}$ , $T_A = 25^{\circ}\text{C}$ $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		150	400 700	mV
Output Leakage Current	$I_{OL}$	$V_{in-} = 0\text{ V}$ , $V_{in+} \geq 1.0\text{ V}$ , $V_O = 5.0\text{ V}$ , $T_A = 25^{\circ}\text{C}$ $V_{in-} = 0\text{ V}$ , $V_{in+} \geq 1.0\text{ V}$ , $V_O = 30\text{ V}$ , $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$		0.1	1000	nA
Supply Current	$I_{CC}$	$R_L = \infty$ Both Comparators, $T_A = 25^{\circ}\text{C}$ $R_L = \infty$ Both Comparators, $V_{CC} = 30\text{ V}$		0.4	1.0 2.5	mA

\*1. At output switch point,  $V_O = 1.4\text{ V}$ ,  $R_S = 0\Omega$  with  $V_{CC}$  from  $5.0\text{ V}$  to  $30\text{ V}$ , and over the full input common mode range ( $0\text{ V}$  to  $V_{CC} - 1.5\text{ V}$ ).

\*2. Due to the PNP transistor inputs, bias current will flow out of the inputs. This current is essentially constant, independent of the output state, therefore, no loading changes will exist on the input lines.

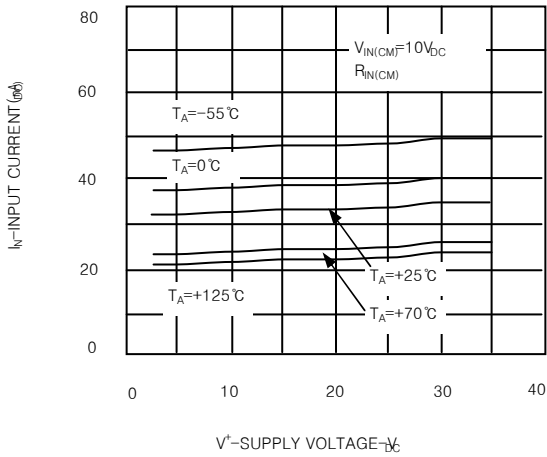
\*3. Input common mode of either input should not be permitted to go more than  $0.3\text{ V}$  negative of ground or minus supply. The upper limit of common mode range is  $V_{CC} - 1.5\text{ V}$ .

\*4. Response time is specified with a  $100\text{ mV}$  step and  $5.0\text{ mV}$  of overdrive. With larger magnitudes of overdrive faster response times are obtainable.

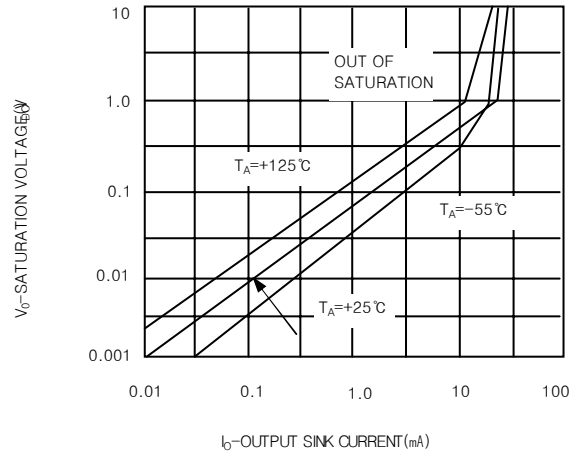
\*5. The comparator will exhibit proper output state if one of the inputs becomes greater than  $V_{CC}$ , the other input must remain within the common mode range. The low input state must not be less than  $-0.3\text{ V}$  of ground or minus supply.

TYPICAL PERFORMANCE CHARACTERISTICS

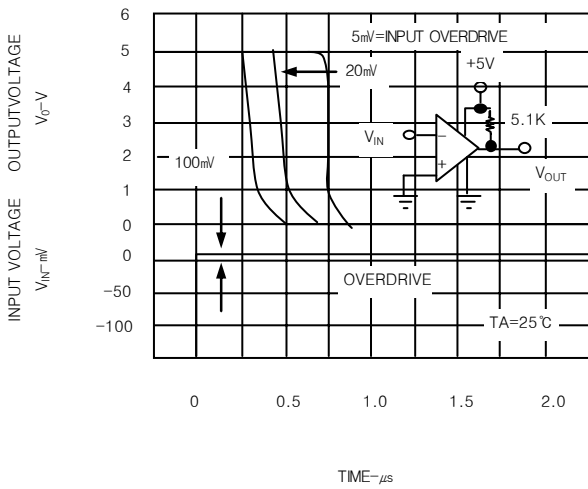
INPUT CURRENT



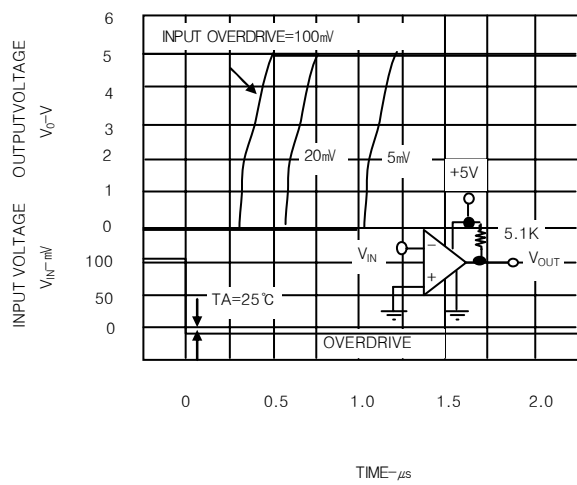
OUTPUT SATURATION VOLTAGE



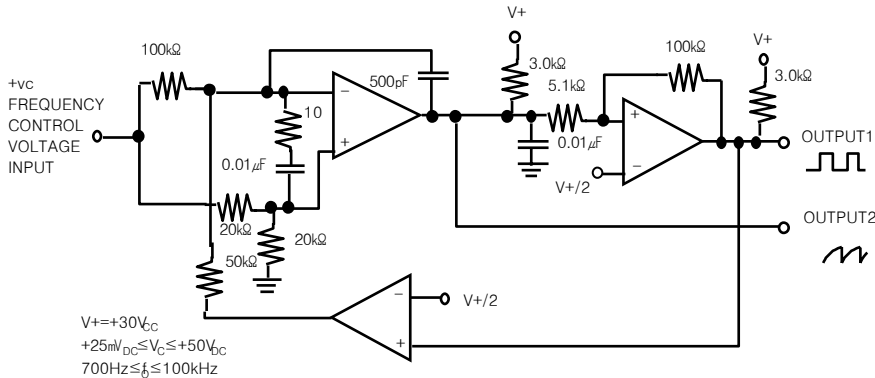
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES-NEGATIVE TRANSITION



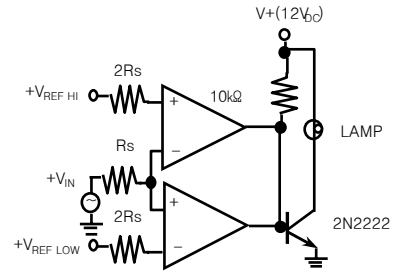
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES-POSITIVE TRANSITION



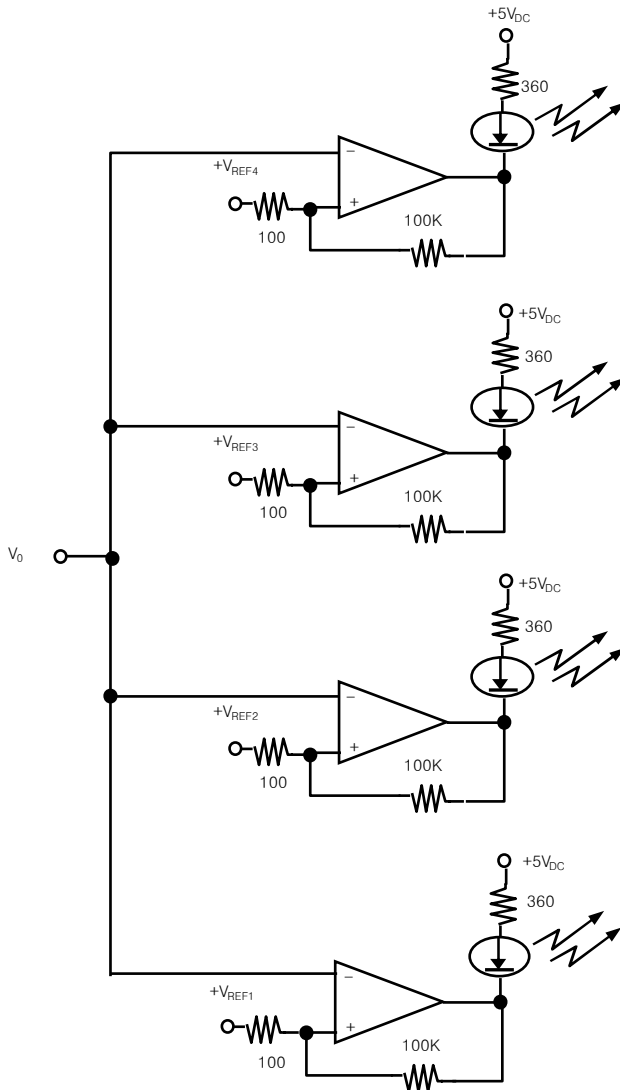
TYPICAL APPLICATIONS



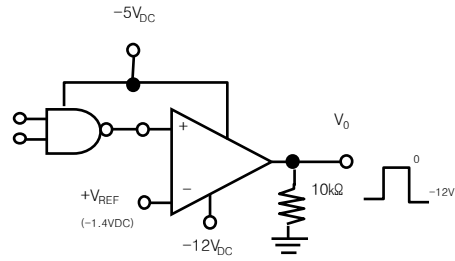
TWO-DECADE HIGH-FREQUENCY VCO



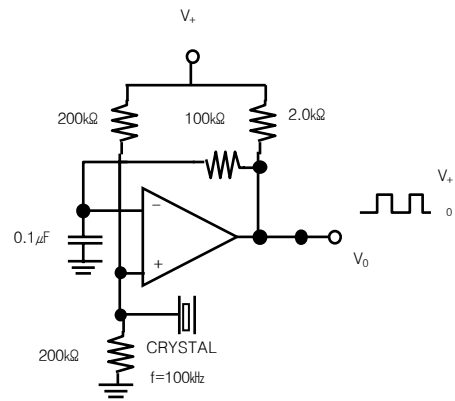
LIMIT COMPARATOR



VISIBLE VOLTAGE INDICATOR



TTL-TO-MOS LOGIC CONVERTER



CRYSTAL-CONTROLLED OSCILLATOR