PAC5285

40V/20W BLDC Motor Controller and Driver with Integrated FETs

Product Overview

The Qorvo® PAC5285 is a 40V/20W BLDC Integrated Motor Controller and Driver with integrated FETs. To enable compact low-power BLDC motor applications, this device integrates a FLASH-programmable MCU, Power Management, Signal Conditioning and 3-Phase BLDC Inverter into a single product.

The PAC5285 contains an Arm® Cortex®-M0 with 32kB of FLASH and 8KB of SRAM and has access to several different analog and digital peripherals used for BLDC motor control and driving.

This device has a single 40V power supply input, which makes it ideal for 12V battery-powered applications. There is a charge pump DC/DC that converts the power supply input into an IC and inverter power supply. There are regulators for a 5V system supply, core and analog supplies as well.

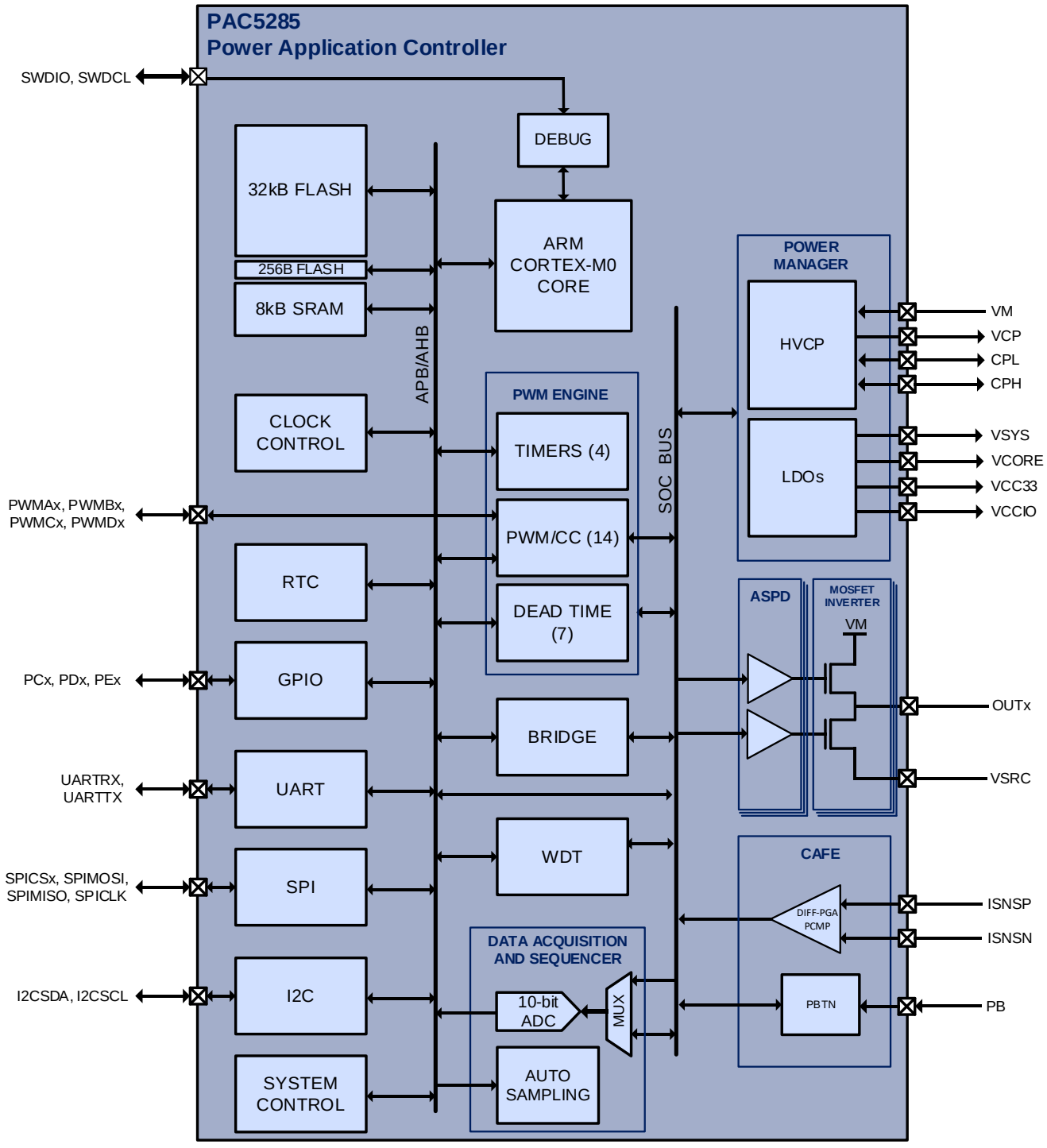
The device also integrates a differential amplifier that may be used for sensing motor current for over-current protection and motor control. The inverter may be shut down during over-current, over-voltage, under-voltage and over-temperature events. There is also a power monitor that allows the ADC to sample all power supply rails internally.

This device contains 6 40V/300mΩ MOSFETs to support 3-phase BLDC motor applications.

The PAC5285 is packaged in a 6x6mm, 40-lead QFN package for compact low-power BLDC motors.

Functional Block Diagram

Figure 1 Architectural Block Diagram



PAC5285

40V/20W BLDC Motor Controller and Driver with Integrated FETs

Key Features

MCU

- 50MHz Arm® Cortex®-M0
  - 32kB FLASH
  - 8kB SRAM
  - 256B INFO FLASH for manufacturing information
  - 20 interrupts, 4 priority levels
- SWD programming interface
- Clock-gating for low-power operation

ADC

- 10-bit 1MSPS SAR ADC
- Dual 8-channel ADC sequencer

Timing Generators

- Four 16-bit PWM timers with up to 8 CCR output units each
- 24-bit SysTick count-down timer
- Watch-dog Timer (WDT)
- Real-time Clock (RTC)
- Two 24-bit General Purpose Timers

IO

- 3.3V/5V configurable drive output
- 12 general-purpose IO
- Digital Input, digital output, analog ADC input
- Configurable weak pull-up or pull-down
- Configurable drive-strength (8mA or 16mA)
- Flexible interrupt controller

Communication Peripherals

- UART/SPI or I2C
- 8-bit UART, up to 1Mbps
- 3-wire or 4-wire SPI, master/slave
- I2C master/slave, 7b/10b
- Single-wire debugger (SWD)

Power Manager

- Up to 40V supply input
- Charge Pump DC/DC
- 5V system supply
- Integrated LDOs for MCU core, analog
- Power and temperature monitor, warning and fault detection
- Low-Power Operation
  - 8μA total hibernate mode

Configurable Analog Front-End (CAFE™)

- Differential amplifier for motor current sense
- 2.5V ADC reference
- OC shutdown and programmable OC warning
- Hibernate push-button wake-up
- Power supply monitoring via ADC
- Integrated VM and VCP sensing without additional external components

Application Specific Power Drivers (ASPD™)

- “Break-before-make” hardware dead-time enforcement to prevent shoot-through
- Integrated level shifters and pre-drivers
- 6 integrated 40V/300mΩ Power MOSFETs for 3-phase BLDC motor applications
- OC, UV protection

Packaging

- QFN 6x6mm 40-pin package
- Exposed pad for thermal management

Certifications

- T_A = -40°C to 105°C

Ordering Information

Orderable Part Number	Description	
PAC5285QJ-T	40V/20W BLDC Controller/Driver with Integrated FETs	3000-piece reel

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Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Power Manager			
VM to VSS	Supply Input Voltage	-0.3 to 40	V
VCP to VM	Charge Pump Voltage	-0.3 to 6	V
CPH to VM		-0.3 to VCP + 0.3	V
CPL to VSS		-0.3 to VSYS	V
VSYS to VSS	System Regulator Voltage	-0.3 to 6	V
VCC33 to VSS	Analog, IO Supply Voltage	-0.3 to 4.1	V
VCORE to VSS	Core Supply Voltage	-0.3 to 2.5	V
Signal Manager			
ISNSP, ISNSN, VSRC to VSS	Current Sense Voltage	-0.3 to VSYS + 0.3	V
PB to VSS	Push-button Wakeup Input	-0.3 to 6	V
Driver Manager			
OUTU, OUTV, OUTW to VSS	Motor Phase Voltage	-1 to 44	V
IO			
PAx, PDx, PEx to VSS	MCU IO Pin Voltage	-0.3 to VCCIO + 0.3	V
PCx to VSS	MCU IO/Analog Input Pin Voltage	-0.3 to VCC33 + 0.3	V
I_{Pxy} pin injection current		7.5	mA
$\sum I_{Pxy}$ sum of all pin injection current		25	mA
Temperature			
T_A	Ambient Temperature	-40 to 105	°C
T_{STG}	Storage Temperature	-40 to 140	°C
Electro-static Discharge (ESD)			
Human Body Model (HBM)		2	kV
Charge Device Model (CDM)	All pins	1	kV

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VM	Supply Input Voltage	5.5	12	27	V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

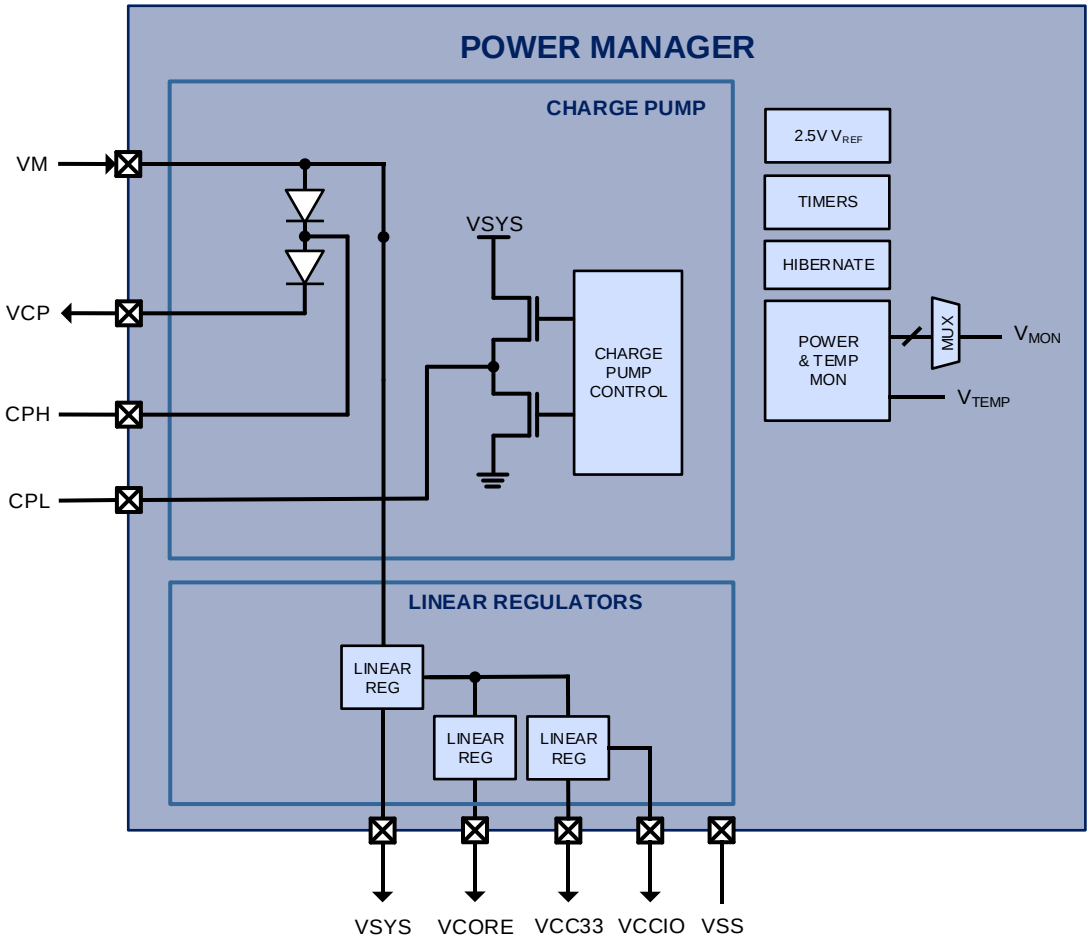
Power Manager

Features

- Charge Pump DC/DC for gate driver and inverter supply (HVCP)
- VSYS LDO for 5V system supply
- VCC33 LDO for 3.3V analog and IO supply
- VCORE LDO for 1.8V core supply
- High-accuracy 2.5V voltage reference for ADC (VREF)
- Power and temperature monitoring, warning and fault detection
- Extremely low hibernate mode I_Q of 8µA

Block Diagram

Figure 2 Power Manager Block Diagram



Functional Description

The Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC5285 and associated application circuitry. It incorporates a High-Voltage Charge Pump DC/DC (HVCP) to generate for the integrated high-side gate drivers and MOSFET inverter.

The VSYS LDO generates a 5V system supply that is used to power the IC and the other LDOs. VSYS is used to supply the low-side gate drivers, VCC33 and VCORE, which are used to generate a 3.3V analog and IO supply and 1.8V digital core supply.

The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

High-Voltage Charge Pump (HVCP)

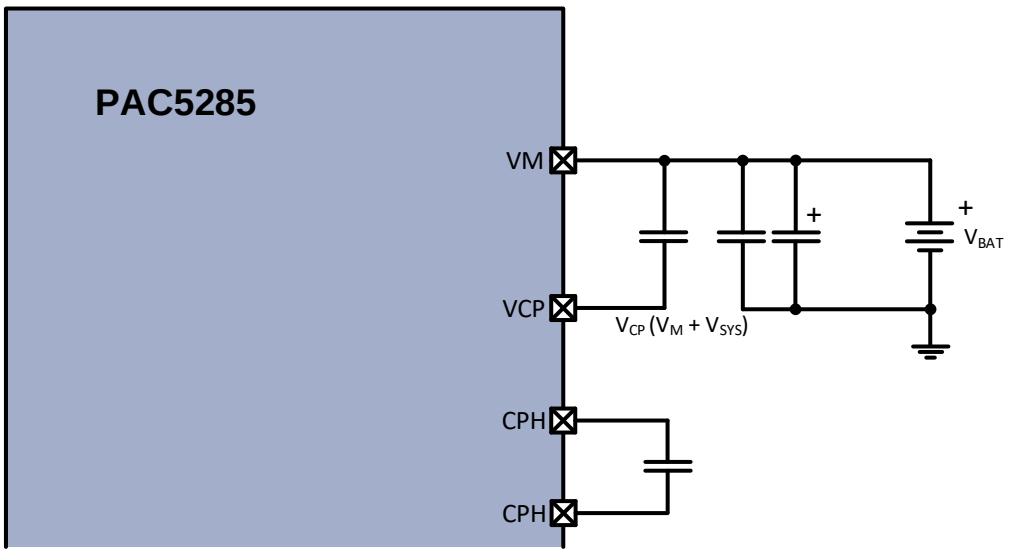
The HVCP is a charge pump that is used to generate VCP, which is the high-side gate driver supply voltage. The charge pump maintains a voltage of VM + VSYS.

The positive terminal of the battery supply is connected to the VM pins on the PAC5285. This supply should be bypassed to ground using a high-value electrolytic capacitor in a parallel with a 0.1µF ceramic capacitor from VM to VSS. These pins require good capacitive bypass to VSS, so the ceramic capacitor should have a trace shorter than 10mm to the pin.

The charge pump requires a capacitor between the VM and VCP pins, to act as a storage capacitor for the gate driver supply. The nominal value of this capacitor should be 6.3V/2.2µF. A flying capacitor should be placed between the CPH and CPL pins with a nominal value of 0.1µF rated for double the VM voltage.

Figure 3 below shows the typical circuit connections for the HVCP on the PAC5285.

Figure 3 HVCP Circuit Connections



Integrated VM Sensing

The Power Manager also integrates the sensing of the battery voltage on VM, without the need for external components. This allows the user to sense VM for the application, without adding resistor dividers and consuming an analog input for the ADC.

Linear Regulators

The PAC5285 includes three linear regulators:

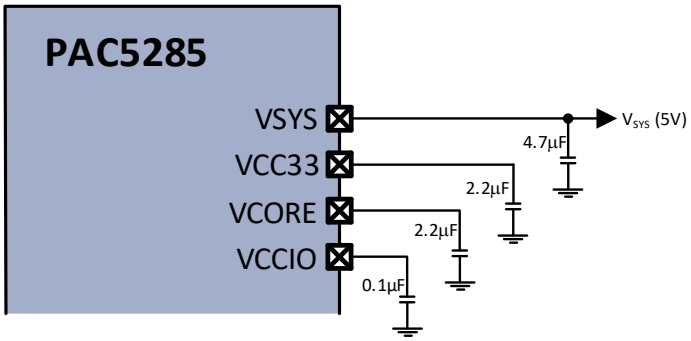
- VSYS
- VCC33
- VCORE

The VSYS regulator generates a 5V supply that is used to supply the internal logic and is the supply for the VCC33 and VCORE LDOs. Once VSYS is above 4.5V, the additional linear regulators VCC33 and VCORE power up. VSYS has up to 20mA of external load available for PCB peripherals.

The VCC33 regulator generates a dedicated 3.3V analog supply for the ADC and GPIO on the MCU. The VCORE regulator generates a dedicated 1.9V digital logic supply for the MCU. Once all LDOs are above their respective power good thresholds, then the MCU is released from reset and begins executing instructions.

Each of the LDOs must be bypassed externally to ground as shown below. See the electrical characteristics below for details on the recommended component values for each of the bypass capacitors.

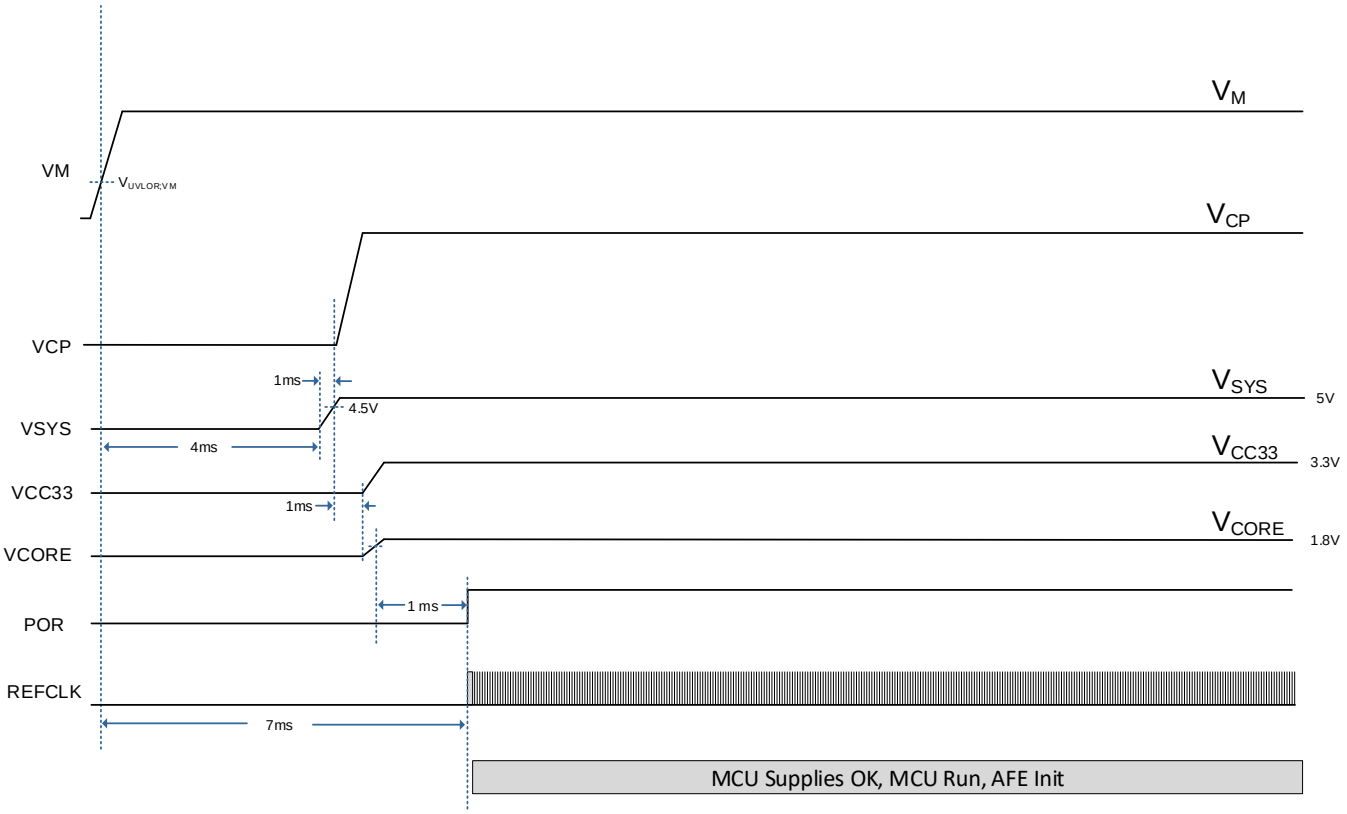
Figure 4 Linear Regulators Connections



Power-up Sequence

The Power Manager follows a typical power-up sequence as shown in Figure 5 below.

Figure 5 Power-up Sequence



A typical sequence begins with input power supply being applied on VM. During this time, VCP will be about one diode drop lower than VM. After VM has reached a safe threshold, after 4ms the VSYS LDO starts to rise. After VSYS gets to its power good threshold, the VCP charge pump output is turned on and VCP will start to rise toward its final value of VM + VSYS.

After VSYS rises above its UVLO threshold and 1ms has elapsed, the VCC33 and VCORE LDOs are started. After VCORE and VCC33 has reached its power good threshold, there is a 1ms delay and then the POR signal will be released from reset to the MCU.

Low-Power Modes

The PAC5285 provides several low-power modes to assist with various tradeoffs between low-power functionality and energy savings. The low-power modes are as follows:

- Sleep/Deep Sleep Mode
- Hibernate Mode

In *Sleep Mode* the MCU stops executing instructions, but all other digital and analog functions remain active. This mode provides a modest amount of power savings, and the MCU may very quickly awake from this mode to being executing instructions.

In *Deep Sleep Mode*, the MCU also stops executing instructions and some digital peripherals on the MCU are also gated and put to sleep, depending on the needs of the application. Some analog functions remain active in this mode.

In *Hibernate Mode* the PAC5285 goes into an ultra-low-power mode and MCU is not powered. Before entering hibernate mode, the MCU may set a timer to wake itself up from hibernate mode or may rely on an external “push-button” event on PB to wake up from hibernate mode.

In this mode, only a minimal amount of current is used by VM, and the Power Manager and all internal regulators are shut down to eliminate power drain from the output supplies.

The system exits hibernate mode after the wake-up timer expires (duration from 25ms to 4s, or infinite) or when a push-button event is received on PB. These would have to be configured before entering hibernate mode. When exiting hibernate mode, the Power Manager goes through the start-up cycle and the MCU is re-initialized. Only the persistent power manager status bits (resets and faults) are retained during hibernation.

Power and Temperature Monitor

Whenever any of the VSYS, VCC33, or VCORE power supplies falls below their respective power good threshold voltage, a fault event is detected and the MCU is reset. The MCU stays in the reset state until VSYS, VCC33, and VCORE supply rails are all good again and the reset time has expired. An MCU reset can also be initiated by a maskable temperature fault event that occurs when the junction temperature reaches 165°C. The fault status bits are persistent during reset and can be read by the MCU upon re-initialization to determine the cause of previous reset.

Power monitoring signals are provided onto the ADC pre-multiplexer for monitoring various internal power supplies. The ADC pre-multiplexer can select from power monitoring signals: VCORE, 0.2•(VCP-VM), 0.4•VCC33, 0.4•VSYS, 0.05•VM or VPTAT.

For power and temperature warning, an IC temperature warning event at a junction temperature of 140°C is provided as a maskable interrupt to the MCU. This warning allows the MCU to safely power down the system.

This value has a compensation coefficient available in INFO FLASH that can be used to obtain an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The die temperature in degrees Kelvin can then be calculated by the following formula:

T_{KELVIN} = 300 * (VPTAT + 0.075) / (VT300K + 0.075)

VPTAT can be read by the ADC by setting the ADC MUX using the voltage monitoring signals above.

For more information on the location of this temperature coefficient, see the PAC5285 Device User Guide.

Voltage Reference

The reference block includes a 2.5V high precision reference voltage that provides the 2.5V reference voltage for the ADC.

Electrical Characteristics

The Electrical Characteristics for the Power Manager are shown below.

HVCP Electrical Characteristics

Table 1 HVCP Manager Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Input Supply (VM)						
$I_{HIB;VM}$	VM hibernate mode supply current	Hibernate mode active, VM = 12V		8		µA
$V_{OP;VM}$	VM operating voltage range		5.5		27	V
$V_{UVLOR;VM}$	VM under-voltage lockout rising		5.2	5.4		V
$V_{UVLOF;VM}$	VM under-voltage lockout hysteresis			0.3		V
$V_{OVLOR;VM}$	VM over-voltage lockout rising		37			V
$V_{OVLOF;VM}$	VM over-voltage lockout hysteresis			3.5		V
Charge Pump Output (VCP)						
$V_{OP;VCP}$	VCP operating voltage range			VM + VSYS		V
C_{VCP}	VCP capacitor value			1		µF
$V_{UVLOR;VCP}$	Charge Pump UVLO rising	VCP - VM		4		V
$V_{UVLOF;VCP}$	Charge Pump UVLO hysteresis	VCP - VM		0.5		V

VM = 12V and T_A = -40°C to 105°C unless otherwise specified

Linear Regulators Electrical Characteristics

Table 2 Linear Regulators Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{SYS}	VSYS output voltage	External load = up to 20mA		5.0		V
V_{CC33}	VCC33 output voltage	No external load allowed		3.3		V
V_{CORE}	VCORE output voltage	No external load allowed		1.9		V
$V_{UVLOR;VSYS}$	VSYS under-voltage lockout rising		4.35	4.5	4.65	V
$V_{UVLOF;VSYS}$	VSYS under-voltage lockout hysteresis			0.3		V
$k_{POK;VCC33}$	VCC33 power OK threshold	VCC33 rising, hysteresis = 10%	85	90	95	%
$k_{POK;VCORE}$	VCORE power OK threshold	VCORE rising, hysteresis = 10%	85	90	95	%
$V_{SYS;DO}$	VSYS drop-out voltage	Minimum VM-VSYS at VSYS=5V, External load = 10mA		200		mV
C_{VSYS}	VSYS bypass capacitor value			4.7	10	µF
C_{VCC33}	VCC33 bypass capacitor value			2.2	10	µF
C_{VCORE}	VCORE bypass capacitor value			2.2	10	µF
C_{VCCIO}	VCCIO bypass capacitor value			0.1		µF
$R_{DSCH;VSYS}$	VSYS discharge resistance	LDO disabled		2.5		kΩ
R_{DSCH}	LDO output discharge resistance	LDO disabled		330		Ω

VM = 12V and T_A = -40°C to 105°C unless otherwise specified

Power Monitor Electrical Characteristics

Table 3 Power Monitor Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{REF}	Reference Voltage	T_A = 25°C	-0.5%	2.5	0.5%	V
		T_A = -40°C to 105°C		2.5		V
f_{CLKREF}	Trimmed CLKREF frequency	T_A = 25°C	3.96	4	4.05	MHz
		T_A = -40°C to 105°C	3.92	4	4.08	MHz
	Trimmed CLKREF jitter	T_A = -40°C to 85°C		0.5		%
k_{MON}	Power Monitoring Voltage coefficient	VCORE		1		V / V
		VSYS, VCC33		0.4		V / V
		VCP – VM		0.2		V / V
		VM		0.05		V / V
		OUTU, OUTV, OUTW		0.1		V / V

VM = 12V and T_A = -40°C to 105°C unless otherwise specified

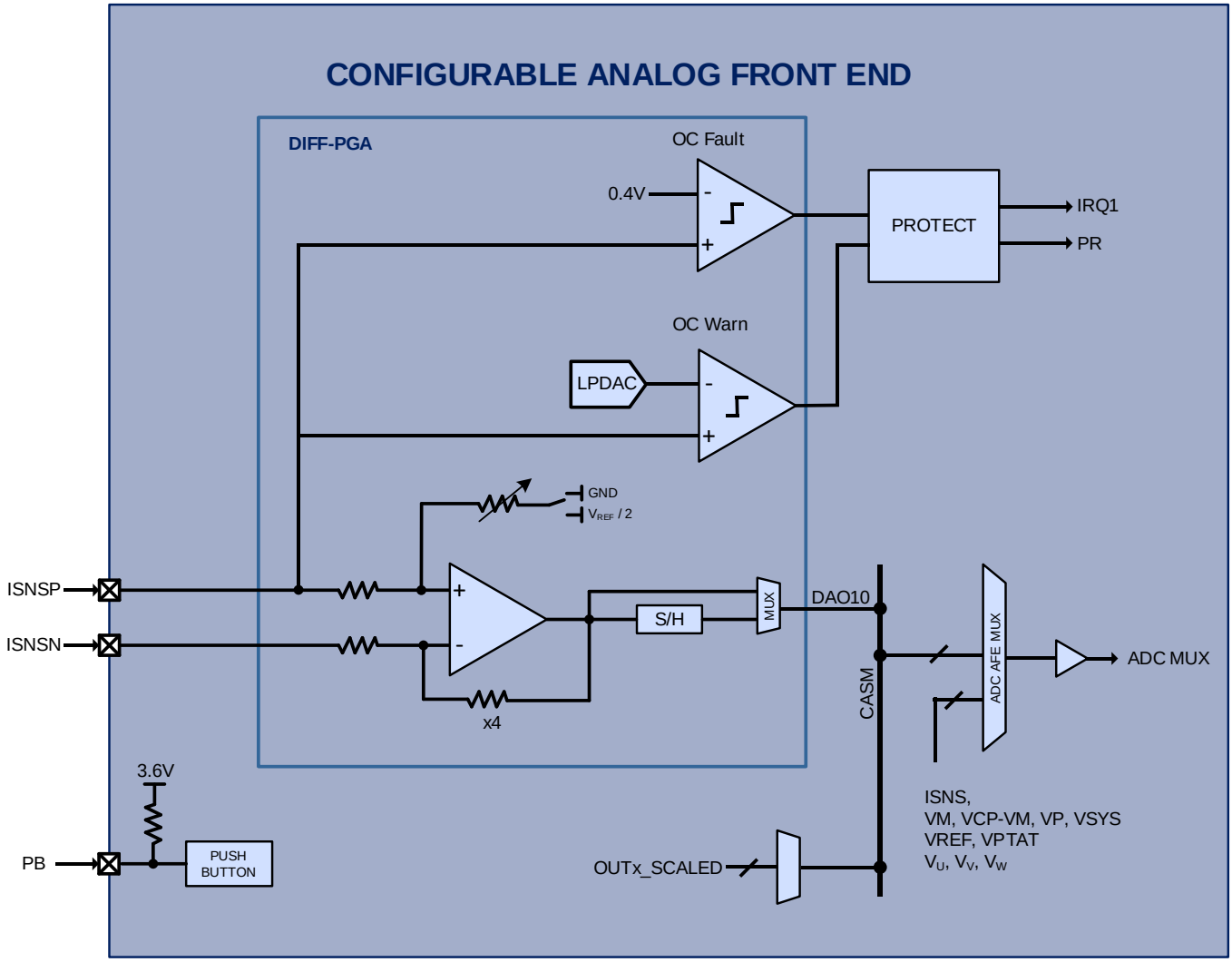
Configurable Analog Front-End (CAFE)

Features

- Differential Amplifier with configurable sample and hold
- Motor Over-Current Protection and Shutdown Comparator
- Programmable Over-Current Warning Comparator
- Power Monitoring
- Hibernate Push-Button Wake-up

Block Diagram

Figure 6 CAFE Block Diagram



Functional Description

The PAC5285 contains a Configurable Analog Front-End (CAFE™) available through analog pins on the device. These pins can be used to configure interconnect circuitry made up of 1 Differential Amplifier and a push-button hibernate wake-up.

The PAC5285 configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real-time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push-button function is provided for optional push button on, hibernate and off power management functions.

The CAFE™ also contains a power monitor MUX that allows all available power supplies to be sampled by the ADC for control and operation of the application.

Differential Amplifier (DA)

The PAC5285 contains one DA which may be used to sense motor current using an external sense resistor. The ISNSP pin is connected to the positive terminal of the amplifier and the ISNSN pin is connected to the negative terminal of the amplifier. The DA has a fixed gain of x4. The differential amplifier is optimized for use with signal source impedance lower than 500Ω and with matched source impedance on both positive and negative inputs for minimal offset. The effective gain is scaled by 80k / (80k + R_{SOURCE}), where R_{SOURCE} is the matched source impedance of each input.

The amplifier has -0.3V to 3.3V input common mode range, and its output can be configured for routing directly to the ADC pre-multiplexer, or through a sample-and-hold circuit synchronized with the ADC auto-sampling mechanism. Each amplifier is accompanied by offset calibration circuitry, and two protection comparators for protection event monitoring.

The output current of the motor phases will be 1.5A absolute maximum. BLDC motors may need to measure negative phase current (for FOC control), so the input voltage on the differential amplifier pins will need to be between -0.3V to 0.3V. This is then gained by x4 to 1.25V for the output of the differential amplifier and routed to the ADC analog input.

So, a typical current sense resistor would be 200mΩ:

- V = 0.25V
- I = 1.5A
- R = V / I = 0.25/1.5; so, R = 200mΩ

Over-Current Warnings and Faults

The PAC5285 has a fixed over-current fault threshold that is monitored by the OC Fault comparator. The OC Fault comparator has a fixed reference of 0.4V. With a 200mΩ sense resistor, this comparator will trip when the sensed current is above 1.5A, as shown in the formula above. When this comparator trips, the PR signal to the ASPD will be asserted and the gate drivers will be disabled. During this event, the IRQ1 signal to the MCU will not be asserted.

The PAC5285 has a programmable over-current warning threshold that is monitored by the OC Warn comparator. The OC Warn comparator has a reference that is set by the output of the 4-bit LPDAC. When this comparator trips, the IRQ1 signal to the MCU will be asserted.

Push Button (PBTN)

PB may be configured as a push-button input that is used to wake-up the PAC5285 when it is in hibernate mode. Before entering hibernate mode, the MCU can configure PB to be a wake-up source to exit hibernate mode. When a high-to-low transition is observed on PB, the CAFE will wake-up the device.

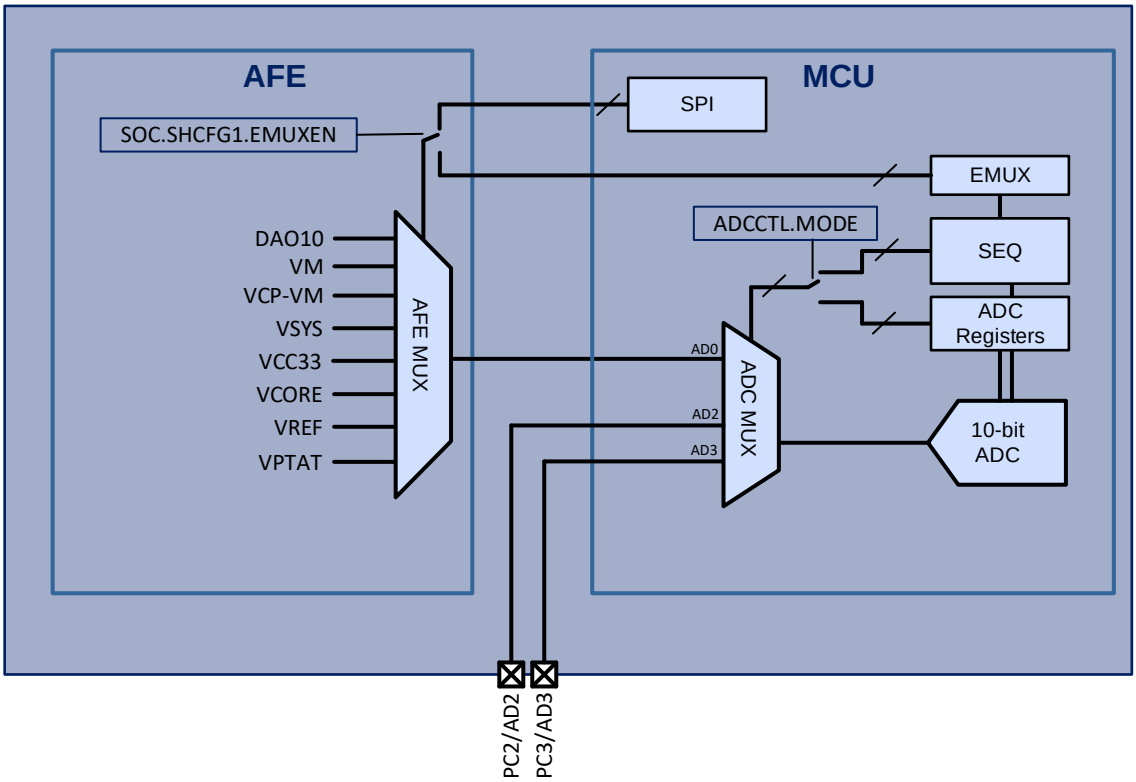
In addition, the PBTN may be used as a hardware reset for the MCU when it is held low for longer than 4s during normal operation.

The PBTN will be pulled up to 3.6V using a 50k resistor. Pulling this signal to ground will raise the push-button event.

ADC Analog Input

The PAC5285 has several different analog input channels that may be used for analog-to-digital conversions using the MCU ADC. The diagram below shows the hierarchy of MUXes that are available for analog signal sampling.

Figure 7 ADC Analog Input



The PAC5285 contains two analog MUXes:

- ADC MUX
- AFE MUX

The ADC MUX is an 8-channel MUX local to the ADC on the MCU that is directly controlled either by registers in the MCU, or automatically by the ADC DTSE. The output of the ADC MUX is sampled by the ADC. The AD0 input to the ADC MUX is connected to the AFE MUX. ADC MUX input channels AD2 and AD3 are directly connected to pins on the PAC5285.

The AFE MUX is an 8-to-1 MUX that selects between the Differential Amplifier (DAO10) output, power supply rails and the internal temperature sensor (VPTAT). This allows the ADC to rapidly sample the motor phase current, power supply rails, external voltage and temperature signals and the internal device temperature using the hardware sequencer on the device (DTSE).

For more information on controlling the various MUXes using the ADC and DTSE, see the PAC5285 User Guide.

Temperature Protection

The PAC5285 has two level of temperature protection. When the device reaches an internal temperature of 140°C, there is a mask-able interrupt that may be generated on IRQ1 to the MCU. The MCU may use this information to change the application behavior or disable the motor. The temperature warning status is cleared when the internal temperature falls below the temperature warning hysteresis threshold after the blanking time.

When the device reaches an internal temperature of 165°C, the device will shut down all power supplies and gate drivers. The device will re-start when the internal temperature falls below the temperature fault hysteresis threshold after the blanking time.

Electrical Characteristics

The Electrical Characteristics for the CAFE are shown below.

DA Electrical Characteristics

Table 4 DA Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{ICMR;DA}$	Input common mode range		-0.3		3.3	V
$V_{OLR;DA}$	Output linear range		0.1		V_{SYS} – 0.1	V
$V_{SHR;DA}$	Sample and hold range		0.1		3.5	V
$I_{CC;DA}$	Operating supply current	Each enabled amplifier		150		μA
$V_{OS;DA}$	Input offset voltage	Gain = 4x	-8		8	mV
$k_{CMRR;DA}$	Common mode rejection ratio		50	80		dB
	Slew rate	Gain = 4x	10			V/μs
$R_{INDIF;DA}$	Differential input impedance	Differential mode		80		kΩ
$t_{ST;DA}$	Settling time	To 1% of final value			360	ns
$A_{VZI;DA}$	Differential amplifier gain	Gain = 4x, V_{DAxP}=V_{DAxN}=0V, T_A = 25°C	-2	4	2	%

T_A = -40°C to 105°C unless otherwise specified

PB Electrical Characteristics

Table 5 PB Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{I;PBTN}$	Input voltage range		0		5	V
$V_{IH;PBTN}$	High-level input voltage		2			V
$V_{IL;PBTN}$	Low-level input voltage				0.8	V
$R_{PU;PBTN}$	Pull-up resistance	To 3.6V, push-button input mode; active-low		50		kΩ

T_A = -40°C to 105°C unless otherwise specified

Temperature Protection Electrical Characteristics

Table 6 Temperature Protection Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{WARN}	Temperature warning threshold			140		ºC
$T_{WARN;HYS}$	Temperature warning hysteresis			10		ºC
$T_{WARN;BLANK}$	Temperature warning blanking			10		μs
T_{FAULT}	Temperature fault threshold			165		ºC
$T_{FAULT;HYS}$	Temperature fault hysteresis			10		ºC
$T_{FAULT;BLANK}$	Temperature fault blanking			10		μs

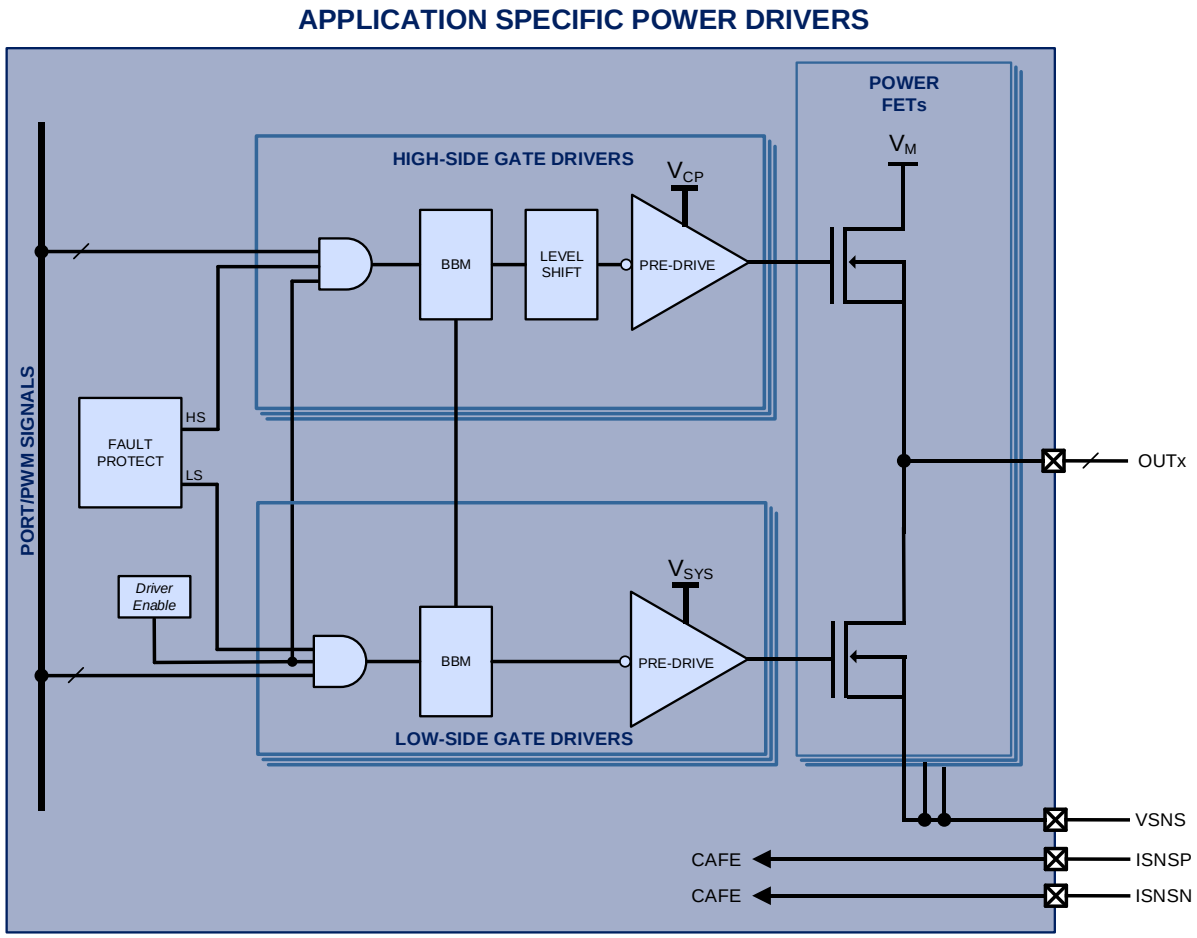
Application Specific Power Drivers (ASPD)

Features

- 3 High-side Level-shifters and Gate Drivers
- 3 Low-side Gate Drivers
- 6 40V/300mΩ Power MOSFETs for 3-phase BLDC motors
- Break-before-make Dead-Time Enforcement
- OC, UV and OV Protection

Block Diagram

Figure 8 ASPD Block Diagram



Functional Description

The Application Specific Power Drivers™ (ASPD) module handles power driving for motor control applications. The ASPD contains 3 high-side gate drivers, 3 low-side gate drivers and 6 N-CH Power MOSFETs to create 3 half H-bridge inverters used for three-phase BLDC motor applications.

Each motor phase is controlled by input signals from the MCU: a high-side PWM input and a low-side PWM input. The MCU performs dead-time insertion when used in complementary mode.

The break-before-make (BBM) unit enforces dead-time between the high-side and low-side gate drivers within a half-bridge. The high-side gate driver is supplied by VCP and the low-side is supplied by VSYS. The output of each motor phase is up to 500mA, with a typical current output of 200mA.

The ASPD also integrates gate driver over-current, VSNS fault, under-voltage and over-voltage protection. In the event of these failures, the ASPD is disabled and the MCU is notified through an interrupt.

The ASPD integrates gate driver over-current warning threshold that can 4 bit programable from 20mV to 320mV.

Electrical Characteristics

The Electrical Characteristics for the ASPD are shown below.

Table 7 ASPD Electrical Characteristics

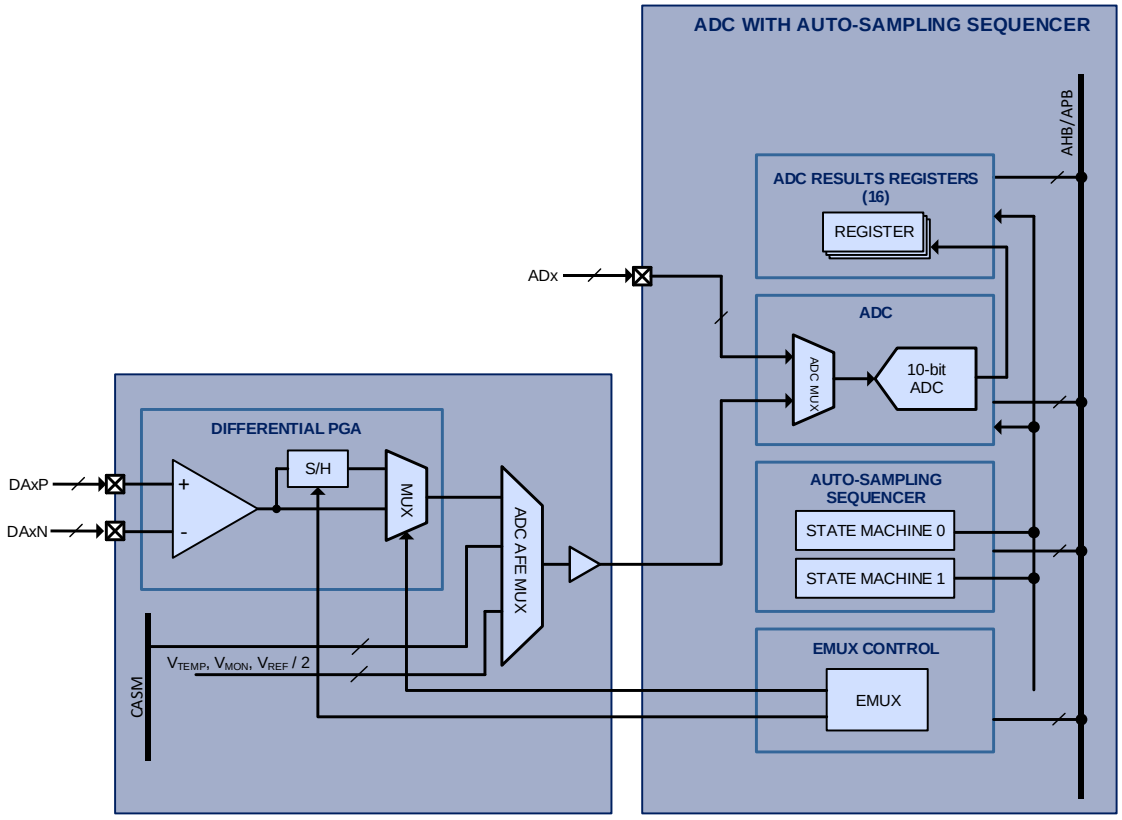
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{DS(ON)}$	Inverter MOSFET $R_{DS(ON)}$			300	600	mΩ
$V_{TH;OCP}$	Over-current protection threshold			0.4		V
$V_{TH;nIRQ}$	Warning current threshold	LPDAC = 1000b		0.16		V
$V_{FLT;SRC}$	VSNS fault threshold			0.5		V

T_A = -40°C to 105°C unless otherwise specified

ADC With Auto-Sampling Sequencer

Block Diagram

Figure 9 CAFE Block Diagram



Functional Description

ADC

The analog-to-digital converter (ADC) is a 10-bit successive approximation register (SAR) ADC with 1 µs conversion time and up to 1MSPS capability. The ADC input clock has a user-configurable divider from /1 to /8 of the system clock. The integrated analog multiplexer allows selection from up to 2 direct ADx inputs, the differential amplifier or several internally sampled voltages in the Configurable Analog Front End (CAFE). The ADC can be configured for repeating or non-repeating conversions and can interrupt the microcontroller when a conversion is finished.

Auto-Sampling Sequencer

Two independent and flexible auto-sampling sequencer state machines allow signal sampling using the ADC without interaction from microcontroller core. Each auto-sampling sequencer state machine can be programmed to take and store up to 8 samples each in the ADC result register from different analog inputs, able to control the ADC MUX and ADC AFE MUX as well as the precise timing of the S/H in the Configurable analog front end. The sampling start of the auto-sampling sequencer can be precisely triggered using timers A, B, C, or D or any of their associated PWM edges (high-to-low or low-to-high). It also supports manual start or a ping-pong-scheme, where one auto-sampling sequencer state machine triggers the other when it finishes sampling.

The auto-sampling sequencer can interrupt the microcontroller when either conversion sequence is finished.

EMUX Control

A dedicated low latency interface controllable by the auto-sampling sequencer or register control allows changing the ADC AFE MUX and asserting/de-asserting the S/H circuit in the configurable analog front end, allowing back to back conversions of multiple analog inputs without microcontroller interaction.

Electrical Characteristics

Table 8 ADC and Auto-Sampling Sequencer Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ADC						
f_{ADCLK}	ADC conversion clock input				16	MHz
t_{ADCONV}	ADC conversion time	f_{ADCLK} = 16MHz			1	µs
	ADC resolution			10		bits
	ADC effective resolution		9.2			bits
	ADC differential non-linearity (DNL)			±0.5		LSB
	ADC integral non-linearity (INL)			±1		LSB
	ADC offset error			0.6		%FS
	ADC gain error			0.12		%FS
Reference Voltage						
V_{REFADC}	ADC reference voltage input			2.5		V
Sample and Hold						
t_{ADCSH}	ADC sample and hold time	f_{ADCLK} = 16MHz		188		ns
C_{ADCIC}	ADC input capacitance			1.3		pF
Input Voltage Range						
V_{ADCIN}	ADC input voltage range	ADC multiplexer input	0		V_{REFADC}	V
EMUX Clock Speed						
$f_{EMUXCLK}$	EMUX engine clock input				50	MHz

V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified

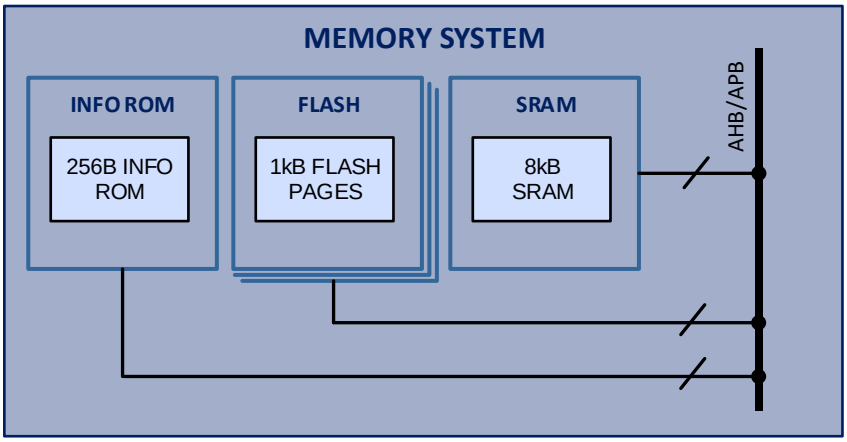
Memory System

Features

- 32kB embedded FLASH
  - 100,000 program/erase cycles
  - 10 years data retention
- 8kB SRAM

Block Diagram

Figure 10 CAFE Block Diagram



Functional Description

The device has multiple banks of embedded FLASH memory, SRAM memory, as well as peripheral control registers that are all program-accessible in a flat memory map.

Program and Data FLASH

32kB in 32 pages of 1kB each is available for program or data memory. Each of them can be individually erased or written to while the microcontroller is executing a program from SRAM.

SRAM

Up to 8kB contiguous array of SRAM is available for non-persistent data storage. The SRAM memory supports word (4-byte), half-word (2-byte) and byte address aligned access. The microcontroller may execute code out of SRAM for time-critical applications, or when modifying the contents of FLASH memory.

Electrical Characteristics

Table 9 ADC and Auto-Sampling Sequencer Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Embedded FLASH						
$t_{READ;FLASH}$	FLASH read time		40			ns
$t_{WRITE;FLASH}$	FLASH write time		20			µs
$t_{PERASE;FLASH}$	FLASH page erase time				10	ms
$N_{PERASE;FLASH}$	FLASH program/erase cycles		10k	100k		cycles
$t_{DR;FLASH}$	FLASH data retention		10			years
SRAM						
t_{SRAM}	SRAM access cycle time		20			ns

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

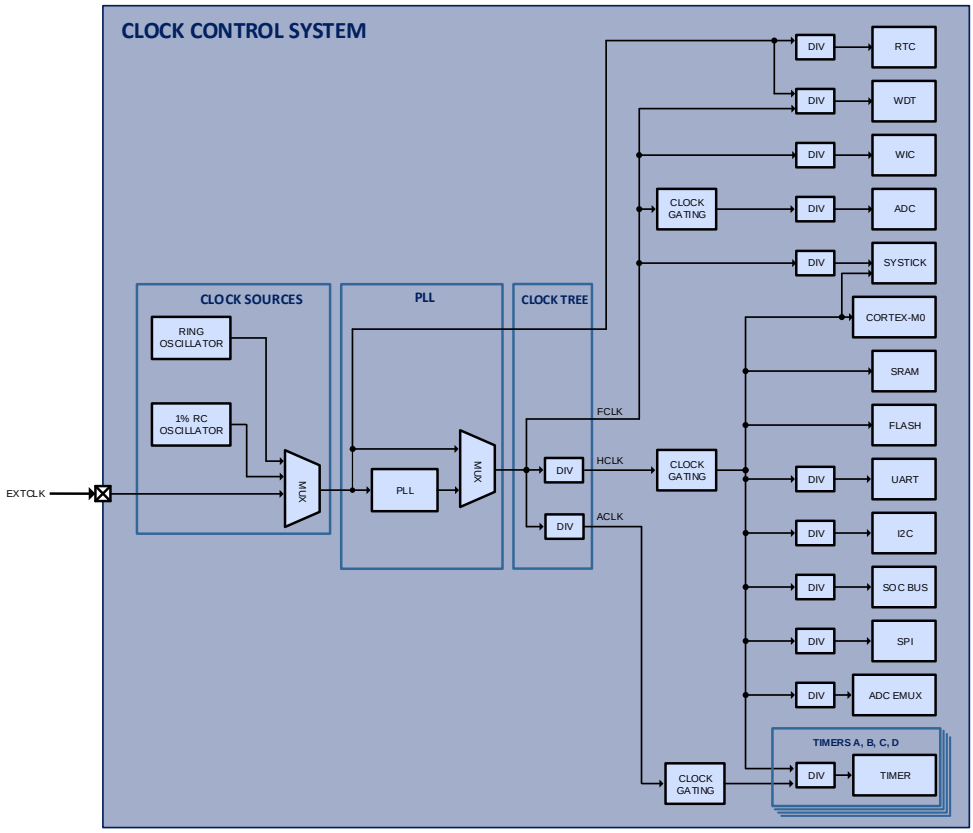
Clock Control System

Features

- Ring oscillator with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings
- High accuracy 2% trimmed 4MHz RC oscillator
- Crystal oscillator driver supporting 2MHz to 10MHz crystals
- External clock input up to 40MHz
- PLL with 1MHz to 25 MHz input, and 3.5MHz to 100MHz output
- /1 to /8 clock divider for HCLK
- /1 to /128 clock divider for ACLK

Block Diagram

Figure 11 CCS Block Diagram



Functional Description

The PAC clock control system covers a wide range of applications.

Free Running Clock (FRCLK)

The free running clock (FRCLK) is generated from one of the 4 clock sources: ring oscillator, trimmed RC oscillator, crystal driver or external clock input. The FRCLK is used for the real-time clock (RTC), watchdog timer (WDT), input to the PLL, or FCLK source to clock the system in low power and sleep mode.

Fast Clock (FCLK)

The fast clock (FCLK) is generated from the PLL or supplied by the FRCLK directly. The FCLK supplies the watchdog timer (WDT), ADC, wake-up interrupt controller (WIC), SysTick timer, Arm® Cortex®-M0 peripheral high speed clock (HCLK) and low speed clock (LSCLK).

High-Speed Clock (HCLK)

The high-speed clock (HCLK) is derived from the FCLK with a /1, /2, /4 or /8 divider. It supplies the peripheral AHB/APB bus, Timers A to D, dead-time controllers, SPI interface, I^2C interface, UART interface, EMUX interface, SOC bus bridge and memory subsystem, and can go as high as 50MHz.

Auxiliary Clock (ACLK)

The auxiliary clock (ACLK) is derived from FCLK with a /1, /2, to /128 divider, and supplies the timer and dead-time blocks. It can be clocked faster or slower than HCLK and can go as high as 100MHz.

Clock Gating

The clock tree supports clock gating in deep-sleep mode for the timer block, ADC, SPI interface, I^2C interface, UART interface, memory subsystem and the Arm® Cortex®-M0 itself.

Ring Oscillator (ROSC)

The integrated ring oscillator provides 4 different clocks with 7.5MHz, 9.6MHz, 13.8MHz, and 25.7MHz settings. After reset, the clock tree always defaults to this clock input with the lowest frequency setting.

Trimmed 4MHz RC Oscillator

The 2% trimmed 4MHz RC oscillator provides an accurate clock suitable for many applications. It is also used to derive the clock for the Multi-Mode Power Manager.

Internal Slow RC Oscillator

An internal 32kHz RC oscillator is used during start up to provide an initial clock to analog circuitry. It is not used as a clock input to the clock tree.

Crystal Oscillator Driver

The optional crystal oscillator driver can drive crystals from 2MHz to 10MHz to provide a highly accurate and stable clock into the system.

External Clock Input

The clock tree can be supplied with an external clock up to 10MHz.

PLL

The integrated PLL input clock is supplied by the FRCLK with an input frequency range of 1MHz to 25MHz. The PLL output frequency is adjustable from 3.5MHz to 100MHz.

Electrical Characteristics

Table 10 CCS Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Clock Tree (FRCLK, FCLK, HCLK and ACLK)						
f_{FRCLK}	Free-running clock frequency				50	MHz
f_{FCLK}	Fast clock frequency				100	
f_{HCLK}	High-speed clock frequency				100	
f_{ACLK}	Auxilliary clock frequency				100	
Internal Oscillators						
f_{ROSC}	Ring oscillator frequency	Frequency setting = 11b		7.5		MHz
		Frequency setting = 10b		9.6		
		Frequency setting = 01b		13.8		
		Frequency setting = 00b		25.7		
f_{TRIM}	Trimmed RC oscillator frequency	T_A = 25°C	-1.25%	4	1.25%	MHz
		T_A = -40°C to 105°C	-2%	4	2%	
	Trimmed RC oscillator clock jitter	T_A = -40°C to 85°C		0.5		%
External Clock Input						
f_{EXTCLK}	External clock input frequency range				40	MHz
$t_{HIGH;EXTCLK}$	External clock high time		10			ns
$t_{LOW;EXTCLK}$	External clock low time		10			ns
PLL						
f_{INPLL}	PLL input frequency range		2		25	MHz
f_{OUTPLL}	PLL output frequency range		3.5		100	MHz
	PLL settling time			0.5		ms
	PLL period jitter	RMS		30		ps
		Peak to peak		±150		

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

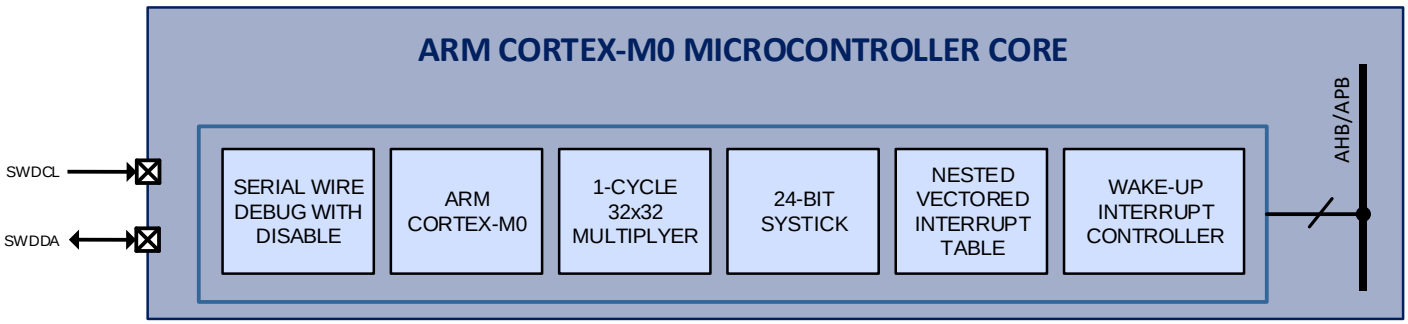
Arm® CORTEX®-M0 Microcontroller Core

Features

- Arm® Cortex®-M0 core
- Fast single-cycle 32-bit x 32-bit multiplier
- 24-bit SysTick timer
- Up to 50MHz operation
- Serial wire debug (SWD), with 4 breakpoint and 2 watch-point unit comparators
- Nested vectored interrupt controller (NVIC) with 25 external interrupts
- Wake-up interrupt controller (WIC) with GPIO, real-time clock (RTC) and watchdog timer (WDT) interrupts enabled
- Sleep and deep-sleep mode with clock gating

Block Diagram

Figure 12 Arm® Cortex®-M0 Microcontroller Core Block Diagram



Functional Description

The Arm® Cortex®-M0 microcontroller core is configured for little endian operation and includes the fast single-cycle 32-bit multiplier and 24-bit SysTick timer and can operate at a frequency of up to 50MHz.

The microcontroller nested vectored interrupt controller (NVIC) supports 25 external interrupts for the device's peripherals and sub-systems. For low-latency interrupt processing, the NVIC also supports interrupt tail-chaining. The wake-up interrupt controller (WIC) can wake up the device from low-power modes using any GPIO interrupt, as well as from the RTC or WDT. The Arm® Cortex®-M0 supports both sleep and deep-sleep low-power modes. The deep-sleep mode supports clock gating to limit standby power even further.

Firmware debug support includes 4 breakpoint and 2 watch-point unit comparators using the serial wire debug (SWD) protocol. The serial wire debug mechanism can be disabled to prevent device access to the firmware in the field.

Electrical Characteristics

Table 11 Microcontroller Electrical Characteristics

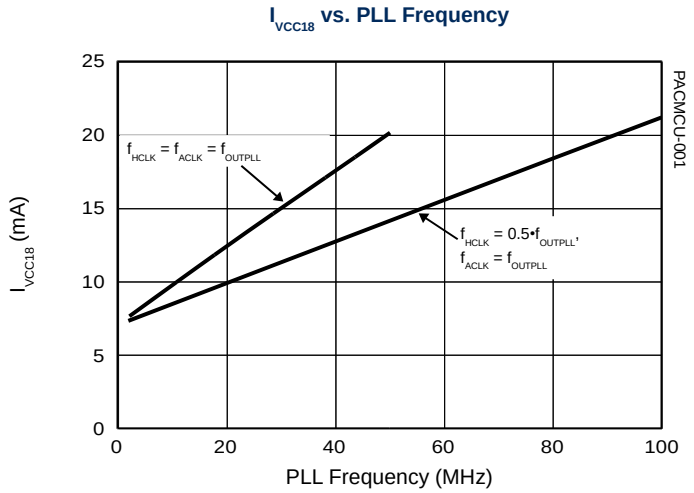
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{HCLK}	Microcontroller clock	HCLK			50	MHz
$I_{OP;VSYS}$	V_{SYS} operating supply current	$f_{FRCLK} = f_{HCLK} = f_{ACLK}$ = ROSC 11b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	2.5[1]	3.4	7	mA
		$f_{FRCLK} = f_{HCLK} = f_{ACLK}$ = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	3.0[1]	5.3	9.5	
		$f_{FRCLK} = f_{HCLK} = f_{ACLK}$ = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	4.1[1]	5.3	9.5	
		$f_{FRCLK} = f_{HCLK} = f_{ACLK}$ = ROSC 01b, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	7.4[1]	9	15	
		$f_{FRCLK} = f_{HCLK} = f_{ACLK}$ = CLKREF, PLL disabled, CPU halt; other clock sources, ADC, timers, and serial interface disabled	1.5[1]	2.3	4.4	
		f_{FRCLK} = 4MHz CLKREF, f_{HCLK} = 50MHz, $f_{ACLK} = f_{OUTPLL}$ = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interface disabled	3.6[1]	4.5	6.7	
		f_{FRCLK} = 4MHz CLKREF, f_{HCLK} = 50MHz, $f_{ACLK} = f_{OUTPLL}$ = 100MHz, CPU halt; other clock sources, ADC, timers, and serial interface disabled	20.9[1]	23.3	26.5	
$I_{Q;VCCIO}$	VCCIO quiescent supply current			0.02		mA

($V_{SYS} = V_{CCIO}$ = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

[1] All minimum operating supply current values are for room temperature only

Typical Performance Characteristics

Figure 13 Arm® Cortex®-M0 Microcontroller Core



(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = 25°C unless otherwise specified.)

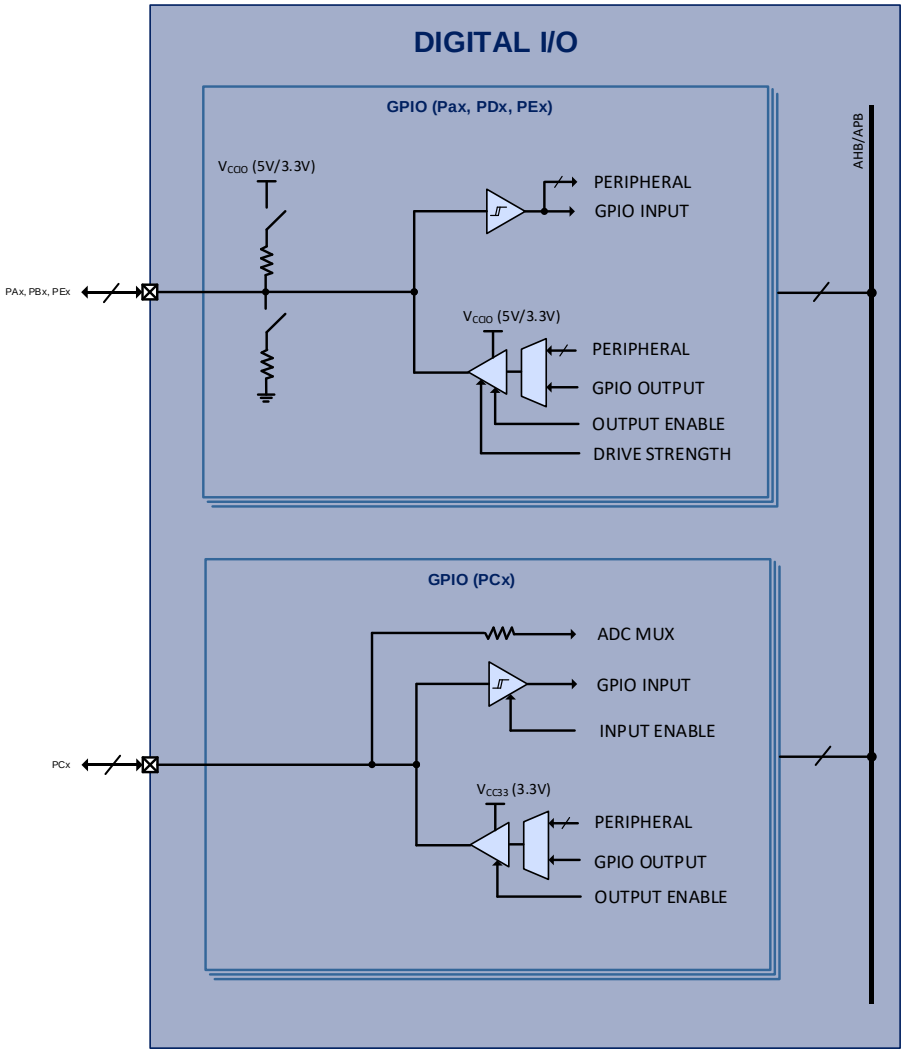
I/O Controller

Features

- 5V-compliant I/O PAx, PDx, PEx
- 3.3V-compliant I/O PCx
- Configurable drive strength on PAx, PDx, PEx
- Configurable pull-up or pull-down on PAx, PDx, PEx

Block Diagram

Figure 14 I/O Controller Block Diagram



Functional Description

The PAC can support up to 4 ports with 8 I/Os each from PAx, PCx, PDx, and PEx, in addition to the I/Os on the analog front end. All PAx, PCx, PDx, and PEx ports have interrupt capability with configurable interrupt edge.

PAx, PDx, and PEx I/Os use V_{CCIO} as the I/O supply voltage that is 5V on default parts (and 3.3V available from factory). The drive current can be configured as 8mA or 16mA. They also support weak pull-up and pull-down to save external components.

PCx uses V_{CC33} as its I/O supply voltage. The drive current is fixed to 8mA. PC0 to PC5 are also associated with analog inputs AD0 to AD5 to the ADC.

GPIO Current Injection

Under normal operation, there should not be current injected into the GPIOs on the device due to the GPIO voltage below ground or above the GPIO supply.[2] Current injected occurs when the GPIO pin voltage is less than -0.3V or when greater than GPIO supply + 0.3V.

In order provide a robust solution when this situation occurs, this device allows a small amount of injected current into the GPIO pins, to avoid excessive leakage or device damage.

For information on the GPIO current injection thresholds, see the absolute maximum parameters for this device.

Sustained operation with the GPIO pin voltage greater than the GPIO supply or when the GPIO pin voltage is less than -0.3V may result in reduced lifetime of the device. GPIO current injection should only be a temporary condition.

[2] VCC33 is the supply for any PC GPIO pin and VCCIO is the supply for any other GPIO pins.

Electrical Characteristics

Table 12 ADC and Auto-Sampling Sequencer Electrical Characteristics

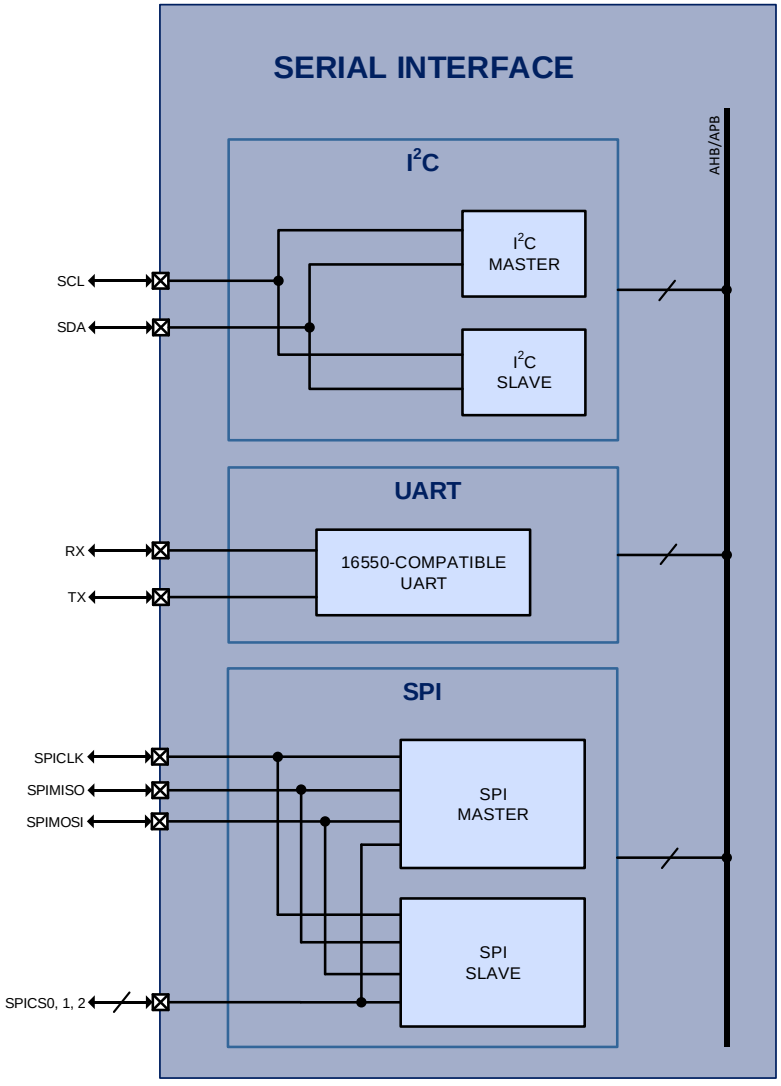
Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
PAx, PDx, PEx (5V Operation)							
V_{IH}	High-level input voltage	V_{CCIO} = 5V		3			V
V_{IL}	Low-level input voltage	V_{CCIO} = 5V				0.8	V
I_{OL}	Low-level output sink current	V_{CCIO} = 5V, V_{OL} = 0.4V	Drive strength setting = 0b	7			mA
			Drive strength setting = 1b	15			
I_{OH}	High-level output source current	V_{CCIO} = 5V, V_{OH} = 2.4V	Drive strength setting = 0b			-7	mA
			Drive strength setting = 1b			-15	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 5V		53	66	87	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 5V		63	108	244	kΩ
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA
PAx, PDx, PEx (3.3V Operation)							
V_{IH}	High-level input voltage	V_{CCIO} = 3.3V		2			V
V_{IL}	Low-level input voltage	V_{CCIO} = 3.3V				0.8	V
I_{OL}	Low-level output sink current	V_{CCIO} = 3.3V, V_{OL} = 0.4V	Drive strength setting = 0b	4			mA
			Drive strength setting = 1b	8			
I_{OH}	High-level output source current	V_{CCIO} = 3.3V, V_{OH} = 2.4V	Drive strength setting = 0b			-4	mA
			Drive strength setting = 1b			-8	
R_{PU}	Weak pull-up resistance	V_{CCIO} = 3.3V		47	74	104	kΩ
R_{PD}	Weak pull-down resistance	V_{CCIO} = 3.3V		50	84	121	kΩ
I_{IL}	Input leakage current	T_A = 125°C		-10	0	10	µA
PCx (3.3V Operation)							
VIH	High-level input voltage	V_{CC33} = 3.3V		2			V
VIL	Low-level input voltage	V_{CC33} = 3.3V				0.8	V
IOL	Low-level output sink current	V_{CC33} = 3.3V, V_{OL} = 0.4V		7			mA
IOH	High-level output source current	V_{CC33} = 3.3V, V_{OH} = 2.4V				-7	mA
IIL	Input leakage current	T_A = 125°C		-10	0	10	µA

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

Serial Interface

Block Diagram

Figure 15 Serial Interface Block Diagram



Functional Description

The device has up to three serial interfaces: I²C, UART, and SPI.

I²C Controller

The I²C controller is a configurable peripheral that can support various modes of operation:

- I²C master operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Single and multi-master
  - Synchronization (multi-master)
  - Arbitration (multi-master)
  - 7-bit or 10-bit slave addressing
- I²C slave operation
  - Normal mode (100kHz), fast mode (400kHz), or fast mode plus (1MHz)
  - Clock stretching
  - 7-bit or 10-bit slave addressing

The I²C peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit data.

UART Controller

The UART peripheral is a configurable peripheral that can support various features and modes of operation:

- Programmable clock selection
- National Instruments PC16550D compatible
- 16-deep transmit and receive FIFO and fractional clock divisor
- Up to 3.125Mbps communication speed (with HCLK = 50MHz)

The UART peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit data.

SPI Controller

The device contains an SPI controller that can each be used in either master or slave operation, with the following features:

- SPI master operation
  - Control of up to three different SPI slaves
  - Operation up to 25MHz
  - Flexible multiple transmit mode for variable-size SPI data with user-defined chip-select behavior
  - Chip select “shaping” through programmable additional delay for chip-select setup, hold and wait time for back-to-back transfers
- SPI master or slave operation
  - Supports clock phase and polarity control
  - Data transmission/reception can be on 8-, 16-, 24- or 32-bit boundary
  - Selectable data bit ordering (LSB or MSB first)
  - Programmable chip select polarity
  - Selectable “auto-retransmit” mode

The SPI peripheral may operate either by polling or can be configured to be interrupt driven for both receive and transmit data.

Dynamic Characteristics

Table 13 Serial Interface Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I2C						
f_{I2CCLK}	I2C input clock frequency	Standard mode (100kHz)	2.8			MHz
		Fast mode (400kHz)	2.8			MHz
		Fast mode plus (1MHz)	6.14			MHz
UART						
$f_{UARTCLK}$	UART input clock frequency				f_{HCLK}/16	MHz
	UART baud rate	f_{HCLK} = 50MHz			3.125	Mbps
SPI						
f_{SPICLK}	SPI input clock frequency	Master mode			f_{HCLK}/2	MHz
		Slave mode			f_{HCLK}/2	MHz

(V_{SYS} = V_{CCIO} = 5V, V_{CC33} = 3.3V, V_{CC18} = 1.8V, and T_A = -40°C to 105°C unless otherwise specified.)

Table 14 I2C Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency	Standard mode	0		100	kHz
		Fast mode	0		400	
		Fast mode plus	0		1000	
t_{LOW}	SCL clock low	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_{HIGH}	SCL clock high	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;STA}$	Hold time for a repeated START condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{SU;STA}$	Set-up time for a repeated START condition	Standard mode	4.7			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	
		Fast mode plus	0			
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
$t_{SU;STO}$	Set-up time for STOP condition	Standard mode	4.0			µs
		Fast mode	0.6			
		Fast mode plus	0.26			
t_{BUF}	Bus free time between a STOP and START condition	Standard mode	4.7			µs
		Fast mode	1.3			
		Fast mode plus	0.5			
t_r	Rise time for SDA and SCL	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t_f	Fall time for SDA and SCL	Standard mode			300	ns
		Fast mode			300	
		Fast mode plus			120	
C_b	Capacitive load for each bus line	Standard mode, fast mode			400	pF
		Fast mode plus			550	

Figure 16 I2C Timing Diagram

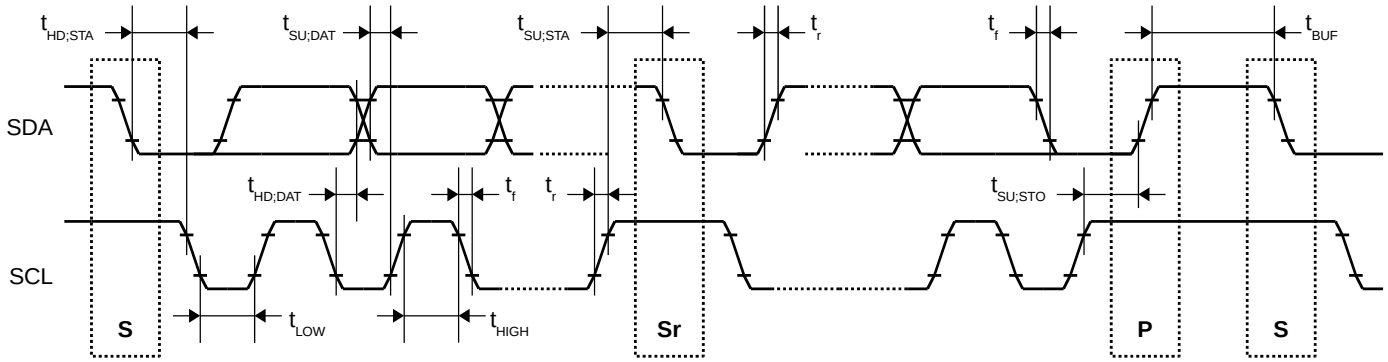
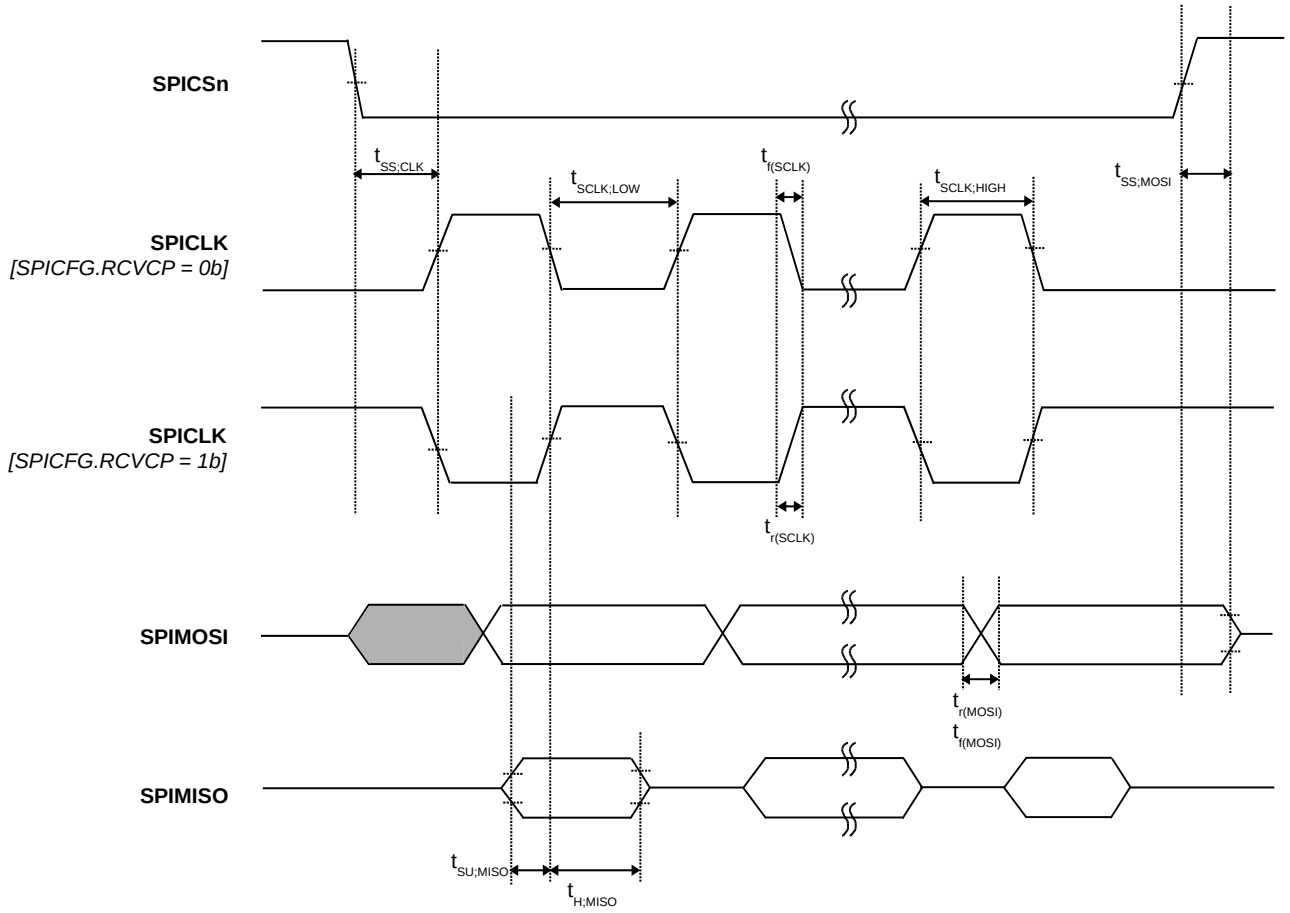


Table 15 SPI Dynamic Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{SCLK;HIGH}$	SPICLK Input High Time	SPICLK = 25MHz	30			ns
$t_{SCLK;LOW}$	SPICLK Input Low Time		30			ns
$t_{SS;SCLK}$	SPICSn to SPICLK Time		120			ns
$t_{SS;MOSI}$	SPICSn to SPIMISO High-impedance time		10		50	ns
$t_{r(SCLK)}$	SPICLK Rise Time			10	25	ns
$t_{f(SCLK)}$	SPICLK Fall Time			10	25	ns
$t_{r(MOSI)}$	SPIMISO Rise Time			10	25	ns
$t_{f(SMOSI)}$	SPIMISO Fall Time			10	25	ns
$t_{SU;MISO}$	SPIMISO Setup Time		20			ns
$t_{H;MISO}$	SPIMISO Hold Time		20			ns

Figure 17 SPI Timing Diagram



Timers

Block Diagrams

Figure 18 PWM Timers Block Diagram

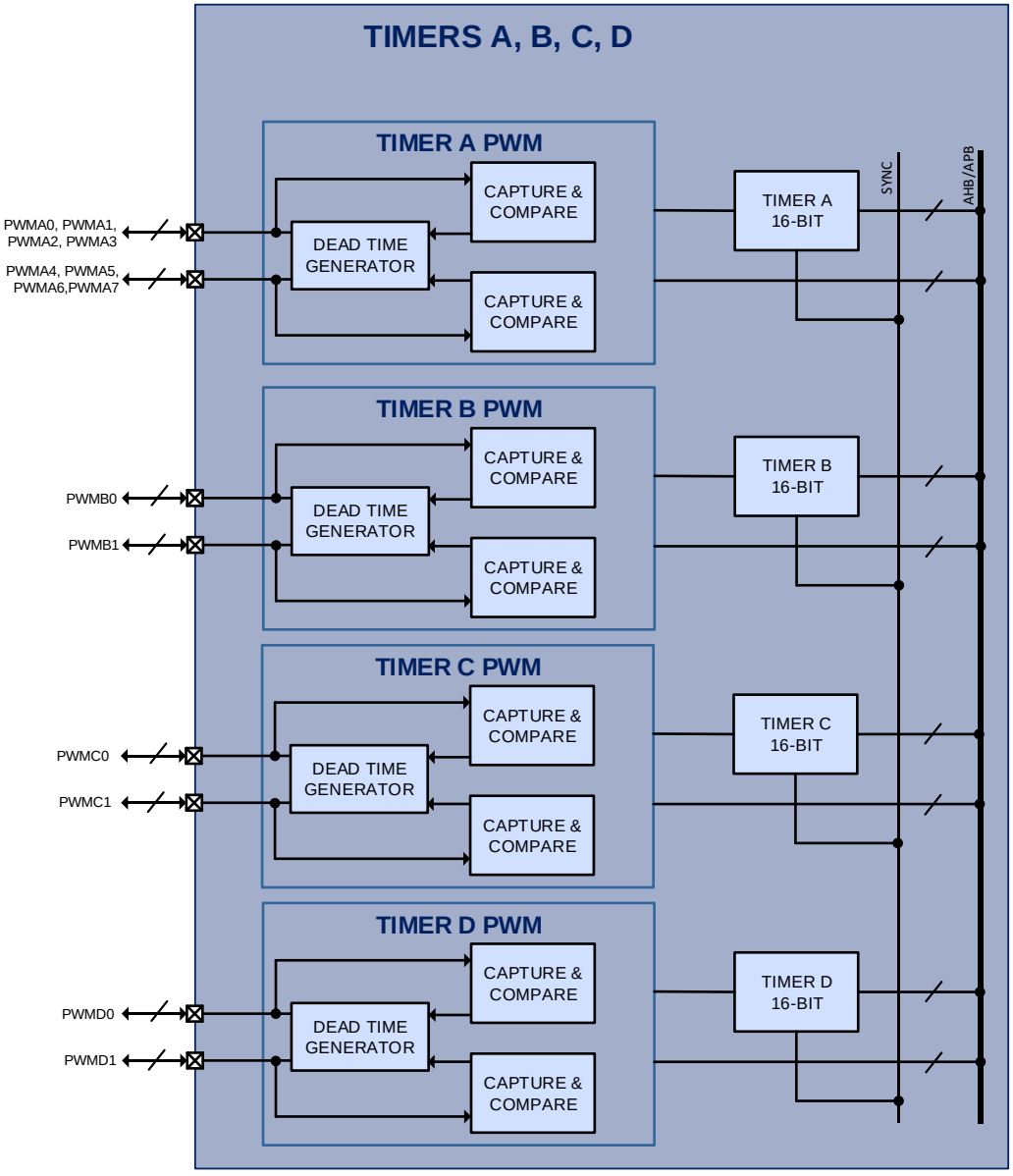


Figure 19 AFE Watchdog and Wake-up Timer Block Diagram

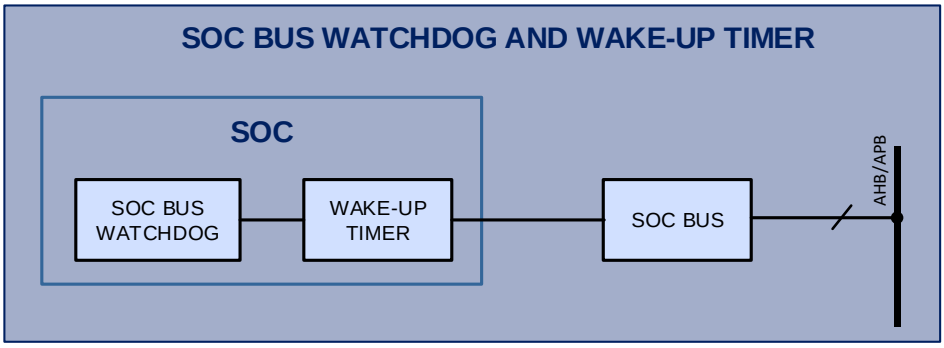
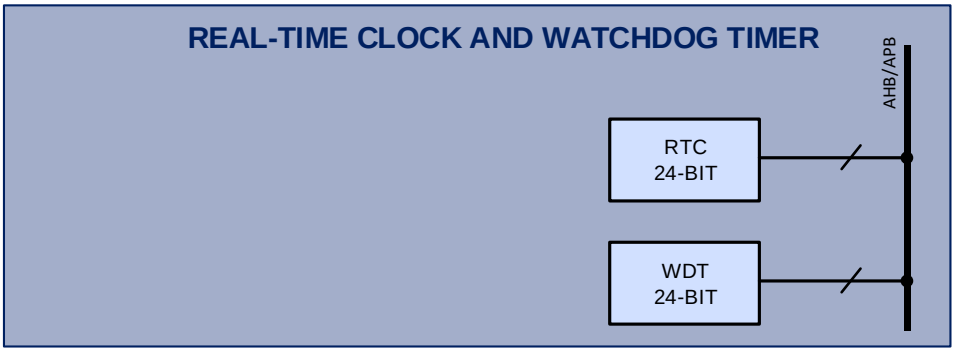


Figure 20 Real-time Clock and Watchdog Timer Block Diagram



Functional Description

The device includes 9 timers: timer A, timer B, timer C, timer D, watchdog timer 1 (WDT), watchdog timer 2, wake-up timer, real-time clock (RTC), and SysTick timer. The device supports up to 14 different PWM signals and has up to 7 dead-time controllers. Timers A, B, C and D can be concatenated to synchronize to a single clock and start/stop signal for applications that require a synchronized timer period between timers.

Timer A

Timer A is a general purpose 16-bit timer with 8 PWM/capture and compare units. It has 4 pairs of PWM signals going into 4 dead-time controllers. Timer A can be concatenated with timers B, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Timer B

Timer B is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller, as well as 2 additional compare units that can be used for additional system time bases for interrupts. Timer B can be

concatenated with timers A, C, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Timer C

Timer C is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer C can be concatenated with timers A, B, and D to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Timer D

Timer D is a general purpose 16-bit timer with 2 PWM/capture and compare units. It has one pair of PWM signals going into one dead-time controller. Timer D can be concatenated with timers A, B, and C to synchronize the PWM/capture and compare units. It can use either ACLK or HCLK as clock input with an additional clock divider from /1 to /128.

Watchdog Timer

The 24-bit watchdog timer (WDT) can be used for long time period measurements or periodic wake up from sleep mode. The watchdog timer can be used as a system watchdog, or as an interval timer, or both. The watchdog timer can use either FRCLK or FCLK as clock input with an additional clock divider from /2 to /65536.

CAFE Watchdog Timer

There is a second watchdog timer in the AFE that can be used to monitor communication between the MCU and AFE on the PAC SOC bus. If this timer expires, it will trigger a device reset when there is no communication for a period of either 4s or 8s.

Wake-Up Timer

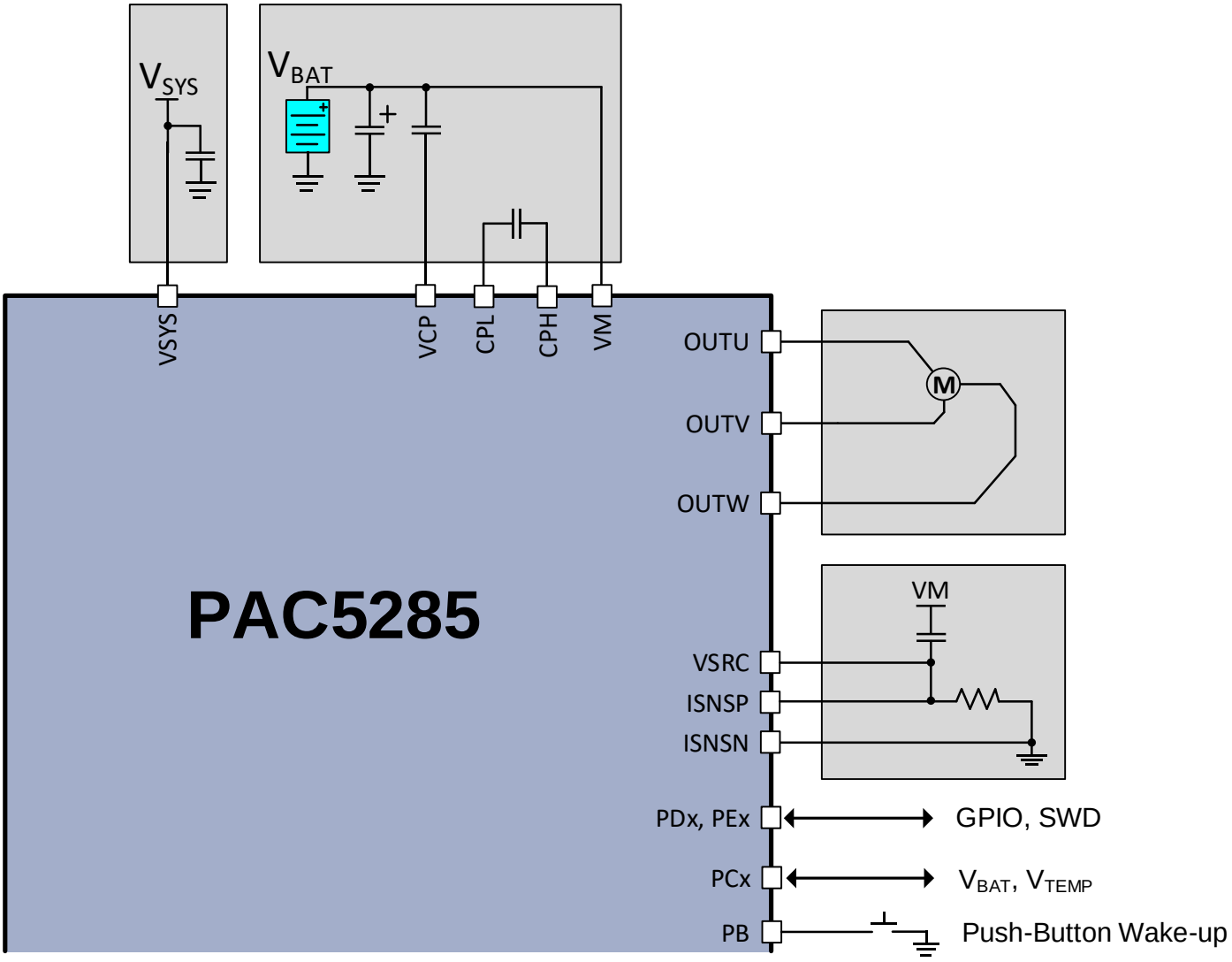
The wake-up timer can be used for very low power hibernate and sleep modes to wake up the micro controller periodically. It can be configured to be 125ms, 250ms, 500ms, 1s, 2s, 4, or 8s.

Real-Time Clock

The 24-bit real-time clock (RTC) can be used for time measurements when an accurate clock source is used. This timer can also be used for periodic wake up from sleep mode. The RTC uses FRCLK as clock input with an additional clock divider from /2 to /65536.

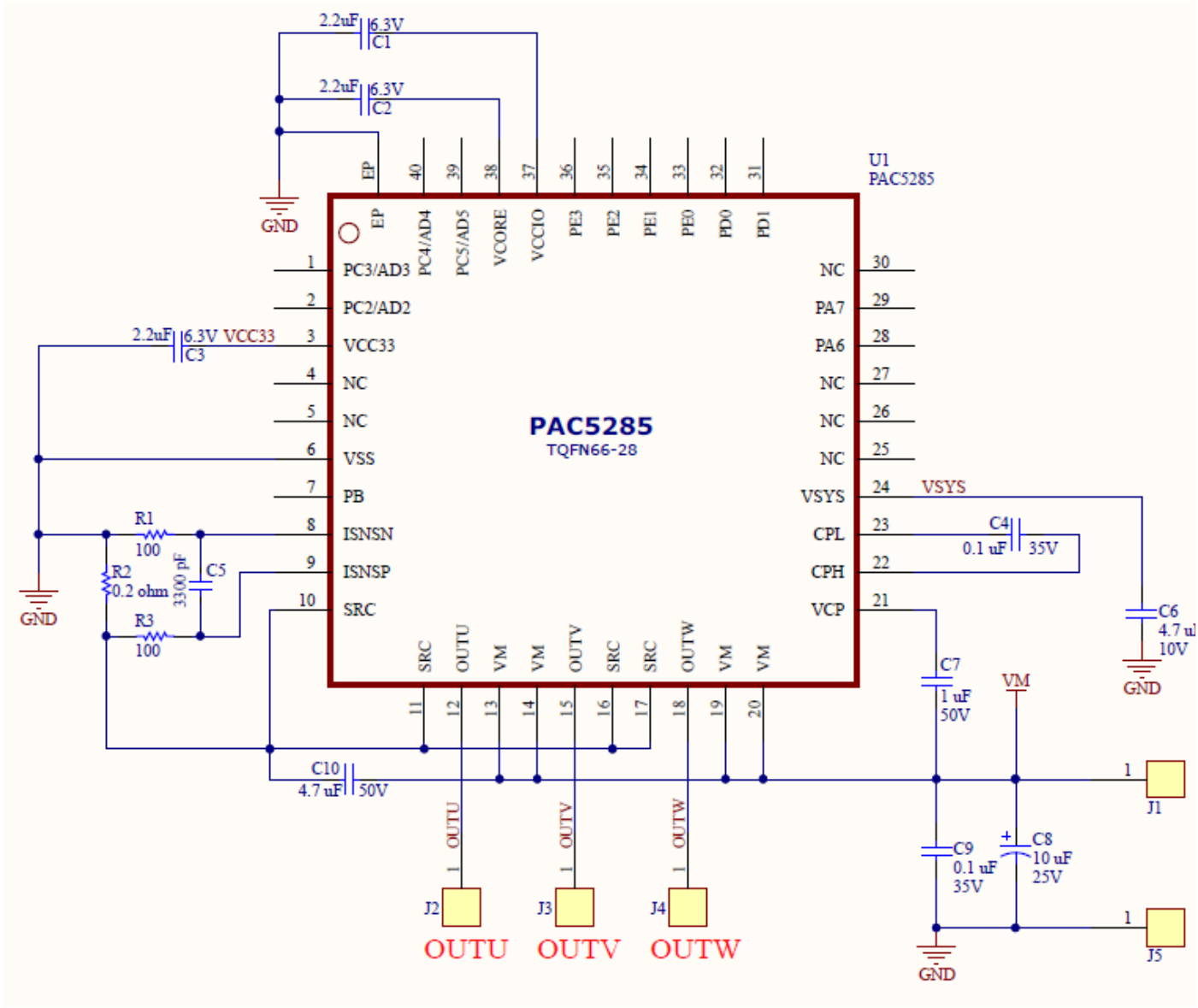
Application Block Diagram

Figure 21 PAC5285 Application Block Diagram



Application Reference Schematic

Figure 22 PAC5285 Application Reference Schematic



Thermal Characteristics

Table 16 Thermal Characteristics

SYMBOL	PARAMETER	VALUE	UNIT
T_A	Operating ambient temperature range	-40 to 105	°C
T_J	Operating junction temperature range	-40 to 125	°C
T_{STG}	Storage temperature range	-55 to 150	°C
	Lead temperature (Soldering, 10 seconds)	300	°C
Θ_{JC}	Junction-to-case thermal resistance	2.897	°C/W
Θ_{JA}	Junction-to-ambient thermal resistance	23.36	°C/W

Pin Configuration and Description

Figure 23 Pin Diagram – Top View

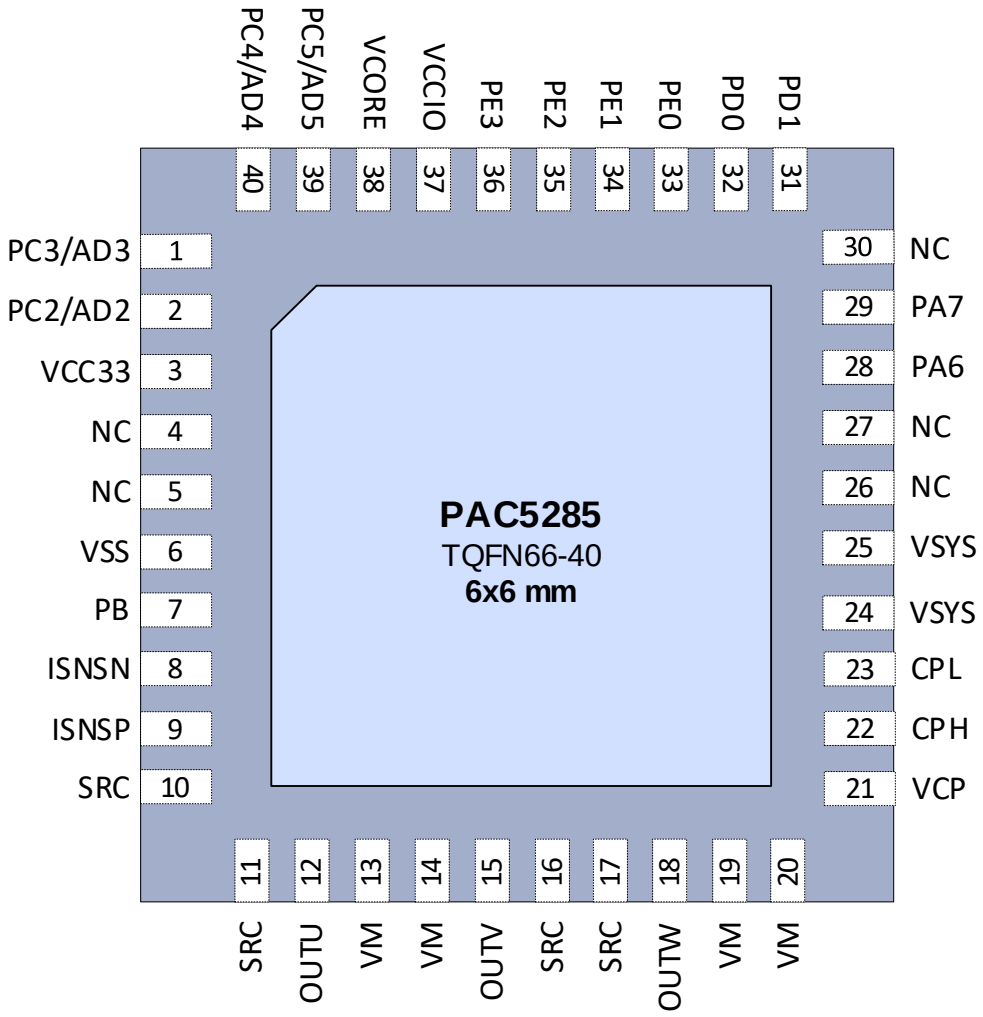


Table 17 – Pin Descriptions

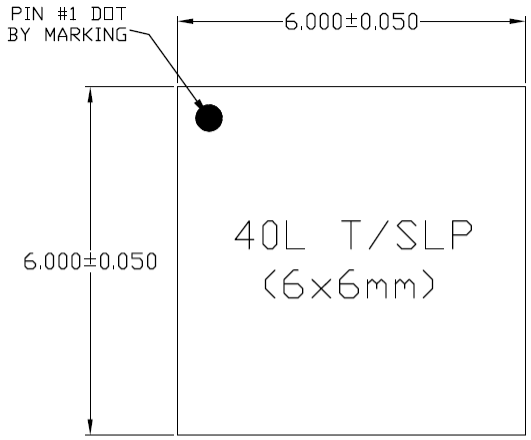
Pin Number	Label	Description
1	PC3/AD3	IO port PC3 or ADC channel AD3.
2	PC2/AD2	IO port PC2 or ADC channel AD2.
3	VCC33	Internally generated 3.3V power supply. Connect to a 10V/1µF ceramic capacitor from VCC33 to VSS close to the device.
4	NC	Not connected. Leave floating.
5	NC	Not connected. Leave floating.
6	VSS	Ground.
7	PB	Active-low push-button for hibernate wake-up.
8	ISNSN	Motor current sense, negative terminal.
9	ISNSP	Motor current sense, positive terminal.
10	SRC	Inverter source node, connect to ISNSP.
11	SRC	Inverter source node, connect to ISNSP.
12	OUTU	Phase U output.
13	VM	Main power supply (Motor Voltage).
14	VM	Main power supply (Motor Voltage).
15	OUTV	Phase V output.
16	SRC	Inverter source node, connect to ISNSP.
17	SRC	Inverter source node, connect to ISNSP.
18	OUTW	Phase W output.
19	VM	Main power supply (Motor Voltage).
20	VM	Main power supply (Motor Voltage). Connect a high value electrolytic capacitor in parallel with a 0.1µF ceramic capacitor from VM to VSS. This pin requires good capacitive bypass to VSS with a trace shorter than 10mm from this pin.
21	VCP	Charge Pump output. Connect a 10V/1µF ceramic capacitor between the VCP and VM pins.
22	CPH	Charge pump switch node. Connect a VM * 1.5V rated 0.1 µF flying capacitor between CPL and CPH.
23	CPL	Charge pump switch node. Connect a VM * 1.5V rated 0.1µF flying capacitor between CPL and CPH.
24-25	VSYS	Internally generated 5V power supply. Connect to a 10V/4.7µF ceramic capacitor from VSYS to VSS close to the device.
26	NC	Not connected. Leave floating.
27	NC	Not connected. Leave floating.
28	PA6	IO port PA6.
29	PA7	IO port PA7.
30	NC	Not connected. Leave floating.
31	PD1	IO port PD1.
32	PD0	IO port PD0.
33	PE0	IO port PE0.
34	PE1	IO port PE1.
35	PE2	IO port PE2.
36	PE3	IO port PE3.

Pin Number	Label	Description
37	VCCIO	Internally generated 3.3V power supply. For 3.3V IO, connect to a 10V/1µF ceramic capacitor from VCCIO to VCC close to the device. For 5V power supply, connect to VSYS.
38	VCORE	Internally generated digital 1.8V power supply. Connect a 6.3V/1µF ceramic capacitor from VCORE to VSS close to the device.
39	PC5/AD5	IO port PC5 or ADC channel AD5.
40	PC4/AD4	IO port PC4 or ADC channel AD4.

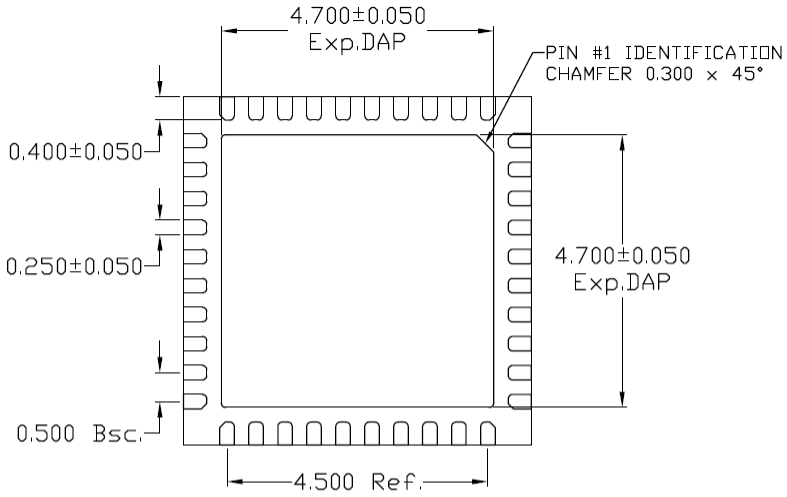
Mechanical Information

Package Marking and Dimensions

Marking: Part number – PAC5285



TOP VIEW

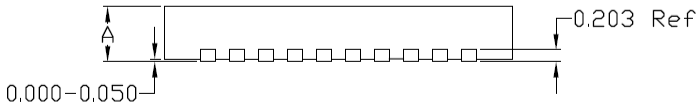


BOTTOM VIEW

NOTE:

1) TSLP AND SLP SHARE THE SAME EXPOSE OUTLINE BUT WITH DIFFERENT THICKNESS:

		TSLP	SLP
A	MAX.	0.800	0.900
	NOM.	0.750	0.850
	MIN.	0.700	0.800



SIDE VIEW

Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

REVISION HISTORY

Revision	Description
0.14	Corrected table and figure numbering; Updated LPDAC info in CAFE.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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