ACT88760

Advanced PMIC with 7 Bucks, 6 LDOs

BENEFITS and FEATURES

- **Wide input voltage range**
  - Vin = 2.7V to 5.5V
- **Complete integrated power solution**
  - 3x 4A DC/DC Step-Down (Buck) Regulators
  - 2x 3A DC/DC Step-Down (Buck) Regulators
  - 2x 2A DC/DC Step-Down (Buck) Regulators
  - Parallelable Bucks for higher current
  - 2x 800mA High PSRR LDOs
  - 4x 400mA General Purpose LDOs
  - LDO Load Switch Mode
- **Space Savings**
  - Fully integrated
  - High Fsw = 1.125MHz to 2.25MHz
  - Optimized for 0.47µH Inductor
  - Integrated sequencing
  - Integrated Constant Current LED Sinks
- **Easy system level design**
  - Configurable Sequencing
  - Multiple Wake up Triggers with GPIOs
  - Seamless Sequencing of External Supplies
  - 11 Programmable GPIOs
- **Highly configurable**
  - µP interface for status reporting and controllability
  - Programmable Reset and Power Good GPIO's
  - Flexible Sequencing Options
  - Multiple Sleep Modes
  - Integrated DVS
- **I^2C Interface – 1MHz**

APPLICATIONS

- Video processor and core supply voltage.
- Computer Vision.
- AR / VR Applications.
- Connected Home Applications.
- Portable devices.

GENERAL DESCRIPTION

The ACT88760 PMIC is an integrated ActiveCiPS™ power management integrated circuit. It powers a wide range of processors, including, video processors, FPGA's, wearables, peripherals, and microcontrollers. The ACT88760 is highly flexible and can be reconfigured via I^2C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc. ACT88760 is programmed at the factory with a default configuration. These settings can be optimized for a specific design through the I^2C interface. The ACT88760 is available in several default configuration. Contact the factory for specific default configurations.

The ACT88760 integrates seven high efficiency switching regulators, six linear regulators, and eleven GPIOs. Two LDOs can be configured as load switches. The eleven GPIOs pins are configurable and used for a variety of system functions.

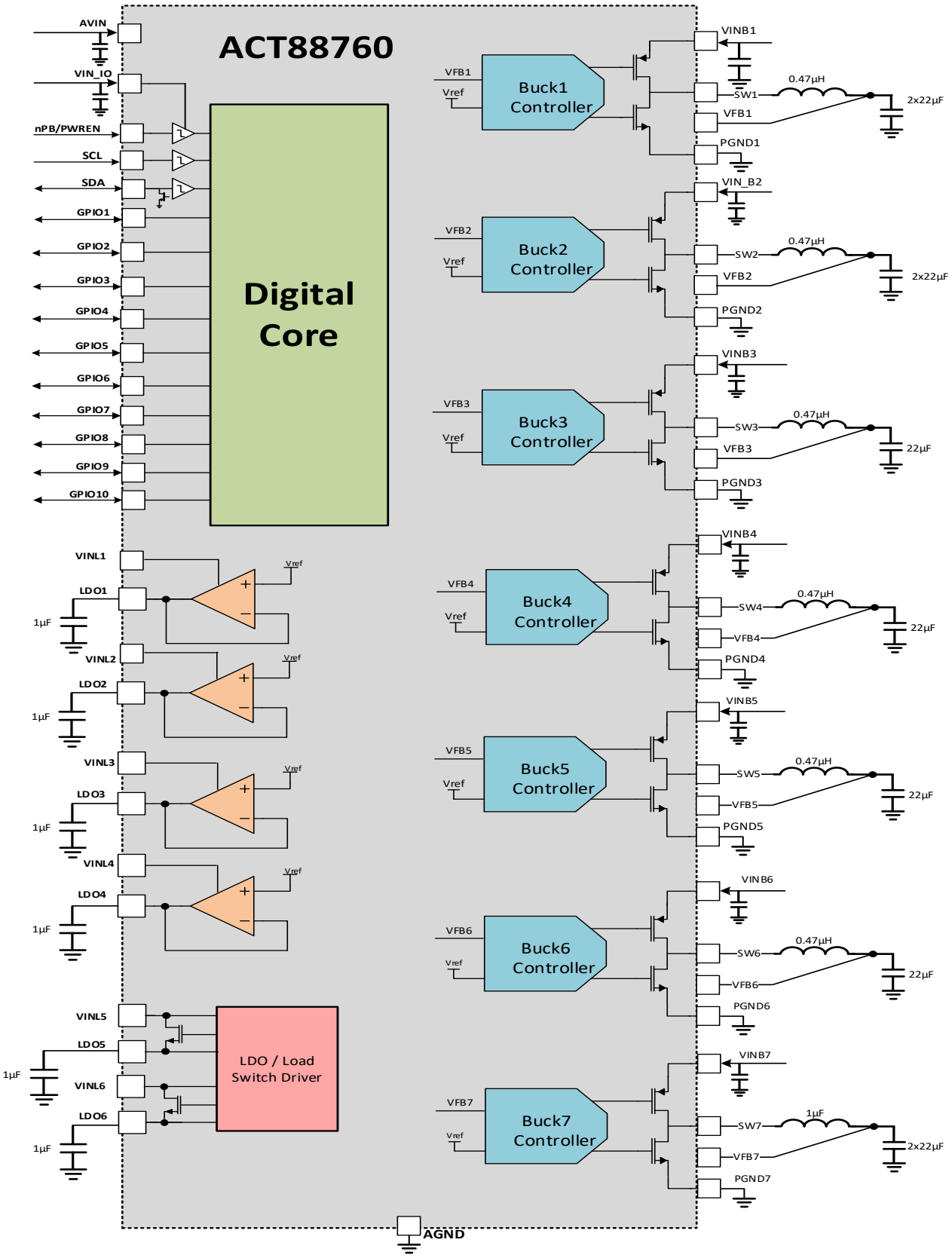
The ACT88760 is designed to work with a single lithium ion or lithium polymer batteries with an input voltage up to 5.5V. It works with input voltages as low as 2.6V.

The seven switching converters are peak current mode, fixed frequency DC-DC step down converters. Buck1/2 and Buck3/4 can be paralleled for 8A or 6A of output current. The high switching frequencies allow small inductors which reduce solution size and optimize load transient response. The converters are internally compensated for small ceramic output capacitors.

Two LDOs are high PSRR with > 70dB. The other for are general purpose LDOs. LDO5/6 can be configured as load switches with less than 25mΩ RDSON.

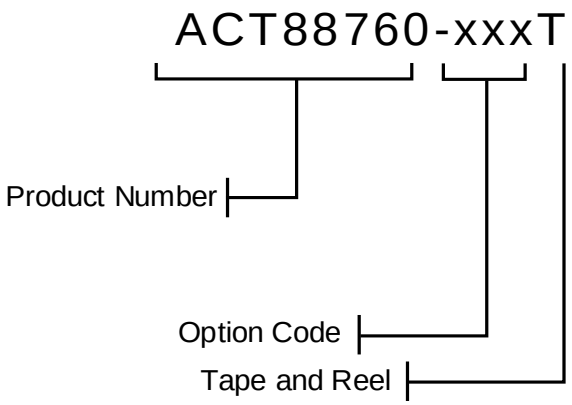
The ACT88760 PMIC is available in a 3.85mm x 3.85mm 81 ball WLCSP package.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	VIN	$V_{Buck1/2}$ Dual Phase		V_{Buck3}	V_{Buck4}	V_{Buck5}	V_{Buck6}	V_{Buck7}
ACT88760-101T		0.8V		0.8V	1.2V	1.1V	3.3V	0.8V
	V_{LDO1}	V_{LDO2}	V_{LDO3}	V_{LDO4}	V_{LDO5}	V_{LDO6}		
	0.8V	0.6V	1.8V	3.0V	LSW	LSW		
ACT88760-102.E2T	VIN	$V_{Buck1/2}$ Dual Phase		V_{Buck3}	V_{Buck4}	V_{Buck5}	V_{Buck6}	V_{Buck7}
	3.3-5V	0.8V		1.0V	1.8V	1.2V	3.3V	3.3V
	V_{LDO1}	V_{LDO2}	V_{LDO3}	V_{LDO4}	V_{LDO5}	V_{LDO6}		
	1.8V	1.2V	3.3V	3.3V	LSW	LSW		
ACT88760-104T	VIN	$V_{Buck1/2}$ Dual Phase		V_{Buck3}	V_{Buck4}	V_{Buck5}	V_{Buck6}	V_{Buck7}
	5V	0.8V		1.8V	1.1V	1.2V	1.2V	3.3V
	V_{LDO1}	V_{LDO2}	V_{LDO3}	V_{LDO4}	V_{LDO5}	V_{LDO6}		
	0.8V	1.8V	2.8V	2.8V	2.8V	1.8V		



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: “xxx” represents the CMI (Code Matrix Index) option. The CMI identifies the IC’s default register settings.

PIN CONFIGURATION – WLCSP - 81

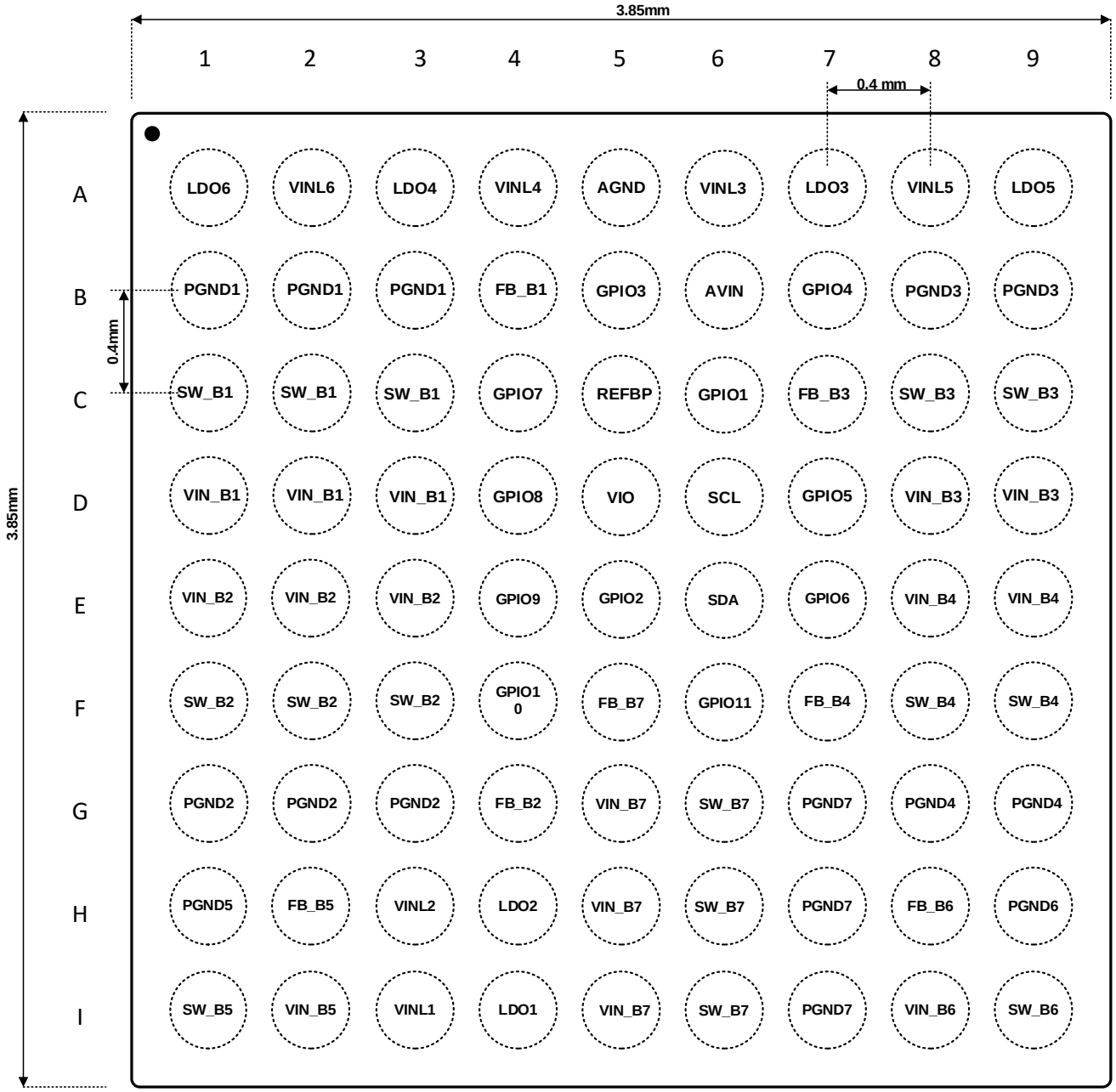


Figure 1: Pin Configuration – Top View (bumps down) – WLCSP- 81

PIN DESCRIPTIONS

Ball (CSP)	NAME	DESCRIPTION
A1	LDO6	Output of LDO6 / LSW6
A2	VINL6	Input to LDO6 / LSW6
A3	LDO4	Output of LDO4
A4	VINL4	Input to LDO4
A5	AGND	Analog Ground. Kelvin connect to the other ground pins on the IC.
A6	VINL3	Input to LDO3
A7	LDO3	Output of LDO3
A8	VINL5	Input to LDO5 / LSW5
A9	LDO5	Output of LDO5 / LSW5
B1, B2, B3	PGND1	Power GND for Buck1
B4	FB_B1	Feedback for Buck1. Connect to the Buck1 output capacitor.
B5	GPIO3	GPIO3
B6	AVIN	Analog Power Input Pin – Main Power Input to the PMIC.
B7	GPIO4	GPIO4 Pin
B8, B9	PGND3	Dedicated Power GND for Buck3
C1, C2, C3	SW_B1	Switch Pin for Buck1 (connect to inductor)
C4	GPIO7	GPIO7 Pin (Can Configure as PWREN, PWRON or nPB Input Pins)
C5	REFBYP	Reference Bypass Pin. Must connect a 100nF between REFBYP and AGND.
C6	GPIO1	GPIO1
C7	FB_B3	Feedback for Buck3. Connect to the Buck3 output capacitor.
C8, C9	SW_B3	Switch Pin for Buck1 (connect to inductor)
D1, D2, D3	VIN_B1	Dedicated Input Voltage to Buck1
D4	GPIO8	GPIO8
D5	VIO	Input / Output Voltage Reference Level for GPIOs
D6	SCL	I^2C Clock Pin
D7	GPIO5	GPIO5
D8, D9	VIN_B3	Dedicated Input Voltage to Buck3
E1, E2, E3	VIN_B2	Dedicated Input Voltage to Buck2
E4	GPIO9	GPIO9 Pin
E5	GPIO2	GPIO2 Pin
E6	SDA	I^2C Data Pin
E7	GPIO6	GPIO6 Pin (Can Configure as PWREN, PWRON or nPB Input Pins)
E8, E9	VIN_B4	Dedicated Input Voltage to Buck4
F1, F2, F3	SW_B2	Switch Pin for Buck2 (connect to inductor)
F4	GPIO10	GPIO10 Pin
F5	FB_B7	Feedback for Buck7. Connect to the Buck7 output capacitor.
F6	GPIO11	GPIO11 (Can Configure as PWREN or PWRON Input Pins)
F7	FB_B4	Feedback for Buck4. Connect to the Buck4 output capacitor.
F8, F9	SW_B4	Switch Pin for Buck4 (connect to inductor)
G1, G2, G3	PGND2	Dedicated Power GND for Buck2
G4	FB_B2	Feedback for Buck2. Connect to the Buck2 output capacitor.
G5, H5, I5	VIN_B7	Dedicated Input Voltage to Buck7

G6, H6, I6	SW_B7	Switch Pin for Buck7 (connect to inductor)
G7, H7, I7	PGND7	Dedicated Power GND for Buck7
G8, G9	PGND4	Dedicated Power GND for Buck4
H1	PGND5	Dedicated Power GND for Buck5
H2	FB_B5	Feedback for Buck5. Connect to the Buck5 output capacitor.
H3	VINL2	Input to LDO2
H4	LDO2	Output of LDO2
H8	FB_B6	Feedback for Buck6. Connect to the Buck6 output capacitor.
H9	PGND6	Dedicated Power GND for Buck6
I1	SW_B5	Switch Pin for Buck5 (connect to inductor)
I2	VIN_B5	Dedicated Input Voltage to Buck5
I3	VINL1	Dedicated Input Voltage to LDO1
I4	LDO1	Output of LDO1
I8	VIN_B6	Dedicated Input Voltage to Buck6
I9	SW_B6	Switch Pin for Buck6 (connect to inductor)

ABSOLUTE MAXIMUM RATINGS (NOTE1)

PARAMETER	VALUE	UNIT
All Pins to AGND unless stated otherwise below	-0.3 to 6.0	V
PGNDx, x = 1, 2, 3, 4, 5 , 6, 7 to AGND	-0.3 to + 0.3	V
AVIN to AGND	-0.3 to 6.0	V
VIO to AGND	-0.3 to Min (6.0 or AVIN + 0.3V)	V
REFBYP to AGND	-0.3 to 6.0	V
VIN_Bx, x = 1, 2, 3, 4, 5, 6, 7 to AGND (VIN_Bx = AVIN is required)	-0.3 to 6.0	V
FB_Bx, x = 1, 2, 3, 4, 5, 6, 7 to AGND	-0.3 to 6.0	V
SW_Bx, x = 1, 2, 3, 4, 5, 6, 7 to PGND	-1.0 to VIN_Bx + 1.0	V
VINLx, x = 1, 2, 3, 4, 5, 6 to AGND	-0.3 to 6.0	V
LDOx, x = 1, 2, 3, 4, 5, 6 to AGND	-0.3 to Min (6.0 or VINLx + 0.3V)	V
GPIOx, x = 1, 2, 3, 4, 6, 7, 8, 11 to AGND	-0.3 to Min (6.0 or AVIN + 0.3V)	V
GPIOx, x = 5, 9, 10 to AGND	-0.3 to 6.0V	V
nPB, PWREN, PWRON to AGND	-0.3 to Min (6.0 or AVIN + 0.3V)	V
SDA, SCL to AGND	-0.3 to Min (6.0 or AVIN + 0.3V)	V
Junction to Ambient Thermal Resistance (Note 2)	23	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
HBM ESD	2000	V
MSL Rating	1	

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.
Note2: Measured on Qorvo Evaluation Kit

RECOMMENDED OPERATING CONDITIONS

PARAMETER	VALUE	UNIT
All Pins to AGND unless stated otherwise below	0 to 5.5	V
AVIN to AGND	2.6 to 5.5	V
VIO to AGND	1.62V to 1.8V	V
VIN_Bx, x = 1, 2, 3, 4, 5, 6, 7 to AGND (VIN_Bx = AVIN is required)	2.6 to 5.5	V
VINLx, x = 1, 2 to AGND	1.08 to 5.5	V
VINLx, x = 3, 4, 5, 6, to AGND	2.6 to 5.5	V
GPIOx, x = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 to AGND	0 to 5.5	V
nPB, PWREN, PWRON to AGND	0 to 5.5	V
SDA, SCL to AGND	0 to 5.5	V
Operating Junction Temperature	-40 to 125	°C

Note1: AVIN must always be the highest input voltage to the IC.

DIGITAL I/O ELECTRICAL CHARACTERISTICS

(AVIN = 3.8V, VIO = 1.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO Pins					
VIO, GPIO Reference Voltage	Operating Voltage Range	1.62	1.8	AVIN	V
VIL, GPIOx, x = 1-8, 11 Input Low	GPIO power from AVIN. AVIN = 2.7V - 5.0V, Input mode			0.3	V
VIL, GPIOx, x = 1-8, 11 Input Low	GPIO power from VIO. VIO = 1.8V Input mode			0.26	V
VIH, GPIOx, x = 1-8, 11 Input High	GPIO power from AVIN. AVIN = 2.7V - 5.0V, Input mode	1.0			V
VIH, GPIOx, x = 1-8, 11 Input High	GPIO power from VIO. VIO = 1.8V Input mode	1.1			V
VIL, GPIOx, x = 9-10 Input Low	VIO = 1.8V Input mode			0.4	V
VIH GPIOx, x = 9-10 Input High	VIO = 1.8V Input mode	1.35			V
GPIOx, x = 1-11 Input Deglitch Time (falling)				30	µs
GPIOx, x = 1-11 Input Deglitch Time (rising)				30	µs
GPIOx, x = 1-8, 11 Delay time	GPIOxDly [1:0] = 00 GPIOxDly [1:0] = 01 GPIOxDly [1:0] = 10 GPIOxDly [1:0] = 11		0 1 2 4		ms
VOHPP, GPIOx, x = 1-8, 11 Output High (Not GPIO5)	AVIN = 5.0V, VIO = 1.8V, I_{OH} = 0.1mA, GPIO configured as push-pull output type.	1.6			V
VOHPP, GPIOx, x = 1-8, 11 Output High (Not GPIO5)	AVIN = 5.0V, VIO = 3.3V, I_{OH} = 0.1mA, GPIO configured as push-pull output type.	3.1			V
VOLPP, GPIOx, x = 1-8, 11 Output Low (Not GPIO5)	AVIN = 5.0V, VIO = 1.8V, I_{OL} = 0.1mA, GPIO configured as push-pull output type.			0.3	V
VOLPP, GPIOx, x = 1-8, 11 Output Low (Not GPIO5)	AVIN = 5.0V, VIO = 3.3V, I_{OL} = 0.1mA, GPIO configured as push-pull output type.			0.2	V
IOOD, GPIOx, x = 1-10 Open Drain Output High	VO = AVIN = 5.0V, VIO = 1.8 – 5.0V. Output Leakage Current, T_J = 25^{O}C			1	µA
VOLOD, GPIOx, x = 1-10 Open Drain Output Low	I_{OL} = 1mA, AVIN = 5.0V, VIO = 1.8 – 5.0V			0.2	V

LED Current Sink Programming (Analog GPIO Pin Only – See GPIO table for Analog GPIO Pin List)					
ISINK range	GPIOx_ILED [2:0]	0	3.0	6	mA
ISINK, LED Current Sink Settings	GPIOx_ILED = 000 (LED disabled)		0		mA
	GPIOx_ILED = 001		0.5		mA
	GPIOx_ILED = 010		1		mA
	GPIOx_ILED = 011		1.5		mA
	GPIOx_ILED = 100		2		mA
	GPIOx_ILED = 101		3		mA
	GPIOx_ILED = 110		4		mA
	GPIOx_ILED1, 2 = 111		6		mA
nPB – Push Button Pin Characteristics (Applicable when IC is configured for Push Button Function, nPB pin)					
nPB De-bounce Time	Push button presses shorter than this time are ignored.		50		ms
nPB Power Off Time (duration for successful turn-off)	EN_PWROFF = 1 EN_PWROFF TIME [1:0] = 00 EN_PWROFF TIME [1:0] = 01 EN_PWROFF TIME [1:0] = 10 EN_PWROFF TIME [1:0] = 11		1<t<4 4<t<8 8 12		s
nPB Power Cycle with Push Button	EN_PB_CYCLE = 1 PWRCYCTIME [1:0] = 00 PWRCYCTIME [1:0] = 01 PWRCYCTIME [1:0] = 10 PWRCYCTIME [1:0] = 11		1<t<4 4<t<8 8 12		s
PWREN – Power Enable Pin Characteristics (Applicable when IC is configured for Power Enable Function, PWREN pin)					
PWREN Input Low	GPIO power from AVIN. AVIN = 2.7V - 5.0V			0.3	V
PWREN Input High	GPIO power from AVIN. AVIN = 2.7V – 5.0V	1			V
PWREN Input Low	AVIN > 2.7V, VIO = 1.8V (VIO used for I/O)			0.26	V
PWREN Input High	AVIN > 2.7V, VIO = 1.8V (VIO used for I/O)	1.1			V
PWREN, EXT_PG Deglitch Time (falling)			1	30	µs
PWREN, EXT_PG Deglitch Time (rising)			1	30	µs

SYSTEM CONTROL ELECTRICAL CHARACTERISTICS

(VIN_Bx = 3.8V, VIO = 1.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVIN Operating Voltage Range		2.7		5.5	V
VIO Operating Voltage Range		1.62	1.8	AVIN	V
UVLO Threshold Falling (Note 1)	VIN_LVL=0	2.5	2.6	2.7	V
	VIN_LVL=1	3.35	3.50	3.65	V
UVLO Hysteresis (Note 1)	Rising threshold higher than falling threshold	50			mV
UV Deglitch Time	UV Detection deglitch time Falling – Enter UV condition Rising – Exit UV condition		 5 100		µs
OV Deglitch Time	OV Detection deglitch time Falling – Enter OV condition Rising – Exit OV condition		 5 200		µs
OV Rising Threshold Programmable Range	Programmable in 0.3V steps	3.7		5.8	V
OV Threshold Accuracy (Note 1)		-3		3	%
OV Hysteresis (Note 1)		80	200	320	mV
System Monitor (SYSMON) Rising Threshold Programmable Range	Programmable in 100mV steps	2.6		4.7	V
System Monitor (SYSMON) Accuracy		-3	SET POINT	3	%
System Monitor (SYMON) Hysteresis			100		mV
System Warning (SYSWARN) Rising Threshold. Programmable Range	Programmable in 100mV steps	2.6		4.7	V
System Warning (SYSWARN) Accuracy		-3	SET POINT	3	%
System Warning (SYSWARN) Hysteresis			100		mV
System Monitor Shutdown (Falling threshold)	SYSMON Falling threshold SETTING 0 SETTING 1	 2.5 3.35	 2.6 3.5	 2.7 3.65	V
Operating Supply Current (AVIN)	All Regulators Disabled		10	20	µA
Operating Supply Current (AVIN)	All Regulators Enabled but no load, All Buck LPM = 1. All LDO in LDO mode, charge pump disabled		700		µA
Operating Supply Current (AVIN)	All Buck Regulators Enabled but no load. ALL LDOs are off. ULPM = 1 for all buck regulators, PMIC in SLEEP/DPSLP mode. Fast clock off		230		µA
Operating Supply Current (AVIN)	Single Buck Regulator Enabled but no load. ALL LDOs are off. ULPM = 1 for all buck regulator, PMIC in SLEEP/DPSLP mode		170		µA

Operating Supply Current (AVIN)	Single LDO Regulator Enabled but no load. ALL BUCKs are off. PMIC in SLEEP/DPSLP mode. Fast clock off		65		µA
Thermal Warning Threshold	TWARN0 Register Bit, TWARN = 00	TWARN1-30	TWARN1-20	TWARN1-10	°C
	TWARN1 Register Bit, TWARN = 01	TWARN2-30	TWARN2-20	TWARN2-10	°C
	TWARN2 Register Bit, TWARN = 10	TWARN3-30	TWARN3-20	TWARN3-10	°C
	TWARN3 Register Bit, TWARN = 11	TSD-35	TSD-25	TSD-15	°C
TSD, Thermal Shutdown	Temperature rising	145	165	185	°C
Thermal Shutdown Hysteresis			30		°C
Startup Delay after initial AVIN	Time from AVIN > UVLO threshold to start of first regulator turning On. (0ms turn on delay setting) nSaveIqMstr=1		620	750	µs
	Time from AVIN > UVLO threshold to start of first regulator turning On. (0ms turn on delay setting) nSaveIqMstr=0		920	1150	µs
Transition time from Deep Sleep (DPSLP) State to Active State	Time from GPIOx pin transition to time when the first regulator turns ON with minimum turn on delay configuration.			1	ms
Transition time from Sleep State (SLEEP) to Active State	Time from I2C command to exit sleep mode to time when the first regulator starts to turn ON with minimum turn on delay configuration.			200	µs
Time to first power rail turn off when entering SLEEP / DPSLP	Time from turn-off event to when the first power rail turns off with minimum off delay.			200	µs
Startup Delay Programmable Range (ONDLY's MSB = 0) (Note that the ONDLY's MSB bit is a factory bit and cannot be changed by the user)	ONDLY= 0000 ONDLY= 0001 ONDLY= 0010 ONDLY= 0011 ONDLY= 0100 ONDLY= 0101 (Note 2) ONDLY= 0110 (Note 2) ONDLY= 0111 (Note 2)		0 500 1000 2000 4000 8000 16000 32000		µs
Startup Delay Programmable Range (ONDLY's MSB = 1 (Note that the ONDLY's MSB bit is a factory bit and cannot be changed by the user)	ONDLY= 1000 ONDLY= 1001 ONDLY= 1010 ONDLY= 1011 ONDLY= 1100 ONDLY= 1101 ONDLY= 1110 ONDLY= 1111		28.5 28.5 114 228 456 912 1824 3648		µs
Turn Off Delay Programmable Range (OFFDLY's MSB = 0) (Note that the OFFDLY's MSB bit is a factory bit and cannot be changed by the user)	OFFDLY = 0000 OFFDLY = 0001 OFFDLY = 0010 OFFDLY = 0011 OFFDLY = 0100 OFFDLY = 0101 OFFDLY = 0110 OFFDLY = 0111		0 500 1000 2000 4000 8000 16000 32000		µs

Turn Off Delay Programmable Range (OFFDLY's MSB = 1) (Note that the OFFDLY's MSB bit is a factory bit and cannot be changed by the user)	OFFDLY = 1000 OFFDLY = 1001 OFFDLY = 1010 OFFDLY = 1011 OFFDLY = 1100 OFFDLY = 1101 OFFDLY = 1110 OFFDLY = 1111		N/A 28.5 114 228 456 912 1824 3648		µs
nRESET Programmable Delay	nRST [1:0] = 000 nRST [1:0] = 001 nRST [1:0] = 010 nRST [1:0] = 011 nRST [1:0] = 100 nRST [1:0] = 101 nRST [1:0] = 110 nRST [1:0] = 111		5 10 20 40 0.5 1.0 2.5 100.0		ms

Note1: All Under-voltage Lockout, Overvoltage measurements are referenced between AVIN and AGND pin.

Note2: These ONDLY settings are not allowed when UV_FLTMSK = 0

BUCK1 & BUCK2 & BUCK7 ELECTRICAL CHARACTERISTICS, REGULATOR:

(VIN_B1/2 = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.6		AVIN	V
Output Voltage Range	Configurable in 5mV steps, RANGE = 0 Configurable in 25mV steps, RANGE = 1	0.5 0.5		1.135 3.675	V
V_{FB_BX}, Output Voltage Accuracy (Note2)	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode)	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous mode operation), Buck LPM = 1	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, 10mA (discontinuous mode operation) Buck ULPM = 1 (Ultra Low Power Mode Enabled)	-3%	V_{NOM}	3%	V
V_{FB_BX}, Output Voltage Accuracy	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode)	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous mode operation), Buck LPM = 1	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, 10mA (discontinuous mode operation) Buck ULPM = 1 (Ultra Low Power Mode Enabled)	-3.5%	V_{NOM}	3.5%	V
Maximum Operation Duty Cycle		99			%
Shutdown Current	Regulator Disabled, (Note2)		0.1	1	µA
	Regulator Disabled		0.1	4.5	uA
Standby Supply Current, Buck Low Power Mode Enabled	Regulator Enabled, No Load, Buck LPM = 1 & Fixed On-Time Disabled.		50		µA
Standby Supply Current, Buck Ultra Low Power Mode Enabled	Regulator Enabled, No Load, Buck ULPM = 1 & Fixed On-Time Enabled.		10		µA
Load Regulation	V_{OUT} = Default CMI Setting PWM mode.		0.05		%/A
Line Regulation	V_{IN} = 3.2V to 5.5V		0.05		%/V
P_{GOOD}, Power Good Threshold	V_{OUT} Rising	89	92	95	%
Power Good Hysteresis	V_{OUT} Falling		3		%
OV_{FLT}, Overvoltage Threshold	V_{OUT} Rising	109	112	115	%
Overvoltage Hysteresis	V_{OUT} Falling		3		%
Switching Frequency	FREQ_SET [1:0] = 0x FREQ_SET [1:0] = 10 FREQ_SET [1:0] = 11		2.25 1.5 1.125		MHz
T_{SS}, Soft-Start Period	10% to 90% ramp time of V_{OUT} SST=1 SST=0		 0.25 0.5		ms
ILIM, Internal High Side Peak Current Limit (Cycle-by-Cycle)	ILIMSET=0 ILIMSET=1		3.8 5.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At Default Set Point All Other Set Points	-20 -25		20 25	%
IWARN, Internal High Side Peak Current Limit Warning Threshold.	Warning threshold as % of ILIM threshold	-37	-22.5	-8	%

Low Side Peak Current Limit (Cycle-by-Cycle) (Note3)	ILIMSET=0 ILIMSET=1		4.2 5.5		A
Low Side On-Resistance, NMOS	I_{SW} = 1A, V_{IN} = 3.8V		12		mΩ
High Side On-Resistance, PMOS	I_{SW} = 1A, V_{IN} = 3.8V		30		mΩ
SW Leakage Current – NMOS	V_{IN} = 5V, V_{SW} = 5V (Note2)			1	μA
	V_{IN} = 5V, V_{SW} = 5V			1	μA
SW Leakage Current – PMOS	V_{IN} = 5V, V_{SW} = 0V (Note2)			1	μA
	V_{IN} = 5V, V_{SW} = 0V			4.5	μA
Output Pull Down Resistance	Enabled when regulator disabled, V_{OUT}=0.1V		3.6		Ω
Dynamic Voltage Scaling Rate	Vout_range = 0 + DVS_SET[] = 00 + DVS_SET[] = 01 + DVS_SET[] = 10 + DVS_SET[] = 11 Vout_range = 1 + DVS_SET[] = 00 + DVS_SET[] = 01 + DVS_SET[] = 10 + DVS_SET[] = 11		 11.2 5.6 2.8 1.4 56 28 14 7		mV/ μs
C_{OUTMIN}, Minimum Output Cap	Min output capacitance with voltage de-rating	20			μF

Note1: There are three balls for VIN, Buck1/2/7, and SW. Buck1/2/7 are rated for 6A average lifetime rating at 105 deg C junction.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection.

BUCK3 & BUCK4 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B3/4 = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.6		AVIN	V
Output Voltage Range	Configurable in 5mV steps, RANGE = 0 Configurable in 25mV steps, RANGE = 1	**0.5** 0.5		**1.135** 3.675	V
Output Voltage Accuracy (Note2)	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode)	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous mode operation), Buck LPM = 1	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, 10mA (discontinuous mode operation) Buck ULPM = 1 (Ultra Low Power Mode Enabled)	-3%	V_{NOM}	3%	V
VFB_BX, Output Voltage Accuracy	VOUT = 1.0V, IOUT = 2000mA (continuous PWM mode)	-1.5%	V_{NOM}	1.5%	V
	VOUT = 1.0V, IOUT = 10mA (discontinuous mode operation), Buck LPM = 1	-1.5%	V_{NOM}	1.5%	V
	VOUT = 1.0V, 10mA (discontinuous mode operation) Buck ULPM = 1 (Ultra Low Power Mode Enabled)	-3.5%	V_{NOM}	3.5%	V
Maximum Operation Duty Cycle		99			%
Shutdown Current	Regulator Disabled (Note2)		0.1	1	µA
	Regulator Disabled		0.1	3	uA
Standby Supply Current, Low Power Mode Enabled	Regulator Enabled, No Load, Buck LPM = 1		50		µA
Standby Supply Current, Buck Ultra Low Power Mode Enabled	Regulator Enabled, No Load, Buck ULPM = 1		10		µA
Load Regulation	VOUT = Default CMI Setting PWM mode.		0.05		%/A
Line Regulation	VIN = 3.2V to 5.5V		0.05		%/V
P_{GOOD}, Power Good Threshold	VOUT Rising,	89	92	95	%
Power Good Hysteresis	VOUT Falling		3		%
OVFLT, Overvoltage Threshold	VOUT Rising,	109	112	115	%
Overvoltage Hysteresis	VOUT Falling		3		%
Switching Frequency	FREQ_SET[1:0] = 0x FREQ_SET[1:0] = 10 FREQ_SET[1:0] = 11		2.25 1.5 1.125		MHz
TSS, Soft-Start Period	10% to 90% ramp time of VOUT SST=1 SST=0		 0.25 0.5		ms
ILIM, Internal High Side Peak Current Limit (Cycle-by-Cycle)	ILIMSET=0 ILIMSET=1		3.5 4.5		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At Default Set Point All Other Set Points	-20 -25		20 25	%

IWARN, Internal High Side Peak Current Limit Warning Threshold.	Warning threshold as % of ILIM threshold	-37	-22.5	-8	%
Low Side Peak Current Limit (Cycle-by-Cycle) (Note3)	ILIMSET=0 ILIMSET=1		3.7 4.7		A
Low Side On-Resistance, NMOS	I_{SW} = 1A, V_{IN} = 3.8V		25		mΩ
High Side On-Resistance, PMOS	I_{SW} = 1A, V_{IN} = 3.8V		50		mΩ
SW Leakage Current – NMOS	V_{IN} = 5V, V_{SW} = 5V (Note2)			1	μA
	V_{IN} = 5V, V_{SW} = 5V			1	uA
SW Leakage Current – PMOS	V_{IN} = 5V, V_{SW} = 0V (Note2)			1	μA
	V_{IN} = 5V, V_{SW} = 0V			3	uA
Output Pull Down Resistance	Enabled when regulator disabled, V_{OUT}=0.1V		3.6		Ω
Dynamic Voltage Scaling Rate	- Vout_range = 0 + DVS_SET[] = 00 + DVS_SET[] = 01 + DVS_SET[] = 10 + DVS_SET[] = 11 - Vout_range = 1 + DVS_SET[] = 00 + DVS_SET[] = 01 + DVS_SET[] = 10 + DVS_SET[] = 11		11.2 5.6 2.8 1.4 56 28 14 7		mV/ μs
C_{OUTMIN}, Minimum Output Cap	Min output capacitance with voltage de-rating	12			μF

Note1: There are two balls for VIN, Buck3/4, and SW. Buck3/4 are rated for 4A average lifetime rating at 105 deg C junction.
Note2: T_A = 25°C

Note3: LSILIM is used for current run-away protection.

BUCK5 & BUCK6 ELECTRICAL CHARACTERISTICS, REGULATORS:

(VIN_B5/6 = 3.8, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Voltage Range		2.6		AVIN	V
Output Voltage Range	Configurable in 25mV steps, RANGE = 0	0.5		3.675	V
V_{FB_BX}, Output Voltage Accuracy (Note2)	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode)	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous mode operation), Buck LPM = 1	-1%	V_{NOM}	1%	V
	V_{OUT} = 1.0V, 10mA (discontinuous mode operation) Buck ULPM = 1 (Ultra Low Power Mode Enabled)	-3%	V_{NOM}	3%	V
V_{FB_BX}, Output Voltage Accuracy	V_{OUT} = 1.0V, I_{OUT} = 2000mA (continuous PWM mode)	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, I_{OUT} = 10mA (discontinuous mode operation), Buck LPM = 1	-1.5%	V_{NOM}	1.5%	V
	V_{OUT} = 1.0V, 10mA (discontinuous mode operation) Buck ULPM = 1 (Ultra Low Power Mode Enabled)	-3.5%	V_{NOM}	3.5%	V
Maximum Operation Duty Cycle		99			%
Shutdown Current	Regulator Disabled (Note2)		0.1	1	µA
	Regulator Disabled		0.1	2.5	µA
Standby Supply Current, Low Power Mode Enabled	Regulator Enabled, No Load, Buck LPM = 1 & Fixed On-Time Disabled.		50		µA
Standby Supply Current, Ultra Low Power Mode Enabled	Regulator Enabled, No Load, Buck ULPM = 1 & Fixed On-Time Enabled.		10		µA
Load Regulation	V_{OUT} = Default CMI Setting PWM mode.		0.05		%/A
Line Regulation	V_{IN} = 3.2V to 5.5V		0.05		%/V
P_{GOOD}, Power Good Threshold	V_{OUT} Rising,	89	92	95	%
Power Good Hysteresis	V_{OUT} Falling		3		%
OVFLT, Overvoltage Threshold	V_{OUT} Rising,	109	112	115	%
Overvoltage Hysterisis	V_{OUT} Falling		3		%
Switching Frequency	FREQ_SET [1:0] = 0x FREQ_SET [1:0] = 10 FREQ_SET [1:0] = 11		2.25 1.5 1.125		MHz
T_{SS}, Soft-Start Period	10% to 90% ramp time of V_{OUT} SST=1 SST=0		 0.25 0.5		ms
ILIM, Internal High Side Peak Current Limit (Cycle-by-Cycle)	ILIMSET=0 ILIMSET=1		2.0 3.0		A
Internal High Side Peak Current Limit (Cycle-by-Cycle) Tolerance	At Default Set Point All Other Set Points	-20 -25		20 25	%
IWARN, Internal High Side Peak Current Limit Warning Threshold.	Warning threshold as % of ILIM threshold	-37	-22.5	-8	%

Low Side Peak Current Limit (Cycle-by-Cycle) (Note3)	ILIMSET=0 ILIMSET=1		2.6 3.8		A
Low Side On-Resistance, NMOS	I_{SW} = 0.5A, V_{IN} = 3.8V, T_J = 25°C		35		mΩ
High Side On-Resistance, PMOS	I_{SW} = 0.5A, V_{IN} = 3.8V, T_J = 25°C		80		mΩ
SW Leakage Current – NMOS	V_{IN} = 5V, V_{SW} = 5V, T_J = 25°C			1	μA
SW Leakage Current – PMOS	V_{IN} = 5V, V_{SW} = 0V, T_J = 25°C			1	μA
Output Pull Down Resistance	Enabled when regulator disabled, V_{OUT}=0.1V		6.7		Ω
Dynamic Voltage Scaling Rate	DVS_SET[] = 00 DVS_SET[] = 01 DVS_SET[] = 10 DVS_SET[] = 11		56 28 14 7		mV/ μs
C_{OUTMIN}, Minimum Output Cap	Min output capacitance with voltage de-rating	12			μF

Note1: There are two balls for VIN, Buck5/6, and SW. Buck5/6 are rated for 4A average lifetime rating at 105 deg C junction.
Note2: T_A = +25°C
Note3: LSILIM is used for current run-away protection

LDO1 & LDO2 ELECTRICAL CHARACTERISTICS

(VIN_LDO1/2 = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{INLx}, Operating Input Voltage		1.08		AVIN	V
V_{LDOx}, Output Voltage Range	Configurable in 12.5mV steps, RANGE = 0 Configurable in 12.5mV steps, RANGE = 1	0.5 1.2		1.2875 1.9875	V
Output Voltage Accuracy (Note1)	At Default CMI Output Setting	-1	V_{NOM}	1	%
Output Voltage Accuracy	At Default CMI Output Setting	-1.5	V_{NOM}	1.5	%
Line Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA			0.25	% / V
Load Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 500mA, VOUTSET = 0.8V		0.7		% / A
	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 500mA, VOUTSET = 0.6V		1.3		% / A
I_{Q1}, Supply Current	Regulator Enabled, VOUT > 1.0V, No Load, Charge pump enabled		190		µA
I_{Q1}, Supply Current	Regulator Enabled, VOUT < 1.0V, No Load, Charge pump disabled		52		µA
I_{SD}, Shut Down Current	Regulator Disabled			1	µA
I_{OUT} Maximum Output Current		800			mA
I_{LIM}, Output Current Limit		810	1100		mA
I_{SHORT}, Shorted Output Foldback Current			30		%
V_{DO}, Drop Out Voltage	ILIM = 0, I_{OUT} = 150mA, AVIN – V_{OUTL} > 2.0V			150	mV
	ILIM = 1, I_{OUT} = 300mA, AVIN – V_{OUTL} > 2.0V			300	mV
Soft-Start Period	SST_LDO=0, Default V_{OUTL}, 10% to 90%		320	500	µs
	SST_LDO=1, Default V_{OUTL}, 10% to 90%		160	250	µs
Power Good Threshold	VLDO Rising, % of V_{NOM}	89	92	95	%
Power Good Hysteresis	VLDO Falling, % of V_{NOM}		3		%
Overvoltage Fault Threshold	VLDO Rising, % of V_{NOM}	109	112	115	%
Overvoltage Fault Hysteresis	VLDO Falling, % of V_{NOM}		3		%
PSRR, Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 1.2V		75		dB
	f = 10kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 1.2V		65		dB
	f = 100kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 1.2V		55		dB
	f = 2000kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 1.2V		40		dB
V_{LTR}, Transient Response (Note1)	I_{OUT} 10mA to 250mA in 10us, V_{OUTL} = 1.8V, V_{INL} = 2.7V		1		%

Discharge Resistance	On when regulator disabled, VOUT = 0.1V DisChrgOptLx = 0 DisChrgOptLx = 1		 9.4 18.8		Ω
Output Capacitance Range	Effective capacitance including tolerance and voltage derating	1.5	2.2	10	µF

Note1: T_A = 25°C

LDO3, LDO4, LDO5, & LDO6 ELECTRICAL CHARACTERISTICS (LDO5 & LDO6 IN LSW MODE = 0)

(VIN_LDOx = 3.8V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{INLX}, Operating Input Voltage		1.62		AVIN	V
V_{LDOX}, Output Voltage Range	Configurable in 12.5mV steps, RANGE = 0 Configurable in 50mV steps, RANGE = 1	0.5 1.2		1.2875 3.6	V
Output Voltage Accuracy	At Default CMI Output Setting (Note1)	-1	V_{NOM}	1	%
Output Voltage Accuracy	At Default CMI Output Setting	-1.5	V_{NOM}	1.5	%
Line Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA			0.25	% / V
Load Regulation	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 500mA, VOUTSET = 1.8V		0.5		% / A
	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 500mA, VOUTSET = 3.0V		0.3		% / A
	V_{INLX} – V_{LDOX} > 400mV AVIN > 3.3V, I_{OUT} = 10mA to 500mA, VOUTSET = 4.15V		0.2		% / A
I_{Q1}, Supply Current	Regulator Enabled, Normal Mode, RANGE = 0		15	30	µA
I_{Q1}, Supply Current	Regulator Enabled, Normal Mode, RANGE = 1		20	40	µA
I_{SD}, LDO3 & LDO4 Shut Down Current	LDO3 & LDO4 Disabled			1	µA
I_{SD}, LDO3 & LDO4 Shut Down Current	LDO5 & LDO6 Disabled			3	µA
I_{SD}, LDO5 & LDO6 Shut Down Current	LDO5 & LDO6 Disabled (Note1)			1	µA
I_{OUT} Maximum Output Current	VIN_LDO1 = 1.62V to 5.5V, LDO1_ILIM=1	0.39			A
I_{LIM}, Output Current Limit	Range = 0, 2.7V < VINLX, LDO_ILIM = 1 LDO3 & LDO4 LDO5 & LDO6	380 340	500 500		mA
	Range = 0, 1.62V < VINLX < 2.7V		490		mA
I_{SHORT}, Shorted Output Foldback Current			30		%
V_{DO}, Drop Out Voltage	I_{OUT} = 150mA, V_{INL} > 2.7V LDO3 & LDO4 LDO5 & LDO6			150 160	mV
	I_{OUT} = 300mA, V_{INL} > 2.7V LDO3 & LDO4 LDO5 & LDO6			300 320	mV
Soft-Start Period	SST_LDO=0, Default V_{OUTL}, 10% to 90%		320	500	µs
	SST_LDO =1, Default V_{OUTL}, 10% to 90%		160	250	µs
Power Good Threshold	VLDO Rising, % of V_{NOM}	89	92	95	%
Power Good Hysteresis	VLDO Falling, % of V_{NOM}		3		%

Overvoltage Fault Threshold	VLDO Rising, % of V_{NOM}	109	112	115	%
Overvoltage Fault Hysteresis	VLDO Falling, % of V_{NOM}		3		%
PSRR, Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL1} = 2.7V, LPM=0		70		dB
	f = 10kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 2.7V, LPM=0		60		dB
	f = 100kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 2.7V, LPM=0		40		dB
	f = 2000kHz, I_{OUT} = 10mA, V_{OUTL} = 0.8V, V_{INL} = 2.7V, LPM=0		20		dB
V_{LTR}, Transient Response	I_{OUT} 10mA to 250mA in 10us, V_{OUTL} = 1.8V, V_{INL} = 2.7V		2.7		%
Discharge Resistance	On When regulator disabled, VOUT = 0.1V		18.8		Ω
Output Capacitance Range	Effective capacitance including tolerance and voltage derating	0.8	1.0	10	µF

Note1: T_A = 25°C

LSW5 & 6 ELECTRICAL CHARACTERISTICS (LDO5 & 6 CONFIGURED AS LOAD SWITCH)

(VIN_LDO = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INLX}, Operating Input Voltage	NLSW Mode PLSW Mode	0.5 1.62		3.3 AVIN	V
Output Current Capability	$V_{LDOX} < V_{INLX}$ – 0.25V, Note1	1.8			A
Current Limit Shutdown		2	3		A
Current Limit Shutdown deglitch time	Minimum time for current limit signal to be valid	10			µs
On Resistance (T_J = 25°C)	V_{INLX} = 1.2V, I_{LSX} = 250mA, AVIN=3.8V to 5.0V		12	25	mΩ
On Resistance	V_{INLX} = 1.2V, I_{LSX} = 250mA, AVIN=3.8V to 5.0V		12	25	mΩ
On Resistance (TJ = 25°C)	V_{INLX} = 3.3V, I_{LSX} = 250mA, AVIN=3.8V to 5.0V		22	35	mΩ
On Resistance	V_{INLX} = 3.3V, I_{LSX} = 250mA, AVIN=3.8V to 5.0V		22	38	mΩ
Soft start time	V_{INLSX} = 1.2V, AVIN = 3.8V, V_{OUTLSX} 10 – 90%		100		µs
Output Discharge Resistance	AVIN = 3.6V, V_{OUTLS1} = 0.1V.		25		Ω
I_{Q1}, Total Current Condition 1	AVIN=3.8V, V_{INL}=1.2V, I_{SYS}+I_{VINLS1} with no load current, Current Limit Enabled, LPM = 0		65	100	µA
I_{SD}, Disable Current	Load Switch Disabled, T_J = 25ºC			1	µA
	Load Switch Disabled			3	µA
PGOOD Rising Delay (Load Switch Mode Only, not LDO mode)			0		µs
PGOOD Falling Delay (Load Switch Mode Only, not LDO mode)			5		µs

Note 1: Full current capability only available if VINLx is in normal range and soft start is complete.

Note 2: Load Switch is not robust to faults on output when Current Limit is disabled.

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(AVIN = 3.3V, T_j = -40°C to +125°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C Protection	Register can be updated and I²C interface is only operational when VIN> VIN_UV. I²C communication is unavailable in RESET state.				
SCL, SDA Input Low	AVIN = 5.0V			0.6	V
SCL, SDA Input High	AVIN = 5.0V	1.08			V
SCL, SDA Input Low	VIO = 1.8V, Independent of AVIN			0.6	
SCL, SDA Input High	VIO = 1.8V, Independent of AVIN	1.08			
SDA Leakage Current	SDA= AVIN			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	See Note 1	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns

Note1: Comply to I²C timings for 1MHz operation - “Fast Mode Plus”.

Note2: No internal timeout for I²C operations.

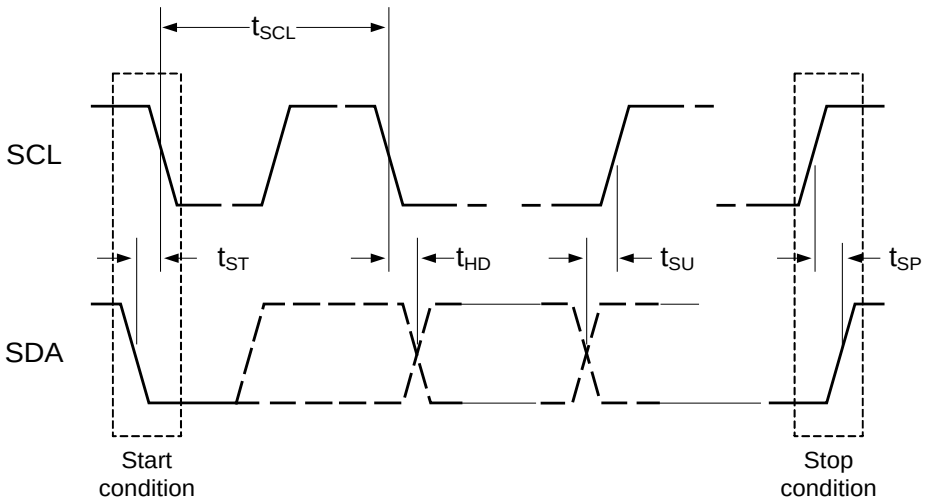


Figure 2: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT88760 is a highly integrated PMIC that is designed to be flexible and work with many system controllers and processors. It combines seven switching regulators and a combination of six linear regulators (LDO) and load switches (LSW) into a small form factor package. The switching regulators' high frequency minimizes the inductor size and reduces the overall solution size. The PMIC also integrates a master controller that provides startup sequencing to both the integrated power supplies and external regulators. The master controller manages startup and power off sequencing, timing, voltages, slew rates, sleep states (Low Power Modes or LPM), and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes.

The ACT88760 contains seven buck regulators. Three switching regulators can support 4A, two support 3A, and two support 2A of output current. The ACT88760 switching regulators are optimized to work with 0.47µH inductors. The regulators are designed for high efficiency and high current for microprocessor core supply voltages that are typically below 1.0V. The regulators are fully compensated internally and require just the inductor and output capacitor for operation. Buck1/2 can be operated in parallel to supply an 8A load, and Buck3/4 can be operated in parallel to supply a 6A load.

LDO1 and LDO2 are 800mA LDOs with high PSRR. LDO3 and LDO4 are general purpose LDOs that support up to 400mA of output current. LDO5 and LDO6 are specialized 400mA LDOs that can be configured as 1.2A low R_{ON} load switches.

The ACT88760 has eleven integrated GPIO pins. The GPIO pins are highly configurable and typically can be configured either as an input or output pin. The GPIO output drive, open drain or push-pull, and voltage level are configurable. Each GPIO can be configured for several different functions such as power good signals, interrupt requests, fault monitoring, sequencing, and controlling external regulators, LED drivers, Dynamic voltage scaling, Low Power Modes LPM entry and exit etc.

Many of the ACT88760s functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact sales@qorvo.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT88760 uses standard I²C commands. The ACT88760 always operates as a slave device and is addressed using a 7-bit slave address followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address.

The IC contains two sets of configurable I²C addresses. Buck7 and LDO1-6 operate from one I²C address and the rest of the regulators along with the master control (such as GPIOs, system monitoring, over temperature thresholds) have a different I²C address.

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pullup resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

Table 1: ACT88760 I²C Addresses

7-Bit Slave Address (Master, GPIOs, Buck1-6)		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h
7-Bit Slave Address (Buck7, LDO 1-6)		**8-Bit Write Address**	**8-Bit Read Address**
0x26h	010 0110b	0x4Ch	0x4Dh
0x28h	010 1000b	0x50h	0x51h
0x68h	110 1000b	0xD0h	0xD1h
0x6Ch	110 1100b	0xD8h	0xD9h

I2C Registers

The ACT88760 has an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, switching frequency, fault thresholds, fault masks, etc. These registers give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are

fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please contact Qorvo for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

The ACT88760 contains three independent state machines. Each state machine includes startup, low power modes, operating, and fault modes. One of the key features is the SLEEP and DPSLP states which are two configurable states that allow the user to optimize their system for low power modes. The output voltages can be adjusted or turned off to achieve the lowest system level power consumption. These states can be entered and exited with GPIOs and I^2C commands. Each of the three state machines is defined by the factory configured CMI and can not be changed by the user.

The ACT88760 can be configured to operate in either the PWREN, PWRON, or Push Button state machines. Only one mode of operation is allowed. Only one of the three modes of operation is allowed in any IC. The details of the PWREN mode, the PWRON mode of operation and the Push Button mode of operation can be seen in the separate state diagrams illustrated below. The state diagrams show the different states possible within each mode of operation.

PWREN State Machine

The PWREN state machine allows the IC to automatically startup when input power is applied. After the outputs are turned on per the programmed startup sequence, either an I^2C command or the PWREN pin can be used to move the IC to the DPSLP state.

PWRON State Machine

The PWRON state machine is very similar to PWREN with two main differences. The outputs do not automatically turn on unless the PWRON pin is pulled high. The PWRON pin is used as an enable input in the PWRON state machine. Also, the PWRON pin cannot be used to move the state machine into the DPSLP state, but another GPIO or an I^2C command can be used to enter and exit DPSLP mode.

Push Button State Machine

The Push Button state machine uses the nPB pin to control the outputs turn on and turn off. The nPB input pin is a unique, multi-function push button input. Refer to the nPB pin functionality for more details.

RESET State

In the RESET, or “cold” state, the ACT88760 is waiting for the input voltage on AVIN to be within a valid range defined by the AVIN_UV and AVIN_OV thresholds. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to the VROFF (PWRON configuration) or POWER SEQUENCE START (PWREN configuration) state when the input voltage is in the correct operating range.

The IC transitions from any other state to RESET if the input voltage drops below the UVLO threshold voltage. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states.

VROFF State

The VROFF state is only used in the PWRON configuration. The IC enters VROFF from RESET when VIN rises above UVLO or falls below OVLO. This is a stable state (not transitional state) where the IC waits for a GPIO input trigger to start sequencing on the output. When it receives this trigger, it transitions to the POWER SEQUENCE START state. The IC returns to this state to turn off all the regulators if the control input trigger is de-asserted at any time during operation. The IC then turns of all the regulators in proper order and waits in the VROFF state for the trigger to restart. If the input voltage drops below the UV threshold or goes over the OV threshold, the IC moves to the RESET state from this state. I^2C is active in this state.

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The outputs are enabled and are starting up in this state. Depending on the IC’s configuration and GPIO inputs, it immediately transitions to the POWER ON, SLEEP, or DPSLP states states when the regulators go into regulation.

The ACT88760 fault mask bits ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 at startup, so if one regulator has a fault at startup, all other regulators still turn on.

POWER ON (Active) State

The ACTIVE state is the normal operating state when the input voltage is within the allowable range, all outputs are turned on, and no faults are present. The IC only enters the ACTIVE State from the POWER SEQUENCE START State with the PWREN and nPB configurations. It enters from the VROFF State in the PWRON configuration.

SLEEP State

The SLEEP state is a configurable low power state. Based on the system's low power operational requirements, the user can configure the SLEEP state by defining which internal and external regulators are kept on or turned off during the SLEEP state. Buck1/2/7 can be programmed to be either ON or OFF. Buck3/4/5/6 can be programmed to be either ON, OFF, or regulate to one of its two VSETx register values. The VSETx registers effectively provide a dynamic voltage scaling (DVS) function. The LDOs can be programmed to be either ON or OFF. The regulators follow their programmed sequencing delay times when turning on or off as they exit or enter the SLEEP state.

The IC can enter SLEEP state via the I²C register SLEEP bit or by a GPIO input. Figure 3 shows how the NVM SLEEP_MODE factory bit sets the I²C and GPIO requirements to enter and exit the SLEEP state.

When the I²C bit SLEEP_MODE = 0, the IC enters SLEEP State with the logical AND of the I²C SLEEP bit and the GPIOs. If more than one GPIO is configured as a SLEEP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the SLEEP State, then only the SLEEP bit controls SLEEP State entry and exit. The IC immediately exits the SLEEP State when the SLEEP bit or a GPIO is de-asserted.

When the I²C bit SLEEP_MODE = 1, the IC enters SLEEP State with the logical OR of the I²C SLEEP bit and the GPIOs. If no GPIOs are configured to control the SLEEP state, then only the SLEEP bit controls the SLEEP State. The IC exits SLEEP State when both I²C and GPIO are de-asserted.

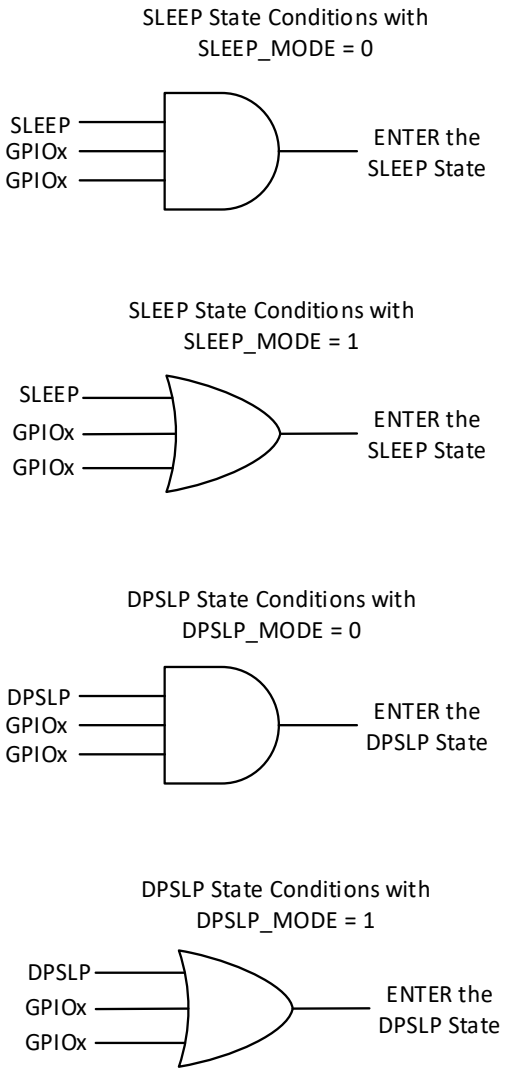


Figure 3. SLEEP and DPSLP State Truth Tables

DPSLP State

The DPSLP State is another low power operating mode for the operating system. It is intended to be used in a lower power configuration than the SLEEP state. It is identical to the SLEEP state, but DPSLP uses slightly different configurations to enter and exit this mode. Buck1/2/7 can be programmed to be either ON or OFF. Buck3/4/5/6 can be programmed to be ON, OFF, or regulate to one of its VSETx register voltages (the DVS function). The LDOs can be programmed to be either ON or OFF.

The DPSLP state programming or configuration can be different and independent from the SLEEP state programming. Each output can be programmed to have different functionality between the SLEEP and DPSLP states. The outputs follow their programmed sequencing delay times when turning on or off as they enter or

exit the DPSLP state. The IC can enter DPSLP state via the I²C register DPSLP bit or by a GPIOs input. Figure 3 shows how the NVM DPSLP factory bit sets the I²C and GPIO requirements to enter and exit the DPSLP state.

Any GPIO can be configured to control the DPSLP state without requiring an I²C command. This GPIO hardware function is called PWREN

The PWREN pin activates DPSLP State in one of two ways. The PWREN function can be configured to be either edge triggered or level triggered. The difference between these configurations only affects DPSLP Mode at power up.

Level triggered: If PWREN is low at startup, the IC enters DPSLP immediately after VIN goes above the UV threshold. Pulling PWREN high exits DPSLP.

Edge triggered: If PWREN is low at startup, the IC ignores PWREN and starts up normally. PWREN must be pulled high and then pulled low to generate a negative going edge to enter DPSLP Mode. If PWREN is high at startup, the IC starts up normally and then immediately enters DPSLP Mode when PWREN is pulled low.

Like the SLEEP state, an NVM factory bit DPSLP_MODE sets the logic OR or AND logic between I²C and GPIOs for entering and exiting the DPSLP state.

When DPSLP_MODE = 0, the IC enters DPSLP State with the logical AND of the I²C DPSLP bit and the GPIOs. If more than one GPIO is configured as a DPSLP State input, then all the GPIOs must be asserted. If no GPIOs are configured to control the DPSLP State, then only the DPSLP bit controls DPSLP State entry and exit. The IC immediately exits the DPSLP State when the DPSLP bit or a GPIO is de-asserted.

When the I²C bit DPSLP_MODE = 1, the IC enters DPSLP State with the logical OR of the I²C DPSLP bit and the GPIOs. If no GPIOs are configured to control the DPSLP state, then only the DPSLP bit controls the DPSLP State. The IC exits DPSLP State when both I²C and GPIO are de-asserted.

GPIOs can also be programmed to individually turn one or multiple outputs on and off. This on/off GPIO functionality in addition to the PWREN functionality. It provides a wide range of configurability for setting different DPSLP on/off patterns. Note that the GPIOs have four delay time options for both the rising and falling edges. These settings are 0ms, 1ms, 2ms, and 4ms.

For example, in SSD applications, the host can use these GPIOs and PWREN to enter different power save modes like PS3.5 and PS4.

In video applications, the GPIOs can be connected to sensor inputs to trigger the IC to exit the DPSLP mode when a sensor input triggers. The GPIO polarity can be programmed as active HIGH or LOW. GPIOs also have a programmable 0ms, 1ms, 2ms, and 4ms deglitch times.

Note that if an OV, UV, or THERMAL fault occurs when in DPSLP state, the PMIC transitions to the appropriate fault state and then transitions to the POWER ON state when the fault clears.

THERMAL State

In the THERMAL state, the IC has exceeded the thermal shutdown temperature. The IC shuts down all regulators and asserts the nRESET pin low to protect the IC in this condition. The THERMAL interrupt can be masked by setting register 0x01h bit 5 (TMSK) = 1. Note that thermal shutdown fault bit, TWARN, still provides the thermal status even if TMSK = 1. The THERMAL state can be disabled by setting register DIS_OTS in Factory level to 1.

OVUVFLT State

If one of the regulators exceed an OV or UV level at any time after the soft start ramp has completed, and the corresponding OV_FLTMSK or UV_FLTMSK volatile bits are set to low, the IC moves to UVOVFLT state. In this state, all regulators shutdown and the IC asserts the nRESET pin. After entering the OVUVFLT state, the IC stays there for 100ms and then goes back to the ACTIVE state. If the OV or UV condition still exists in the ACTIVE state, the IC returns to the OVUVFLT state. The cycle continues until the OV or UV fault is removed, or the input power is removed. The IC does not directly enter OVUVFLT in an overcurrent condition but does enter this state due to the resulting UV condition.

- PWREN Input Pin is the trigger for Power sequence & DPSLP.
- VIN UV and OV Levels are Configurable.
- If VIN < VIN_UV or VIN > VIN_OV, IC will enter RESET State.
- IC can enter RESET state if WD TIMER expires and a hard reset is performed by the WD TIMER.
- RESET state clears all registers and values are set to defaults or programmed NVM settings.
- DPSLP, SLEEP, DPSLP_EN & SLEEP_EN are Volatile Register bits (Volatile).

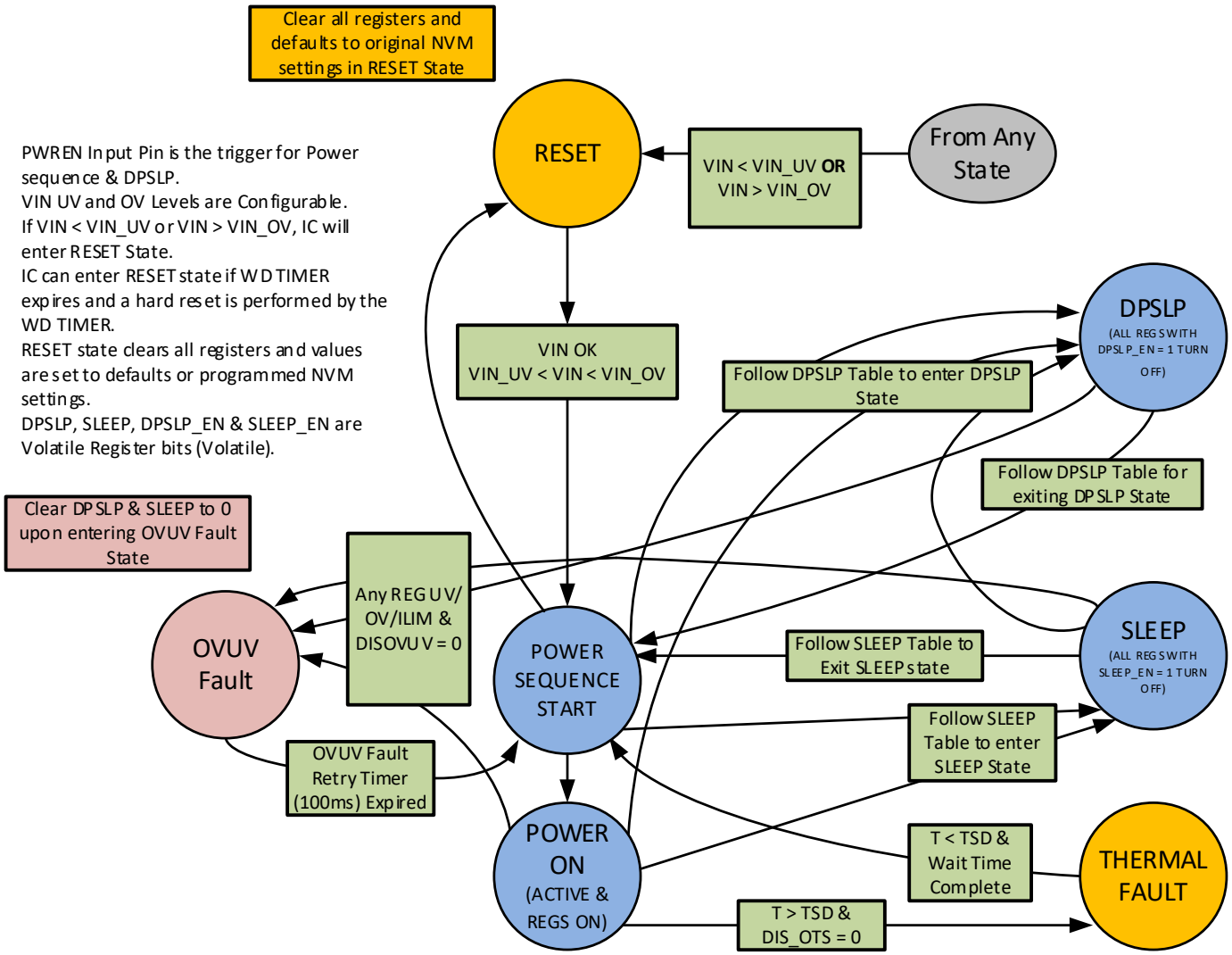


Figure 4: PWREN State Machine

- GPIO 6 can be used as the PWRON Input.
- VIN UV and OV Levels are Configurable.
- If VIN < VIN_UV or VIN > VIN_OV, IC will enter RESET State.
- IC can enter RESET state if WDTIMER expires and a hard reset is performed by the WD TIMER.
- RESET state clears all registers and values are set to defaults or programmed NVM settings.
- DPSLP, SLEEP, DPSLP_EN & SLEEP_EN are Volatile Register bits (Volatile).

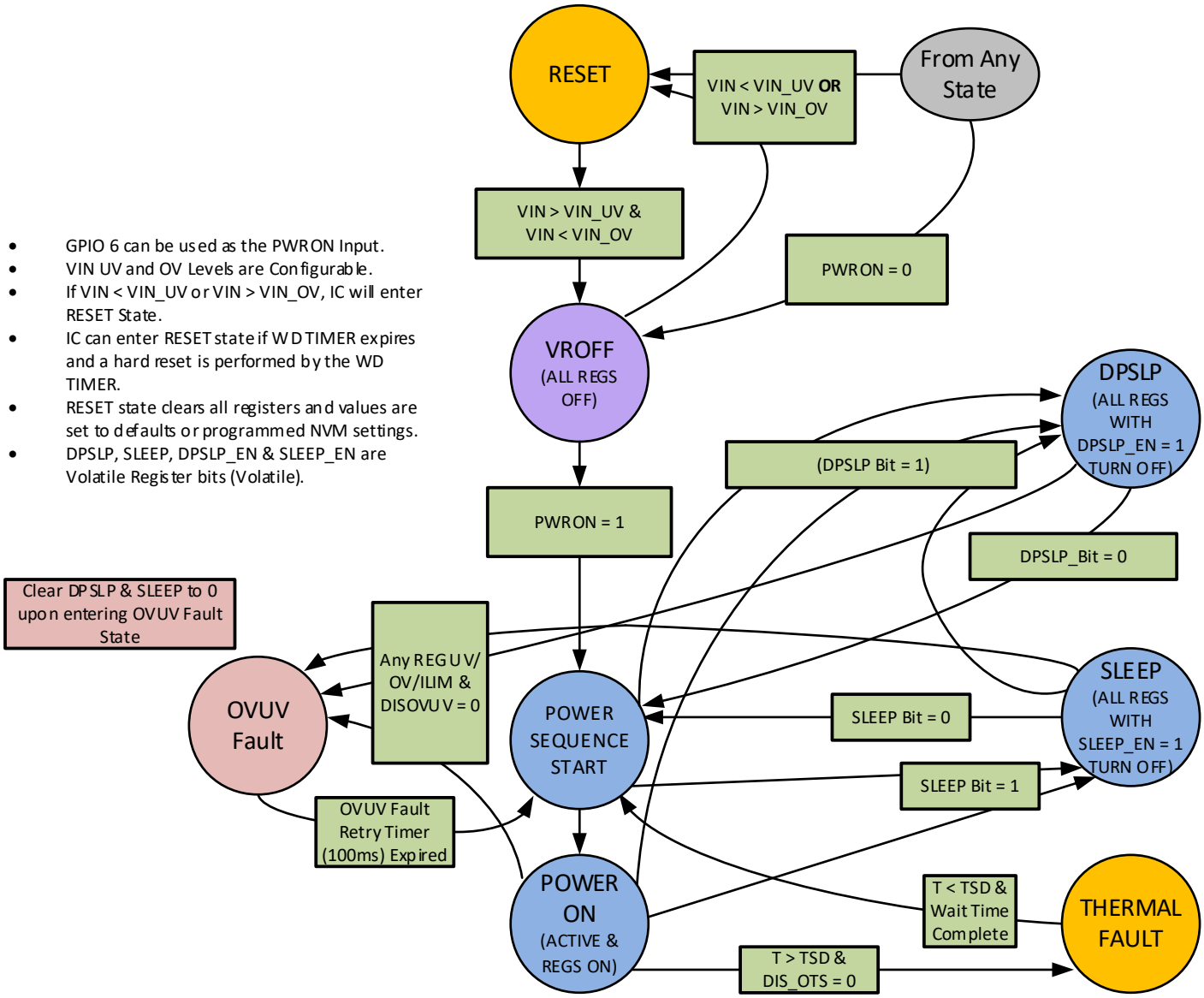


Figure 5: PWRON State Machine

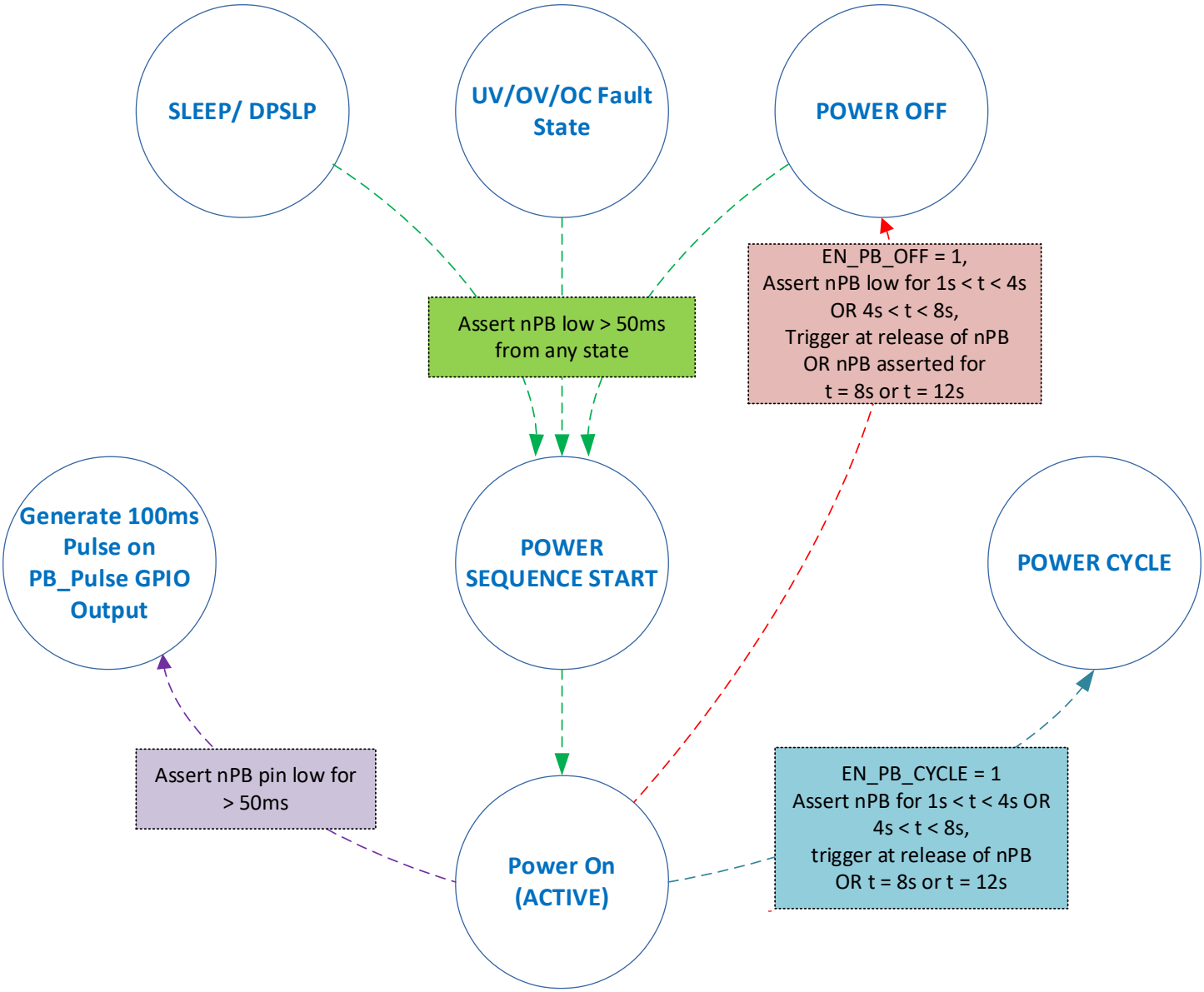


Figure 6: Push Button State Machine

PMIC OPERATION

The following sections describe the available ACT88760 functionality. Much of this functionality is configurable and can be mapped to different IC pins with a different CMI.

Sequencing

The ACT88760 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the 13 outputs has five basic sequencing parameters: input trigger, turn-on delay, turn-off delay, softstart time, and output voltage. Each of these parameters is controlled via the ICs internal registers. Contact Qorvo for custom sequencing configurations. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Turn on and Turn off Options. The ACT88760 provides several options for enabling the IC. These include automatic power up when input power is applied as well as power up with a digital input signal to a GPIO. The GPIO can be configured to latch the IC on with an input pulse or to be level triggered. Once powered on, the IC can be turned off with either the GPIO or an I²C command.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power OK (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to the IC's nPB/PWREN or GPIO pins. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with another external power supply or a control signal from the host. As an example, if the LDO1 input trigger is Buck1, LDO1 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can be changed with a custom CMI configuration. The GPIOs can be internally connected to a power supply's internal POK signal and used as an output to turn on external supplies in the overall sequencing scheme. A GPIO configured as the enable signal to turn on an external power supply is called the EXT_EN function.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ONDLY[2:0]. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between the input trigger for SLEEP or DPSLP Mode being asserted and when each output starts to turn off. Each output's turn-off delay is configured via its I²C bit OFFDLY[2:0]. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 10% to 90% to its programmed voltage. Each output's softstart time is configured separately via its I²C softstart bits. Softstart times can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Output Voltage. Each regulator's voltage is programmed via its I²C bits VSETx. The Buck1/2/7 have four VSETx registers, Buck3/4/5/6 have two VSETx registers, and the LDOs only have one. Note that in all conditions a buck's VSET0 register must be programmed to the highest voltage setting of all its VSETx registers. VSET1/2/3 settings do not have any restrictions other than they must all be lower than VSET0. A buck converter typically regulates to its VSET0 voltage in ACTIVE mode, but a GPIO can be configured to have the regulator regulate to one of its other voltages. The buck converter can be programmed to DVS to different VSETx values via a GPIO or by I²C. The LDOs do not support DVS.

All buck regulators can change between VSETx values on-the-fly (true DVS). If a system requires two different voltage options at startup, a GPIO can be programmed as a Voltage Select function. The Voltage Select input acts as an individual DVS control input to a buck converter. The Voltage Select input is typically tied high or low before output voltage is enabled and then does not change after the output is turned on. However, the ACT88760's does allow the Voltage Select to be changed on-the-fly for small output voltage changes that are less than 25%. For larger voltage changes, Qorvo recommends changing the voltage via I²C in small increments so the output voltage does not trigger an OV or UV condition.

Each output's Bx_VSET0 and Bx_VSET1 voltage can be changed via I²C after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. All bucks and LDO output voltages can be changed on-the-fly by writing a new value into their I²C registers. If a large voltage change is needed, change the output voltage by the multiple smaller steps. Qorvo recommends minimizing the step size change to prevent the IC from detecting an instantaneous over or under voltage condition due to fault thresholds being immediately changed, but output voltage taking time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) for all Buck regulators is available via the I²C interface. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. The IC operates in the ACTIVE state, but just regulates the outputs to a different voltage as specified by VSETx. For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Buck1/2/7 have four DVS settings. Buck3/4/5/6 have two DVS settings. Buck1/2/7 enter DVS differently from Buck3/4/5/6. Entering DVS by a GPIO pin, I²C, or when entering SLEEP/DPSLP are CMI dependent, so contact Qorvo for details.

Buck1/2/7 enter DVS by using GPIO pins (Table 2) or via I²C using the BKxDvsI2C[1:0] bits in register 0x44h. Note that Buck1/2/7 cannot automatically enter DVS when the IC enters SLEEP or DPSLP mode.

Buck3/4/5/6 enter DVS by using a single GPIO pin or via I²C using the DVS_FROM_I2C_DBx bits in register 0x02h. They can also be programmed to automatically enter DVS when the IC enters SLEEP or DPSLP mode.

Table 2: Buck1/2/7 DVS Control

Buckx_I2C_DVS_EN bit	Control Input - BKxDvs	Control Input - GPIOx, GPIOy	Buck1/2/7 Voltage Control Register
0	xx	00	VSET0
0	xx	01	VSET1
0	xx	10	VSET2
0	xx	11	VSET3
1	00	xx	VSET0
1	01	xx	VSET1
1	10	xx	VSET2
1	11	xx	VSET3

Input Voltage Monitoring (SYSMON)

The ACT88760 monitors the input voltage on the AVIN pin to ensure it is within specified limits for system level operation. The IC “wakes up” and allows I²C communication when AVIN rises above the UVLO threshold. The UVLO falling threshold can be set to either 2.7V or 3.6V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable. However, the outputs do not turn on until AVIN rises above the SYSMON threshold. The SYSMON rising threshold is programmable between 2.6V and 4.7V with 100mV steps. The SYSMON falling threshold has 100mV hysteresis.

If AVIN drops below the SYSMON falling threshold, the ACT88760 operates in one of two modes, which are programmable via a factory bit. This bit is not user adjustable. When SYSMON_SD=0 the outputs continue to operate normally while AVIN is still above UVLO. A GPIO can be programmed to output an active low SYSMON signal to indicate the SYSMON threshold has been crossed. The IC also asserts the nIRQ interrupt when AVIN < SYSMON. The nIRQ interrupt can be masked by an NVM register bit. The SYSMON signal output is a real-time signal. The IC also has a real-time status bit, SYSDAT in register 0x02h that follows the internal SYSMON signal. Note that the nIRQ output is latched until the SYSSTAT bit in register 0x00h is read via I²C.

When SYSMON_SD=1 the outputs immediately turn off when AVIN drops below the SYSMON falling threshold. Note that the outputs do not follow their programmed turn of delay. Figure 7 shows the SYSMON details when SYSMON_SD=0 (not programmed to turn off the outputs). If programmed to turn off the outputs, Figure 8 would show the outputs turning off when AVIN dropped below SYSMON.

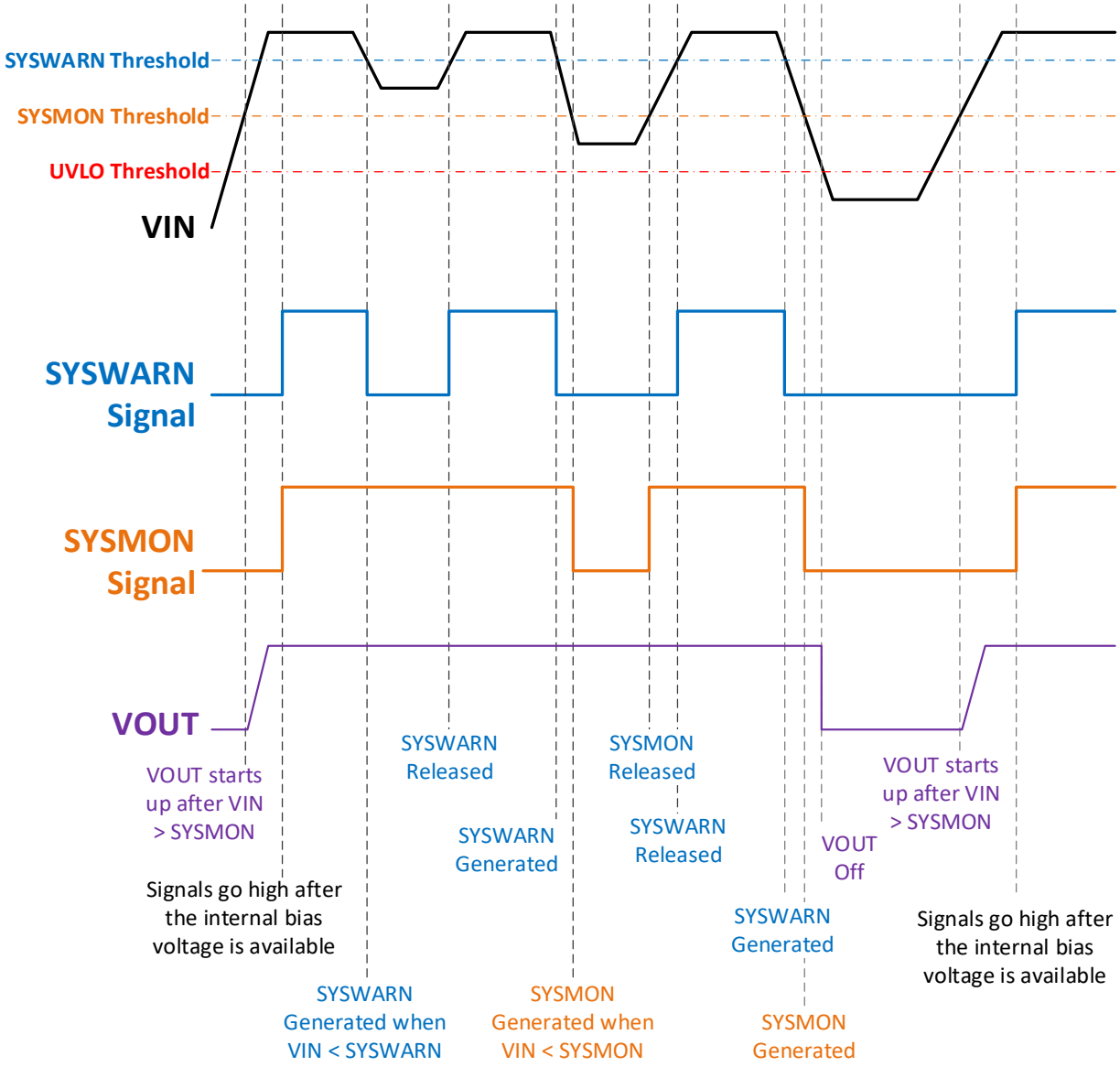


Figure 7: SYSMON and SYSWARN Signals when SYSMON_SD=0

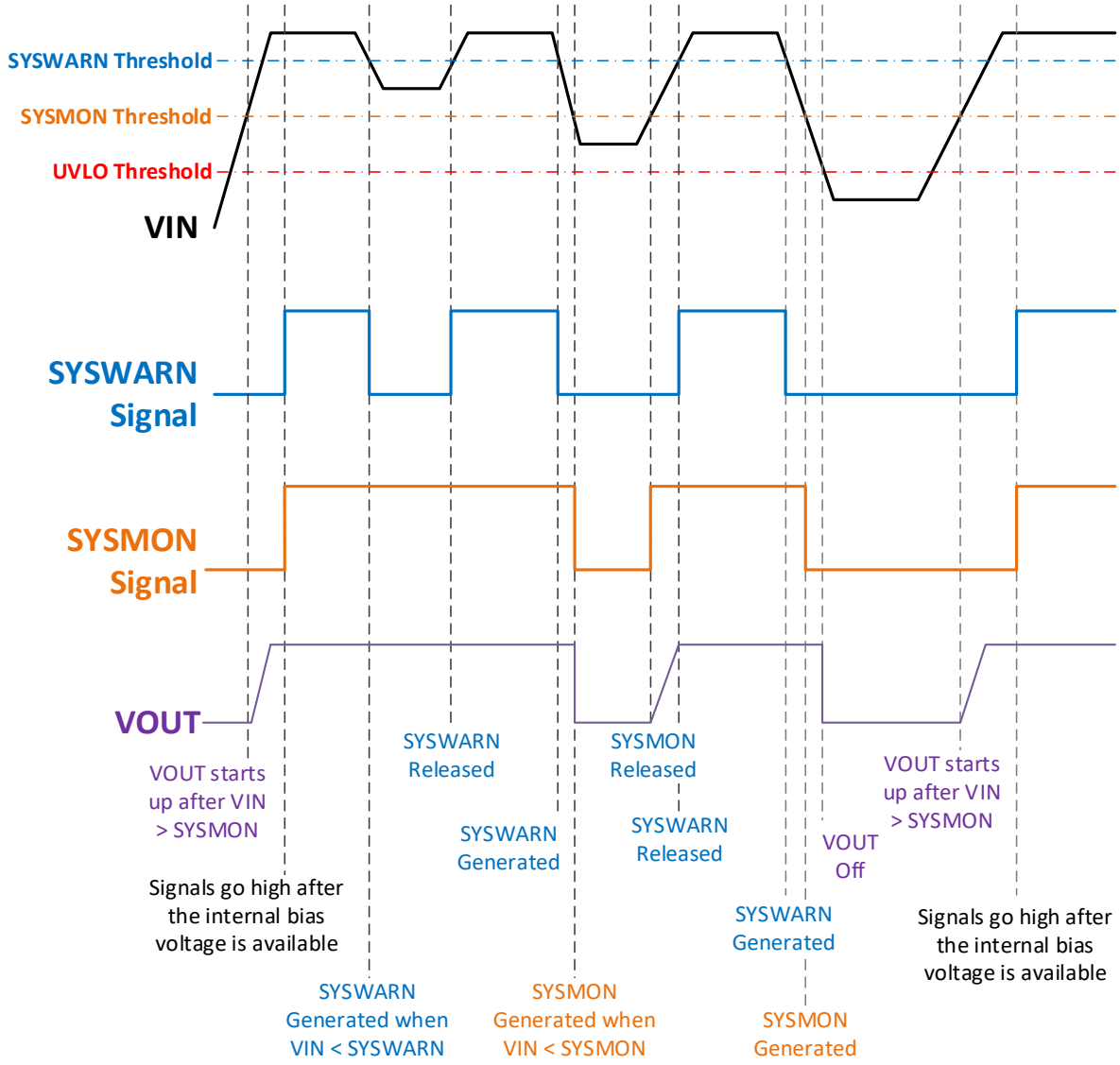


Figure 8: SYSMON and SYSWARN Signals when SYSMON_SD=1

Input Voltage Warning (SYSWARN)

The ACT88760 also has a second level of input voltage monitoring, SYSWARN. SYSWARN provides another level of low input voltage warning to the host. The rising threshold is programmable between 2.6V and 4.7V with 100mV steps by the SYSWARN bits. It should not be programmed lower than the SYSMON threshold. A GPIO can be programmed to output an active low SYSWARN signal so the host can use it for system control purposes. In the meantime, the IC asserts the nIRQ interrupt when VIN < SYSWARN. The nIRQ interrupt can be masked in the NVM register bit. The SYSWARN signal output is a real-time signal. The IC also has a real-time status bit, SYSWARN, that follows the internal SYSWARN signal. Note that the nIRQ output is latched until the SYSWARN bit in register 0x00h is read via I^2C.

Fault Protection

The ACT88760 contains several levels of fault protection, including the following:

- System Monitor (SYSMON) – UV and OV detection

- System Warning (SYSWARN) – UV and OV detection
- Output Overvoltage
- Output Undervoltage
- Output Current Limit and Short Circuit
- 4 Levels of Thermal Warning
- Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of whether that fault is masked. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only deasserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

Input Voltage UVLO

The ACT88760 monitors its input voltage at the AVIN pin for a UVLO condition. When the input voltage is below the UVLO threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I²C functionality is not enabled until AVIN goes above the UVLO threshold. When the input voltage goes above UVLO, the IC transitions to the Power Sequence Start or the VROFF state. The UVLO threshold can be set to either 2.7V or 3.6V by a factory programmable bit, VIN_LVL. VIN_LVL is not user adjustable.

Input Voltage OV

The ACT88760 monitors its input voltage at the AVIN pin for an OV condition. There are two overvoltage levels, POK_OV and VIN_OV. The first level is set by the POK_OV register, which is programmable between 3.5V and 5.6V in 300mV steps. When AVIN goes above the POK_OV threshold, an interrupt is generated on the nIRQ output, but all outputs stay on. If VIN_POK_OV_MASK = 0, the VIN_POK_OV register provides real-time status if. If it = 1, then VIN_POK_OV register is latched until read by I²C. The second level, VIN_OV, is programmable between 3.7V and 5.81V. VIN_OV should be programmed higher than POK_OV. When the input voltage is above the VIN_OV threshold, the IC is in the RESET State, all outputs are turned off, and nRESET is asserted low. I²C functionality is still enabled while AVIN is above the VIN_OV threshold. When the input voltage goes below the VIN_OV threshold, the IC transitions back to the Power Sequence Start State and starts up normally.

Output Under/Over Voltage

The ACT88760 monitors the output voltages for under voltage and over voltage conditions. The bucks' undervoltage bits are POK and the overvoltage bits are OV. The LDOs' undervoltage bits are PWRGOOD and the overvoltage bits are OV. The undervoltage thresholds are ~92% of the setpoint and the overvoltage thresholds are ~108% of the setpoint.

If the fault mask bits are set to 1, output UV/OV faults will not trigger interrupt, and the IC will not enter UV/OV shutdown.

If the fault mask bits (UV_FLTMSK and OV_FLTMSK) are set to 0, output UV/OV faults will trigger interrupt. And if the bit DisOvUvShdn in register 0x09h is set to 0, the IC will enter UV/OV shutdown. The IC can be configured to assert the nIRQ pin low when an output goes UV/OV to interrupt the system processor nIRQ remains asserted low until either the faulty regulator is turned off or it goes back into regulation, and the POK [-] bit (for Bucks) and PWRGOOD[-] bit (for LDOs) has been read via I²C to clear the interrupt. After the UV/OV condition is removed, an I²C read is required to clear the interrupt.

When it enters the UV/OV state, it shuts down all outputs for 100ms and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit.

POK[]/PWRGOOD[] are real-time status bits while OV[] is a latching status bit. POK[]/PWRGOOD[] are set to 1 when VOUT is over the POK/PWRGOOD levels and reset to 0 when VOUT is under POK/PWRGOOD level. Note that these bits are valid even if the UV/OV faults are masked. Masking an OV/UV fault just prevents the fault from being reported via the nIRQ pin. They still provide real-time UV/OV fault status via its fault flag, even if the fault is masked.

OV[] is set to 1 when VOUT is over the OV level and stays latched at 1 until readback by I²C OV[] and the output voltage has dropped below the OV threshold.

A UV/OV fault condition pulls the nRESET pin low. Note that nRESET output is configurable via CMI settings. Note that when the IC enters the UV/OV state due to an output UV/OV condition, all other outputs also turn off, even if their UV and OV faults are masked.

Output Current Limit

The ACT88760 incorporates a three-level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 77.5% of the Cycle-by-Cycle current limit threshold for greater than 17 continuous switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. This does not turn off that output or other outputs. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies off for 100ms and restarts. The third level is when the peak switch current reaches 122.5% of the Cycle-by-Cycle current limit threshold for five continuous switching cycles. This immediately shuts down the regulator and waits 14ms before restarting. The IC also has LS current limit for protection from current run-away. If the LS current limit is reached for nine continuous switching cycles, the IC may or may not turn off shutdown the regulator and wait 14ms before restarting depending on the specific CMI.

If the buck regulator current limit fault causes a UV fault which is reported back to the master controller (unmasked), the PMIC may shutdown for 100ms by entering the OV/UV state, and the behavior of the PMIC in this case is similar to the behavior in the OV/UV state.

For LDOs, the overcurrent thresholds are set by each LDO's Output Current Limit setting. When the output current reaches the Current Limit threshold, the LDO limits the output current. This reduces the output voltage, creating an undervoltage condition, causing all supplies to turn off for 100ms before restarting.

The overcurrent fault limits for each output are adjustable via I^2C. Overcurrent fault reporting can be masked via I^2C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT88760 monitors its internal die temperature and reports a warning via the nIRQ interrupt pin when the temperature rises above the Thermal Interrupt Warning Threshold of typically 125^{O}C. The ACT88760 contains four levels of thermal warning. The thermal warning status bits can be individually read from their corresponding register bits. One of the four thresholds can be mapped to generate an interrupt on the nIRQ pin.

The IC can report report a fault when the temperature rises above the Thermal Shutdown Temperature of typically 165^{O}C. An over-temperature condition moves the state machine to the THERMAL FAULT state and shuts down all outputs unless the fault is masked. Both the fault and the warning conditions can be masked via I^2C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin and prevents the PMIC from automatically reacting to the condition.

PWREN

PWREN is one of the three operating modes. See the State Machine section for more information. The PWREN functionality is controlled by the PWREN pin, which can only be assigned to GPIO6. The PWREN functionality is only available when the IC is configured for PWREN.

PWRON

PWRON is one of the three operating modes. See the State Machine section for more information. The PWRON functionality is controlled by the PWRON pin, which can only be assigned to GPIO6. The PWRON functionality is only available when the IC is configured for PWRON.

Push Button

Push Button is one of the three operating modes. See the State Machine section for more information. The Push Button functionality is controlled by the nPB pin, which can only be assigned to GPIO6. The Push Button functionality is only available when the IC is configured for Push Button.

The nPB provides multiple system level functions which depend on both the length of time that nPB is asserted low and the I^2C register settings. Table 12 summarizes the available options.

Power On: When nPB is pressed for longer than its 50ms debounce time, the IC always enters the ACTIVE state from any previous state, including SLEEP/DPSLP, UV/OV/OC protection, and POWER OFF states, and it resets the SLEEP/DPSLP bits to "0". If the press time is less than 50ms, the debounce timer resets and the IC stays in its current state.

Power Off: nPB can be used to turn the outputs off and put the IC into the POWER OFF state. Enable this functionality by setting EN_PWROFF=1. Asserting nPB for longer than the time defined by PB_OFF_TIMER turns the outputs off with the programmed turn off sequencing.

Note that the IC first enters the ACTIVE state after the 50ms debounce time. For the 1s<4s and 4s<8s settings, the IC turns off when nPB is deasserted. For the 8s and 12s settings, the IC turns the outputs off after nPB is pressed for either 8s or 12s. nPB does no need to be released to turn the outputs off. The four timing options are below:

00: 1s < Tpress < 4s, trigger at release

01: 4s < Tpress < 8s, trigger at release

10: Tpress = 8s, trigger at exactly 8s

11: Tpress = 12s, trigger at exactly 12s

For the 1s<4s and 4s<8s timing, if nPB is deasserted before the programmed time, the IC goes to the ACTIVE state after the 50ms debounce time and stays in the ACTIVE state. When the timing is programmed for 8s or 12s, the IC immediately turn the outputs off when nPB is held for longer than the 8s or 12 programmed time.

Power Cycle: The IC also contains a Power Cycle function. Enable this function by setting EN_PWRCYS=1. This function turns all outputs off with their programmed power down sequencing and then automatically restarts them with their startup sequencing.

Asserting nPB for longer than the time defined by PB_CYCLE_TIMER turns the outputs off with the programmed turn off sequencing. Note that the IC first enters the ACTIVE state after the 50ms debounce time. For the 1s<4s and 4s<8s setting, the IC starts the power cycle when nPB is deasserted. For the 8s and 12s settings, the IC starts the power cycle without the need to deassert nPB. The four timing options are below:

00: 1s < Tpress < 4s, trigger at release

01: 4s < Tpress < 8s, trigger at release

10: Tpress = 8s, trigger at exactly 8s

1: Tpress = 12s, trigger at exactly 12s

For the 1s<4s and 4s<8s timing, if nPB is deasserted before the programmed time the IC goes to the ACTIVE state after the 50ms debounce time and stays in the ACTIVE state. When the timing is programmed for 8s or 12s, the IC immediately starts the power sequence when nPB is held for longer than the 8s or 12 programmed time.

Note that the IC can perform both settings by programming PB_OFF_TIMER and PB_CYCLE_TIMER to different values. If both settings are programmed to the same setting PB_OFF takes priority.

Generate Pulse: One GPIO can be configured as a PB_Pulse function to generate a 100ms pulse when push-button is asserted for > 50ms.

Table 12 describes the available nPB functions.

nPB FUNCTION SUMMARY			
Function	**nPB Time**	**nPB TIME Configuration**	**nPB Configuration**
Power On	t > 50ms		EN_PWROFF = 0 EN_PWRCYS = 0
Generate Pulse on GPIO	t > 50ms		EN_PB_PULSE = 1
Power Off	1s < t < 4s	PB_OFF_TIMER = 00	EN_PWROFF = 1
	4s < t < 8s	PB_OFF_TIMER = 01	
	t = 8s	PB_OFF_TIMER = 10	
	t = 12s	PB_OFF_TIMER = 11	
Power Cycle	1s < t < 4s	PB_CYCLE_TIMER = 00	EN_PWRCYS = 1
	4s < t < 8s	PB_CYCLE_TIMER = 01	
	t = 8s	PB_CYCLE_TIMER = 10	
	t = 12s	PB_CYCLE_TIMER = 11	

Table 12: Summary of nPB Functions

nIRQ

The ACT88760 interrupt pin informs the host of any unmasked IC faults. In general, anything with a status change indicator can assert the nIRQ pin. The status changes can be masked by set the corresponding register bits. Note that all interrupts are masked by default and must be unmasked as needed. If interrupt bit is set, the fault must be read before it clears the interrupt bit. nIRQ stays asserted until both the fault clears and the interrupt bit is cleared by an I^2C read. If the fault remains after the I^2C read, the interrupt bit remains set.

The following status changes assert nIRQ:

- Input over-voltage, under-voltage
- Input voltage drops below SYSMON
- Input voltage drops below SYSWARN
- Thermal warning, thermal shutdown
- Buck operation faults
- Buck under-voltage shutdown
- Any buck regulator exceeding peak current limit for 17 cycles after soft start or a UV/OV condition.
- Any regulator exceeding current limit for more than 20µs after soft start or a UV/OV condition.
- Watch Dog timer expiring.
- GPIOs wake up mode high to low transition

nRESET

The nRESET pin is an open drain 5V compatible output used to issue the main reset to the system's CPU/controller. The output monitors the input voltage and valid regulator outputs to trigger a reset if the input voltage or

regulator output voltages are not valid. The nRESET delay time is controlled by the TRST_DLY control bits. The delay time is programmable from 5ms to 100ms. nRESET is essentially the same as a Power Good (PG) function but with a fixed delay after all the supply rails go into regulation.

The nRESET output signal is typically tied to all regulators outputs that are necessary for the system controller and I/Os to function properly. Each regulator has a register bit, RST, that determines if that regulator's POK signal is used as an input to the nRESET output signal. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs is not okay, the nRESET output will be asserted low.

The POK signal for any regulator can only be low when the regulator is enabled and the output is not regulating at normal levels. When a regulator's RSTI_by_POK bit = 0, the disabled regulator does not affect the nRESET signal even if its POK signal were configured to control the nRESET output. When a regulator's RSTI_by_POK bit = 1, then the disabled regulator does assert nRESET low. Note that RSTI_by_POK bit is a factory bit and can not be changed by a user.

In most applications, RSTI_by_POK bit = 0 so that a disabled regulator's POK bit stays high. The POK bits only go low (not ok) when the regulator is enabled but the output is not at the target regulation voltage. When a regulator is enabled, its internal POK immediately goes low until the output voltage goes above 90% of its programmed voltage.

Note that if a regulator's POK is configured as one of the input triggers to the nRESET function and that regulator turns off, the nRESET pin gets momentarily asserted low. The regulator could be turned off due to a GPIO input or going into SLEEP or DPSLP modes. When the regulator turn off due to a GPIO input or existing SLEEP or DPSLP modes, its POK output momentarily goes low, which also asserts nRESET low. If this is not desired, that individual regulator can be reconfigured to not be a RESET trigger input. Another option is to use the PGOOD function as a RESET to the system microprocessor.

PGOOD

The PGOOD output is similar to nRESET, but with some key differences. At power up the RESET function drives the PGOOD output, and PGOOD is asserted high at the same time that nRESET is deasserted high. The key difference is that PGOOD does not momentarily deassert low when a regulator enters or exits SLEEP or DPSLP states or when it is enabled or disabled with a GPIO. The regulator's POK signal does not force the PGOOD output low. The PGOOD output is only de-asserted when a fault occurs on any of the regulators after its soft start time. PGOOD is also deasserted low when all regulators on the IC are turned off or when the master UVLO (MUVLO) signal triggers. The master UVLO is a signal that is triggered when the input voltage (AVIN Input) is removed or when it drops below the UVLO threshold to reset the IC. A factory bit (ILIMFLT_PG_MASK[]) controls whether or not an output's current fault deasserts PGOOD. If ILIMFLT_PG_MASK = 0, any output's current limit fault deasserts PGOOD. If ILIMFLT_PG_MASK = 1, then current faults do not affect PGOOD.

EXT_EN

The EXT_EN is a GPIO output function that is used to enable an external power supply. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_EN output can be triggered by one of the regulator's POK signals. It can be programmed with a 0, 1, 2, or 4ms delay time.

EXT_PG

The EXT_PG is a GPIO input function that is used to indicate that an external power supply has turned on and its output voltage is in regulation. This function is useful for incorporating external power supplies into the overall system level startup sequencing. The EXT_PG output can be used as an input trigger to turn on one of the ACT88760 regulators.

POK

Any regulator's internal POK bit can be connected to a GPIO to provide an external POK signal. The POK function indicates that a regulator's output voltage is in regulation.

GPIO Wake up Mode

All GPIOs can be configured to force the IC into and out of DPSLP mode. Any number of GPIOs can be configured for this functionality. Please see the DPSLP State section for details. In addition, there are interrupt triggers that can be set up for GPIOs 1-11. The input status of the GPIOs can be read from the GPIOx_STAT bits, register 0x03h, 0x2Bh. Only the bits associated with the GPIOs that are configured as inputs are valid. The other bits are undefined and return a random value when read. For GPIOs configured as inputs, except PWRON, an input status change (1 to 0 or 0 to 1) can be configured to assert the nIRQ pin. For the PWRON input, a status change from 0 to 1 can be configured to assert the nIRQ pin, but a status change from 1 to 0 cannot. When the PWRON status changes from 1 to 0, all volatile and

non-volatile registers are reloaded to their default settings, which masks the status change. The status change function is masked by default and must be unmasked to enable the function, except GPIO8 which is unmasked by default.

LED Driver

GPIO9/10 can be configured as LED sinks. They sink a constant current that is programmed by the GPIOx_ILED bits. The programmable sink currents are 0, 0.5, 1, 1.5 ,2 ,3 ,4, and 6mA. 0mA effectively turns the LED sink off.

Discharge Function

The discharge function is used to quickly discharge a regulator's output voltage when the regulator is disabled. A GPIO can be configured as an open drain output and connected to the regulator's output through a resistor. When the output is turned off, all residual output capacitor energy is quickly discharged through the resistor to ground. The maximum discharge current is set by the discharge resistance and the output voltage. The discharge function is intended to quickly discharge the regulator's output voltage, but not to continuously sink current from an externally supplied voltage.

PIN DESCRIPTIONS

The ACT88760 input and output pins are configurable via CMI configurations. The following descriptions refer to the basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

AVIN Input Pin

AVIN is the PMIC bias power input. AVIN provides bias power to the master controller, the control circuits for all the regulators, the voltage monitors and fault comparators for UV, OV, SYSMON, Current limits etc. AVIN must be connected to the same voltage source as the VIN_Bx pins. It requires a 10 µF bypass capacitor to AGND.

VIO Pin

The VIO output pin is a regulated voltage that can be set to 1.2V, 1.8V, 2.4V, or 3.3V. This voltage is used internally to power all GPIOs, and it sets the GPIO output voltage level when they are configured as push-pull outputs. The output voltage is powered from an integrated low quiescent current LDO. VIO requires a 1 µF capacitor to AGND. It can supply up to 20 mA of current to external circuity.

PWREN / PWRON / nPB Pin

This pin can be configured to only one of these three different functions. The pin's configuration is set by the ICs specific CMI. See the State Machine section of the datasheet for details on how this pin functions in each of the three available states: PWREN, PWRON, and Push Button.

SCL, SDA

These are the IC's I^2C clock and data pins. They have standard I^2C functionality. The SCL and SDA pins have dedicated functionality and cannot be used for other functionality. If I^2C is not needed, these pins should be tied to either ground or to AVIN. See the System Control section for the IC's available slave addresses. SCL and SDA can be configured as true open drain, or as open drain with internal 5kΩ pullup resistors. The pullup voltage can be configured to either VIO or AVIN.

PGNDx

The PGNDx pins are the buck converter power ground pins. They connect directly to the buck converters' low side FETs. Bypass VIN_Bx to PGNDx and place the bypass capacitors close to the IC with minimal trace distance and maximum trace width to minimize parasitic inductance.

VIN_Bx

VIN_Bx pins are the dedicated input power pins to the buck converters. All VIN_Bx pins must be connected to the same voltage input. Each buck converter's VIN_Bx pin must be bypassed directly to its PGNDx pin on the top PCB layer with high-quality ceramic capacitors. Refer to the Step-down DC/DC Converters section for more details on the capacitor requirements.

SW_Bx

SW_Bx are the buck converter switch nodes. They connect directly to each buck's inductor on the top layer.

FB_Bx

These are the feedback pins for each buck converter. They should be kelvin connected to the buck output capacitors.

VINLx

These are the dedicated LDOx input power pins. Each VINLx pin can be connected to a different input voltage to optimize system level efficiency. Each pin must be bypassed directly to AGND on the top PCB layer with a 1µF or greater ceramic capacitor.

LDOx

These are the LDO output pins. Each LDO output must be bypassed to AGND with an appropriate capacitor. See the LDO section for capacitor requirements.

GPIOx

The ACT88760 has 11 GPIO pins. The GPIOs allow a variety of functions to be implemented. They can be used as inputs, open-drain outputs, or push-pull outputs. Their polarity can also be changed. These options allow implementation of a variety of system functions plus flexibility of functions tied to each pin. GPIOs can be configured for the following:

Reset output - nRESET

Power Good output - PG

Interrupt output – nIRQ

Power OK output – POK

External Regulator Enable output – EXT_EN

External Regulator Power Good input – EXT_PG

SLEEP Control input - SLEEP

DPSLP Control input - PWREN

Dynamic Voltage Scaling input – DVS

System Monitor output – SYSMON

System Warning output – SYSWARN

LED Driver input – LED

Not all GPIOs can support all available functions. The default GPIO configuration is defined by the IC's CMI. Some GPIOs can be reconfigured on-the-fly.

Some GPIOs that are configured as open drain outputs can be internally pulled up to either VIO or AVIN through an 86kΩ resistor. All GPIOs are 5V compliant and can be pulled to 5V regardless of their bias supply.

Table below shows each GPIO's available functionality

GPIO #	Assigned Function	VIN_POK (Warning)	ANY INTERNAL REG_POK	ANY INTERNAL REG_EN	SLEEP / DPSLP CONTRO	nRESET	Input Status (Interrupt)	nIRQ	LED Drive	EXTREG_EN (USE INTERNAL REG_EN / POK)	PULL DOWN (DISCHG EXT_REG)	Input Mode	Output Mode (CMOS)	Output Mode (Open Drain)	Invert (In/Out)	Delay	Internal Pull Up
GPIO1	nIRQ	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO2	nRESET	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO3	--	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO4	--	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO5	EXTEN1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	No	Yes	Yes	Yes	No
GPIO6	nPB/PWREN /PWRON	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO7	EXT PG1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO8	--	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
GPIO9	LED1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No	No
GPIO10	LED2	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No	No
GPIO11	--	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	100K (VIO)
SCL	SCL	No	No	No	No	No	No	No	No	No	No	Yes	No	No	No	No	10K(VIO)/5K(AVIN)
SDA	SDA	No	No	No	No	No	No	No	No	No	No	Yes	No	Yes	No	No	10K(VIO)/5K(AVIN)

Step-down DC/DC Converters

General Description

The ACT88760 contains seven fully integrated step-down converters.

All buck converters are fixed frequency, current mode controlled, synchronous PWM converters with peak efficiencies up to 96.5%. They switch at 1.125Mhz, 1.5MHz, or 2.25Mhz, and are internally compensated, requiring only three small external components (Cin, Cout, and L) for operation. They ship with default output voltages that can be modified via I^2C for systems that require advanced power management functions.

Buck1/2/7 support output currents up to 4A. Buck3/4 support output currents up to 3A. Buck5/6 support output currents up to 2A.

Buck1/2 can be configured to operate in parallel to provide a 2-phase operation with 8A (10A peak) currents. Buck3/4 can also be operated in parallel to provide 6A (8A peak). Buck5/6/7 do not support 2-phase operation.

Each buck converter has a dedicated input pin and power ground pin. Each buck converter must have a dedicated input capacitor that is optimally placed to minimize its power routing loops. Note that even though each buck converter has separate inputs, all buck converter inputs must be connected to the same voltage potential.

All ACT88760 buck regulators are highly configurable and can be quickly and easily reconfigured via I^2C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I^2C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Softstart ramp

DVS Slew rate control

Switching delay and phase control

Low power mode

Overcurrent thresholds

Refer to Qorvo's Register Map Definition application note for full details on I^2C functionality and programming ranges.

Operating Mode

By default, Buck1-7 operate in fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving Low Power Mode, LPM, at light loads to save power. LPM mode reduces conduction losses by preventing the inductor current from going negative. Each buck converter's LPM can be independently enabled or disabled via its DISLPM I^2C bit. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM. Operating in LPM saves power and reduces the quiescent current by working in a fixed on-time hysteretic mode and by disabling unneeded IC functions when the LPM mode skips pulses. Disabling LPM mode reduces light load efficiency but improves load transient response during a light to heavy load transition.

LPM minimizes quiescent current in between switching cycles. This reduces input current to approximately 50µA in LPM mode. Light load output voltage ripple increases from approximately 5mV to 10mV when in LPM mode. Light load voltage droop when going from light load to heavier loads is only increased by 2-3mV when in LPM mode. LPM allows the customer to test the IC in their use case and optimize the balance between power consumption, voltage ripple, and transient response in their system. Setting DISLPM = 0 enables LPM while setting DISLPM = 1 disables LPM.

Many customers will program the buck converters to LPM mode (LPM=1) after entering their system level low power mode and then program the IC back to PWM mode (LPM=0) just before leaving their system level low power mode. This provides the best load transient response while still taking advantage of reduced power dissipation in light load conditions. Note that when Vin=5V and operating in LPM mode, the output inductor should be 1µH.

ULPM (Ultra Low Power Mode)

The ACT88760 incorporates an ultra-low power mode, ULPM, that provides significant efficiency improvements at very light loads. This improvement can be as much as 8% with a 2mA load. ULPM mode reduces the buck converters quiescent current from ~50µA to ~10µA. The IC does this by turning off unused circuity and keeping only critical functionality enabled. Because ULPM is only used with extremely light loads, overcurrent protection is disabled to save quiescent current. ULPM mode helps systems like SSDs achieve very low power loss at extremely light loads, which is a requirement in their standby modes. ULPM mode regulates the output voltage between 99% to 101% of the setpoint. When the output voltage increases to 101%, the buck converter shuts down to save quiescent current until the output

voltage drops to 99%. It then turns back on and increases the output voltage to 101% again. ULPM mode should only be used when the load current is less than 15mA. With higher load currents, the output voltage drop can trigger UVLO before the converter can react. Using it with greater than 15mA results in much lower efficiencies than standard PWM or LPM mode operation.

If DVS mode is not needed when going into and out of DPSLP mode, program ULPM mode to automatically turn on when the IC enters SLEEP/DPSLP mode. If DVS is needed when going into and out of SLEEP/DPSLP mode, ULPM mode must be manually enabled after entering SLEEP/DPSLP mode and disabled before leaving SLEEP/DPSLP mode.

Synchronous Rectification

All bucks feature integrated synchronous rectifiers (or LS FETs) to maximize efficiency and minimize the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, all converters automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I^{2}C. Each CMI version requires a different set of command to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is enabled via the I^{2}C bit Dis_Pulldown.

Soft-Start

Each buck regulator contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the regulator is enabled, as well as after responding to a short circuit or other fault condition. Each regulator's softstart time is independently adjustable to either 250µs or 500µs via its I^{2}C SST register.

Output Voltage Setting

Buck1-7 regulate to the voltage defined by I^{2}C register VSET0 in normal operation. Buck1/2/7 have an additional three DVS settings defined by VSET1, VSET2, and VSET3. Buck3/4/5/6 have one additional DVS setting, VSET1.

Bucks 1/2/3/4/7 have an Output-High and an Output-Low programming range. Buck5/6 only have an Output-High range.

Mode	Range	Step	Bucks
Output-Low	0.5V-1.135V	5mV	1/2/3/4/7
Output-High	0.5V-3.675V	25mV	1/2/3/4/5/6/7

The Output-Low programming range is 0.5V to 1.135V in 5mV steps.

VBUCKx = 0.5V + VSETx * 0.005V

Where VSETx is the decimal equivalent of the value in I^{2}C VSETx register. The VSETx registers contain an unsigned 7-bit binary value.

The Output-High programming range is 0.5V to 3.675V in 25mV steps.

VBUCKx = 0.5V + VSETx * 0.025V

Where VSETx is the decimal equivalent of the value in I^{2}C VSETx register. The VSETx registers contain an unsigned 7-bit binary value. As an example, with Buck1 in the Output-Low setting and its VSET register contains 0111100b (60 decimal), the output voltage is 0.8V.

Qorvo recommends that a buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

100% Duty Cycle Operation

All buck regulators support 100% duty cycle operation. This allows operating conditions where the output voltage is very close to the input voltage. During 100% duty cycle operation, the P-ch high-side power MOSFET is turned on continuously, providing a direct connection from the input to the output (through the inductor), ensuring the lowest possible dropout voltage in battery powered applications.

As the input voltage drops, the converters have a transition between normal operation and 100% duty cycle mode. During normal switching, the minimum off-time is 40ns. If the operating conditions require < 40ns off-time, the switcher turns off for 40ns and then may skip the next switching cycle if the output voltage has not dropped to the point where the internal error amp commands another switching cycle. The output voltage is well regulated in this mode even though the IC skips pulses.

Dynamic Voltage Scaling

Each buck converter supports Dynamic Voltage Scaling (DVS). DVS allows the user to optimize the processor's energy to complete tasks by lowering the processor's

operating frequency and input voltage when lower performance is acceptable. In normal operation, all buck regulators regulate to the voltage programmed in the I²C register Bx_VSET0. During automatic DVS initiated by SLEEP / DPSLP states, Buck3/4/5/6 regulate to Bx_VSET1. A GPIO can also be configured to change an output's voltage between VSET0 and VSET1. Buck1/2/7 contain two additional VSETx registers, VSET2 and VSET3, to provide two additional DVS settings. When transitioning between VSETx settings, the control loop steps the output voltage through each step. The timing between steps is determined by the regulator's I²C SLEW bits. When going from a higher VSETx to a lower VSETx setting, the maximum output voltage transition rate may be limited by the rate determined by the output capacitance and the load current. When transitioning between a lower VSETx to a higher VSETx setting, the output transitions at the programmed slew rate.

VSET0 must always be programmed equal to or greater than the VSET1/2/3 setting. There is no programming limitations for VSET1/2/3 other than they must be programmed equal to or lower than VSET0.

During the transition between VSETx settings, the regulator's UV threshold is ignored to prevent incorrect fault triggering. The OV threshold is always relative to VSET0

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Qorvo recommends that a buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Optimizing Noise

Each ACT88760 buck converter contains several features available via I²C to further optimize functionality. The top P-MOSFET's turn-on timing can be shifted 100ns from the master clock edge via the PHASE I²C bit. It can also be aligned to the rising or falling clock edge via the PHASE I²C bit. The internal FET rise and fall times can be optimized to minimize switching noise at the cost of lower efficiency via the DRVADJ I²C bit.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set by the ILIM_SET I²C bits.

If the peak switch current reaches the programmed threshold (77.5% of ILIM_SET) for 17 consecutive switching cycles, the IC asserts that converter's ILIM_WARN bit and pulls nIRQ low. When DISOVUVShutdown = 0, a short circuit condition that results in a UV condition shuts down all supplies and then restarts the system in 100ms.

If the peak switch current exceeds 122.5% of the value set by ILIM_SET for five consecutive switching cycles, it only shuts down the regulator with the fault and then restarts it after 14ms.

If a buck converter reaches overcurrent or short circuit protection, the status is reported in that regulator's ILIM_REGx register. The contents of these registers are latched until read via I²C. Overcurrent and short circuit conditions can be masked via the I²C bit Bx_ILIM_FLTMSK. Note that ILIM_FLTMSK, ILIM_WARN_FLTMSK, OV_FLTMSK and UV_FLTMSK default to 1 (masked) at power up. The user can un-mask faults by setting these bits to 0 via I²C.

Compensation

The buck converters utilize a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. No compensation design is required; simply follow a few simple guidelines described below when choosing external components.

Minimum On-Time

The ACT88760 Buck regulators have a minimum on-time of 85ns. If the calculated on-time is less than the allowable minimum, then the user must configure the converter to switch at a lower frequency. The following equation calculates the on-time.

$$T_{ON} = \frac{V_{OUT}}{V_{IN} * F_{SW}}$$

Where V_{out} is the output voltage, V_{IN} is the input voltage, and F_{SW} is the switching frequency. The available switching frequencies are 1.125MHz, 1.5MHz, and 2.25MHz. The registers that set the switching frequency are in factory registers and are not user accessible.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. Note that even though each buck converter has separate input pins, all input pins

must be connected to the same voltage potential. 10µF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. Each buck's input capacitor must be placed as close to the IC as possible. The traces from VIN_Bx to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The ACT88760 buck converters are optimized for operation with 0.47µH to 1µH inductors. Choose an inductor with a low DC resistance and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, VIN is the input voltage, F_{SW} is the switching frequency, and L is the inductor value. Note that when Vin=5V and operating in LPM mode, the output inductor should be 1µH.

Output Capacitor Selection

The ACT88760 is designed to use small, low ESR, ceramic output capacitors. Buck1/2/7 typically require 2x 22µF output capacitors while Buck3/4/5/6 typically requires a 22µF capacitor. To ensure stability, the actual Buck1/2/7 capacitance must be greater than 20µF while Buck3/4/5/6 must be greater than 12µF. There is no maximum output capacitance limitation. Design for an output ripple voltage less than 1% of the output voltage. The following equation calculates the output voltage ripple as a function of output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

Unused Buck Outputs

If a buck converter is not used, connect the VIN_Bx pin to the other VIN_Bx pins. Connect FB_Bx to AGND. Leave SWx open. The input and output capacitors are not needed.

LDO CONVERTERS

General Description

ACT88760 features six low drop out linear regulators (LDO). The six LDOs are separated into three sets of two LDOs, each with unique features that allow system level optimization. Each LDO also has a dedicated input voltage pin for system optimization.

LDO1 and LDO2

LDO1/2 are 800mA, high PSRR LDOs. They are optimized for high-PSRR. LDO1/2 feature a low power mode (LPM) that reduces quiescent current at light load conditions. LPM is enabled when bit DISCP is set to 1. DISCP is a factory bit that cannot be changed by the user. When LPM is disabled (DISCP = 0), the LDOs can support 800mA, but the Iq increases to 190µA. Note that when VOUT is less than 1V, LPM can be enabled to reduce Iq and the LDO can still provide 800mA of output current. When LPM is enabled, Iq is reduced to 52µA.

LDO3 and LDO4

LDO3/4 are 300mA, general purpose LDOs. They are optimized for a low dropout voltage. LDO3/4 do not have a programmable LPM

LDO3 and LDO4 in Load Switch Mode (LSW)

LDO3/4 can be configured for a P-ch FET for load switch mode. The bits that control this are LDO3_MODE_SEL and LDO4_MODE_SEL, which are factory bits, control if the outputs act as LDOs or load switches.

LDO5 and LDO6

LDO5/6 are 250mA general purpose LDOs. They do not have a programmable LPM. LDO5/6 can also be configured as a 2A load switch (LSW)

LDO5 and LDO6 in Load Switch Mode (LSW)

LDO5/6 can be independently configured for LSW mode. This option is only accessible via factory I^2C bits and requires a custom CMI. When in load switch mode, LDO5/6 still retain overcurrent protection. However, overvoltage and undervoltage protection are disabled. In load switch mode, LDO5/6 have two operating options: NLSW and PLSW modes. In NLSW mode, the load switch is an n-ch FET. NLSW mode is used with an input voltage between 0.5V and 3.3V. Due to the lower n-ch FET Rdson, NLSW mode can operate with up to 2A of bypass current while maintaining a low voltage drop. In PLSW mode, the load switch is a p-ch FET. It can operate with an input voltage between 1.62V and AVIN. The PLSW current limit is set to 0.33A or 0.48A by the ILIM_SCL_LDO5/6 I^2C bit. NLSW and PLSW modes can only be fixed at the factory. NLSW mode has a fixed 100µs softstart time. PLSW mode relies on the current limit setting for softstart. The LDO5/6 POK are functional in Load Switch mode. The POK signal is asserted when the switch is enabled and is not in current limit. The LSW configuration bits are in factory memory and are not user accessible.

The gate driver circuit for the NMOS switch is ramped to control the soft start time for the output. For PLSW mode, softstart is controlled by limiting the starting current to the current limit setting. Once the switch is fully turned on, the driver circuit consumes lower current during operation.

Enable / Disable Control

When power is applied to the IC, all LDOs automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I^2C or GPIO. Each CMI version requires a different set of commands to disable a converter, so contact the factory for specific instructions if needed.

Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. Each LDO's discharge function is enabled via I^2C by setting the DIS_PULLDOWN_Lx = 0.

Soft-Start

Each LDO contains a softstart circuit that limits the rate of change of the output voltage, minimizing input inrush current and ensuring that the outputs power up monotonically. This circuitry is effective any time the LDO is enabled, as well as after responding to a short circuit or other fault condition. Each LDO's softstart time is adjustable to either 160µs or 320µs via its I^2C bits SST_LDOx. LDO1/5/6 softstart registers are user accessible. LDO2/3/4 softstart registers are in factory registers and are not user accessible.

Output Voltage Setting

Each LDO regulates to the voltage defined by their VSET I^2C register. The LDOs do not have additional VSETx registers.

Each LDO has an Output-High and an Output-Low programming range. The following tables define LDO voltage ranges and steps for each setting

Mode	Range	Step	LDO
Output-Low	0.5V-1.2875V	12.5mV	1/2/3/4/5/6
Output-High	1.2V-1.9875V	12.5mV	1/2

Output-High	1.0V-4.15V	50mV	3/4/5/6

For all LDOs, the Output-Low programming range is 0.5V to 1.2875V in 12.5mV steps.

VLDOx = 0.5V + VSET * 0.0125V

Where VSET is the decimal equivalent of the value in I^2C VSET register. The VSET registers contain an unsigned 6-bit binary value.

For LDO1/2, the Output-High programming range is 1.2V to 1.9875V in 12.5mV steps.

VLDOx = 1.2V + VSET * 0.0125V

For LDO3/4/5/6, the Output-High programming range is 1.0V to 4.15V in 50mV steps.

VLDOx = 1.0V + VSET * 0.05V

As an example, with LDO1 in the Output-Low setting and its VSET register contains 111000b (56 decimal), the output voltage is 1.2V.

Qorvo recommends that an LDO's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Overcurrent and Short Circuit Protection

Each LDO provides overcurrent and short circuit protection. The overcurrent threshold is set by the LDOx_ILIM I^2C bits. In both an overload and a short circuit condition, the LDO limits the output current which causes the output voltage to drop. This can result in an undervoltage fault in addition to the current limit fault. If an LDO reaches current limit protection, the status is reported in the ILIM_REG[x] I^2C registers. The contents of these registers are latched until read via I2C. When the current limiting results in a drop-in output voltage that triggers an undervoltage condition, the IC shuts down all power supplies, asserts nIRQ low, and enters the UVLOFLT state. The IC restarts in 100ms and starts up with default sequencing. Overcurrent and short circuit conditions can be masked via the I^2C bits LDOx_ILIM_FLTMSK and LDOx_UV_FLTMSK.

The LDO contains current-limit circuitry featuring a current-limit fold-back function. During normal operation and moderate overload conditions, the regulator can support more than its rated output current. During sustained extreme overload conditions when current limit is triggered however, the current limit is reduced by approximately 30%, reducing power dissipation within the IC. The current limit has a fold back behavior in this regard where the triggering condition is higher than the regulated current value during overload.

Input Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic input capacitor. A 1uF is typically suitable, but this value can be increased without limit. Connect the input capacitor between the LDO input pin and AGND. The input capacitor should be a X5R, X7R, or similar dielectric.

Output Capacitor Selection

Each LDO requires a high quality, low-ESR, ceramic output capacitor.

LDO1/2 output capacitance is typically 2.2uF with a 1.5uF minimum capacitance value and a 10uF maximum capacitance value.

LDO3/4/5/6 output capacitance is typically 1uF with a 0.8uF minimum capacitance value and a 10uF maximum capacitance value.

Connect the output capacitor between the LDO output pin and AGND. A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The output capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics are not recommended due to their wide variation in capacitance over temperature and voltage ranges.

Unused LDO Outputs

If an LDO is not used, connect the VINLx pin to either GND or AVIN. Connect the LDOx output to AGND. The input and output capacitors are not needed.

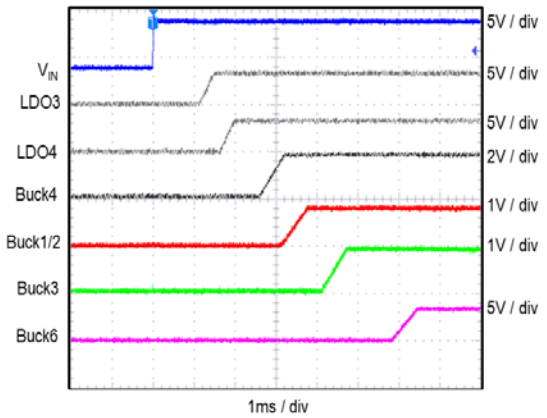
PC Board Layout Guidance

Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT88760 PCB. Refer to the Qorvo ACT88760 Evaluation Kits for layout examples

1. Place the buck input capacitors as close as possible to the IC. Connect the capacitors directly to the corresponding VIN_Bx input pin and PGNDx power ground pin on the same PCB layer as the IC. Avoid using vias.
2. Minimize the switch node trace length between each SW_Bx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. Place the LDO input capacitors close to their input pins. Connect their ground pins into the ground plane that connects the IC's PGNDx pins.
4. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
5. Connect the PGNDx ground pins and the AGND ground pin directly to the PGND under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
6. Connect the VIN input capacitor to the AGND ground pin.
7. Remember that all open drain outputs need pullup resistors.
8. Connect the PGND directly to the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions and are relatively insensitive to layout considerations.

TYPICAL OPERATING CHARACTERISTICS

CMI 102
Startup Sequencing



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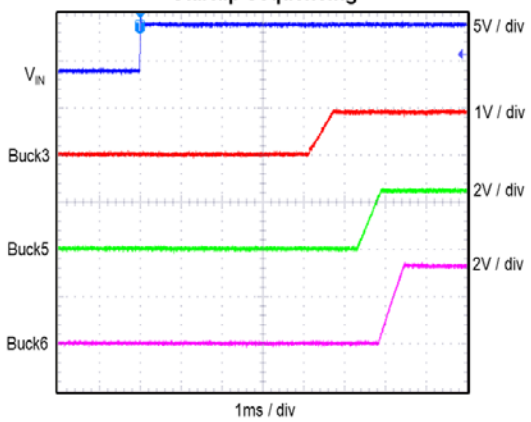
Startup Sequencing



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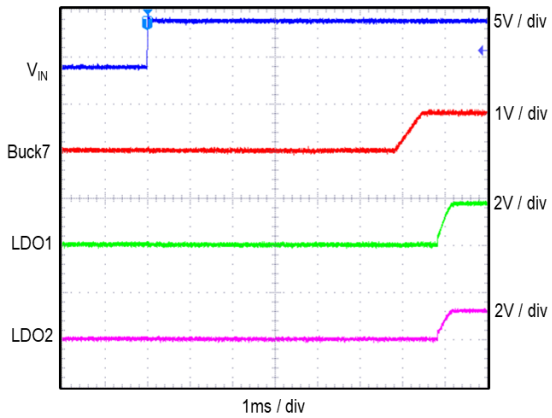

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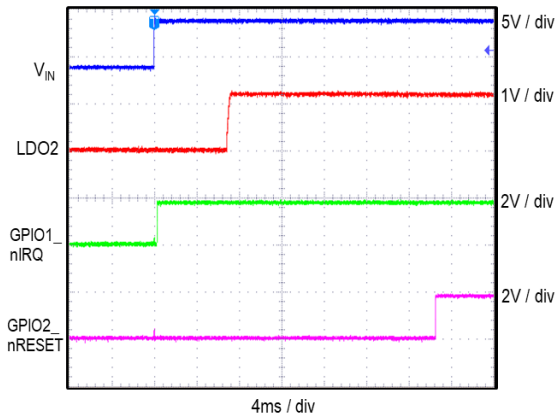

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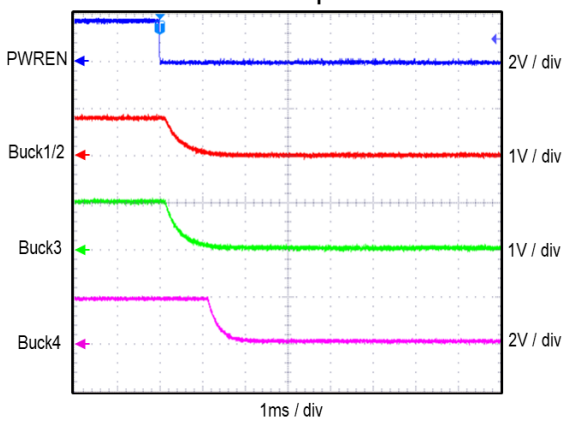
Power down Sequence - DPSLP



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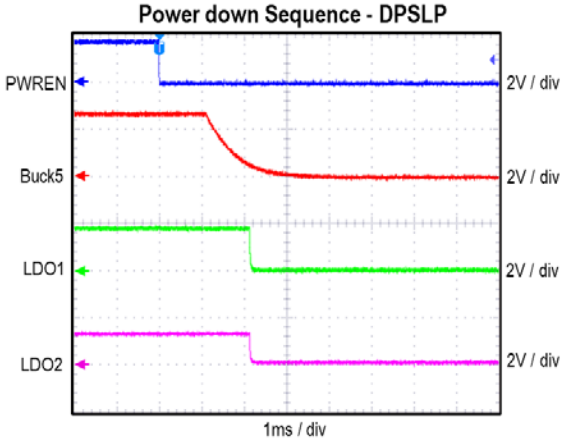
Power down Sequence - DPSLP



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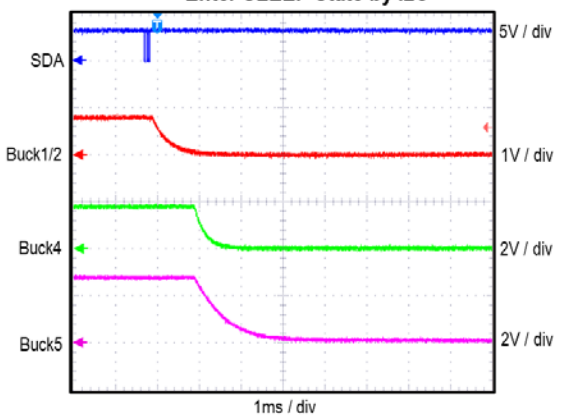
Enter SLEEP State by I2C



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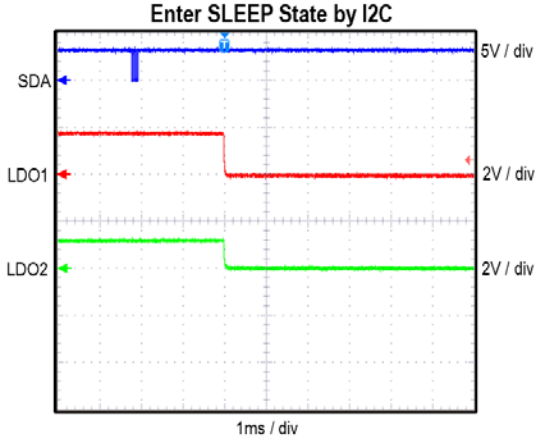
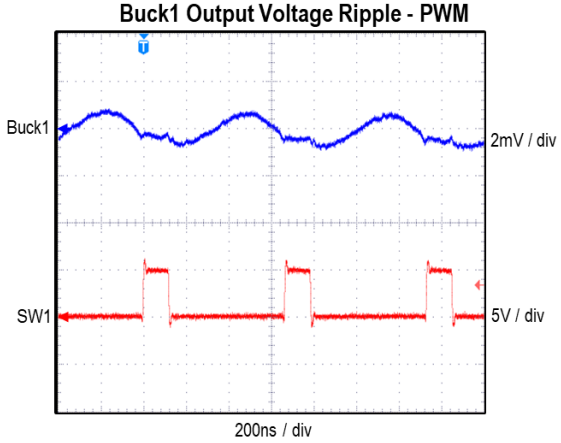
Enter SLEEP State by I2C



CMI 102
Buck1 Output Voltage Ripple - PWM



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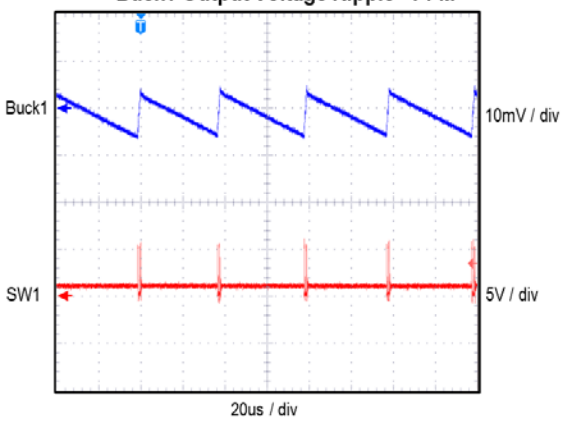
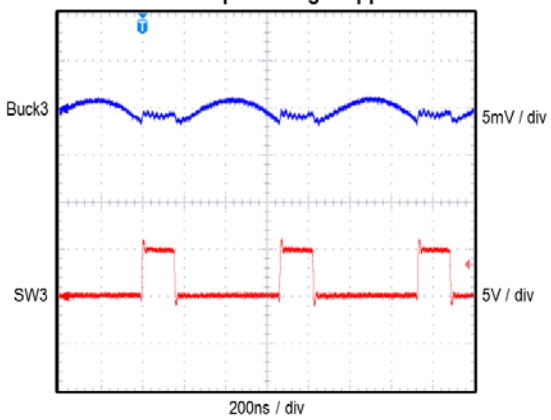
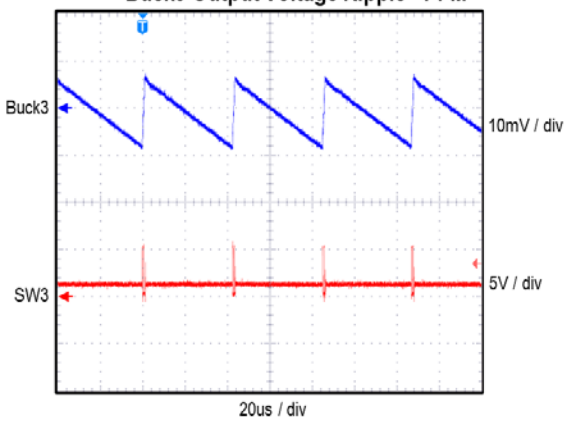
Buck1 Output Voltage Ripple - PFM



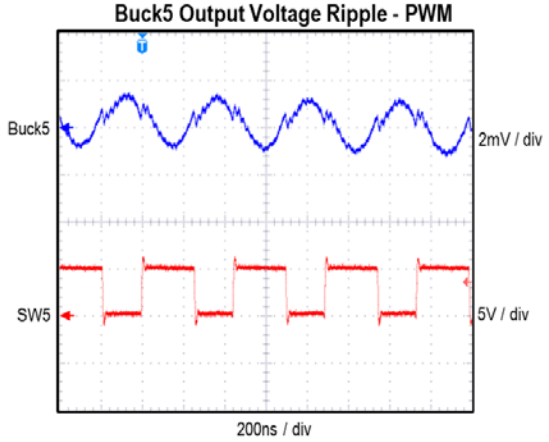
CMI 102
Buck3 Output Voltage Ripple - PWM



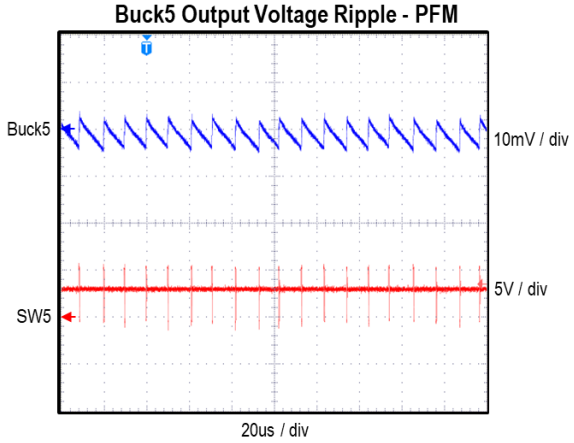
CMI 102
Buck3 Output Voltage Ripple - PFM



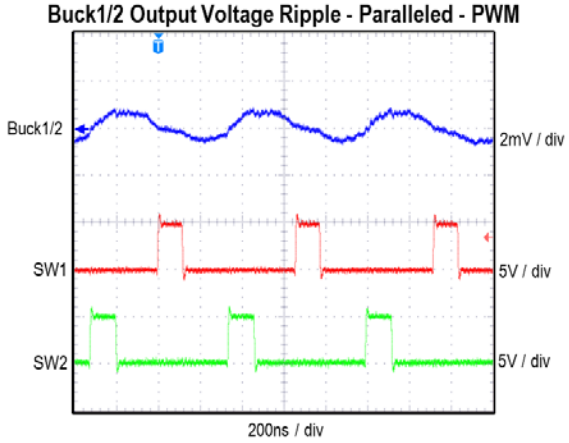
CMI 102
Buck5 Output Voltage Ripple - PWM



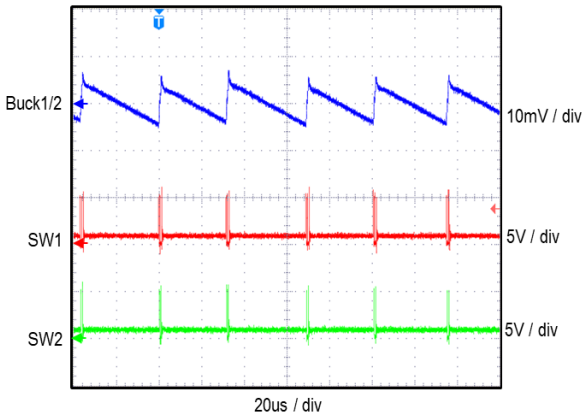
CMI 102
Buck5 Output Voltage Ripple - PFM



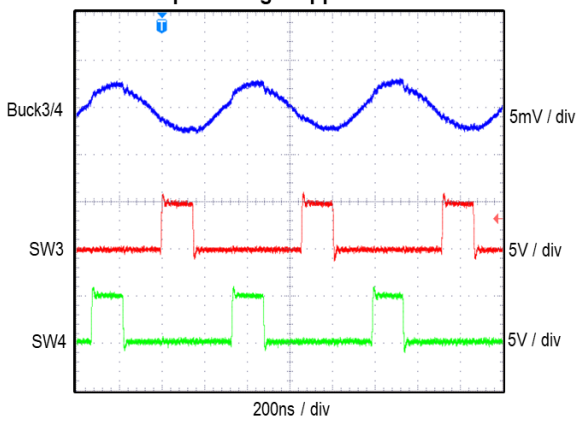
CMI 102
Buck1/2 Output Voltage Ripple - Paralleled - PWM



CMI 102
Buck1/2 Output Voltage Ripple - Paralleled - PFM



CMI 102
Buck3/4 Output Voltage Ripple - Paralleled - PWM



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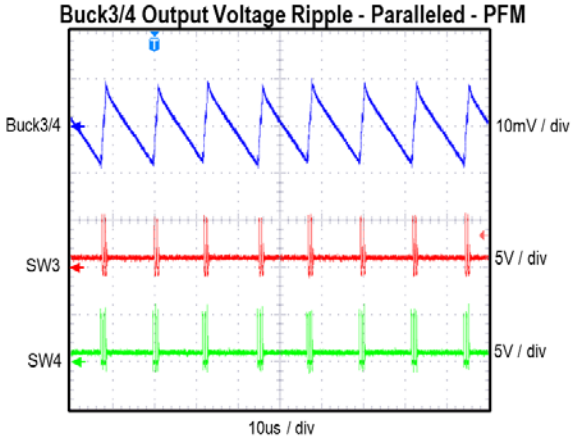
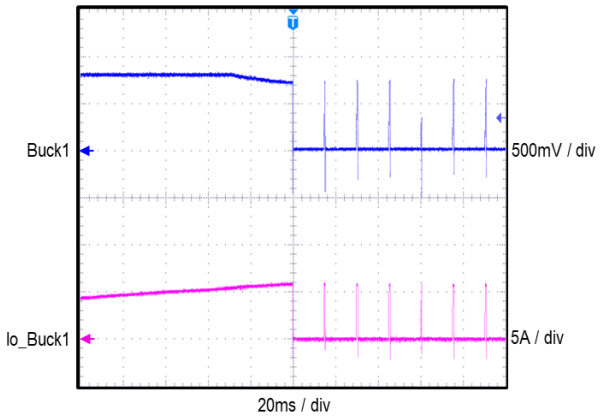
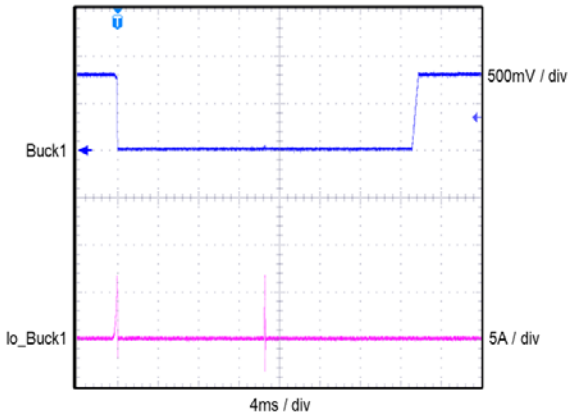
Buck3/4 Output Voltage Ripple - Paralleled - PFM



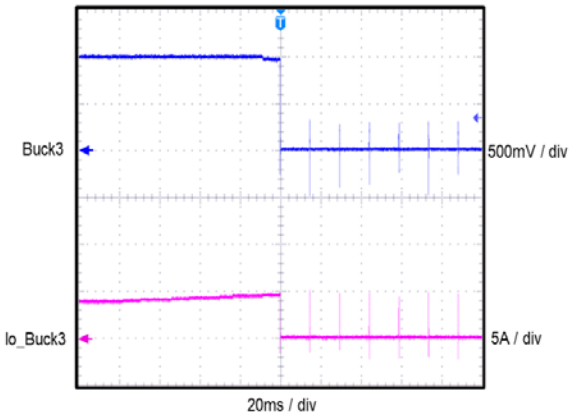
CMI 102
Buck1 Overcurrent



CMI 102
Buck1 Short Circuit



CMI 102
Buck3 Overcurrent



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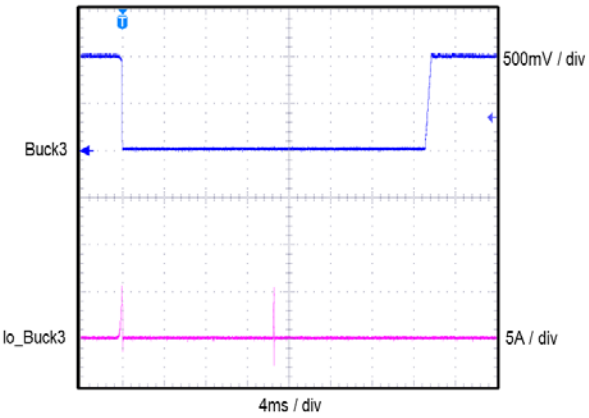
Buck3 Short Circuit



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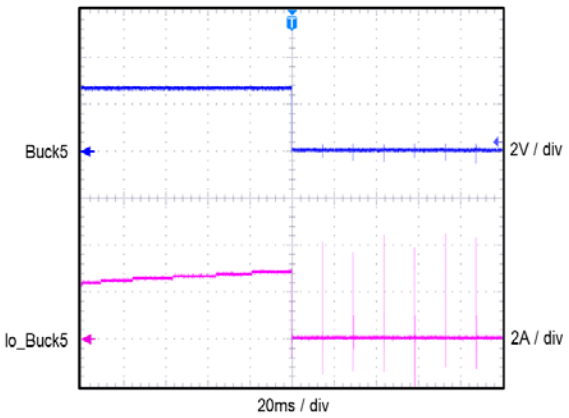
Buck5 Overcurrent



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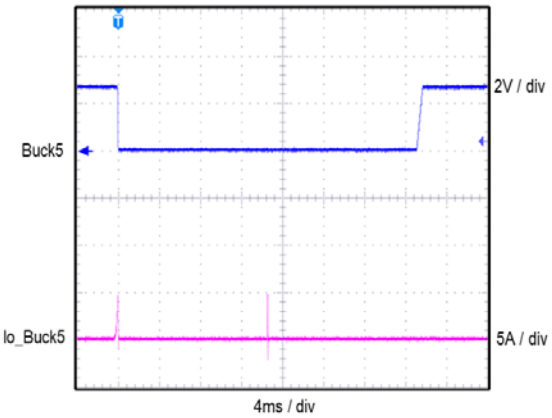
Buck5 Short Circuit



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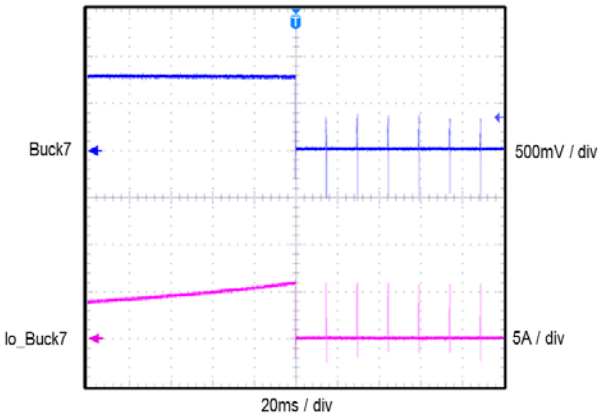
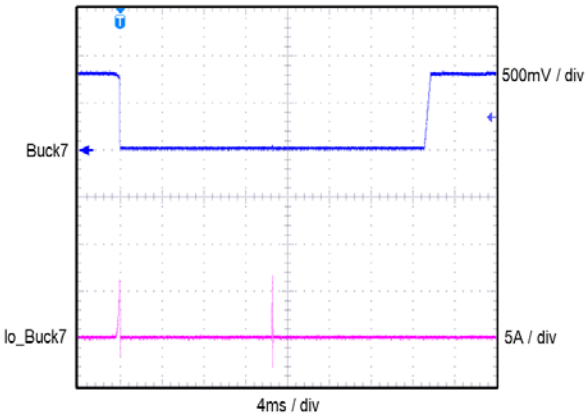
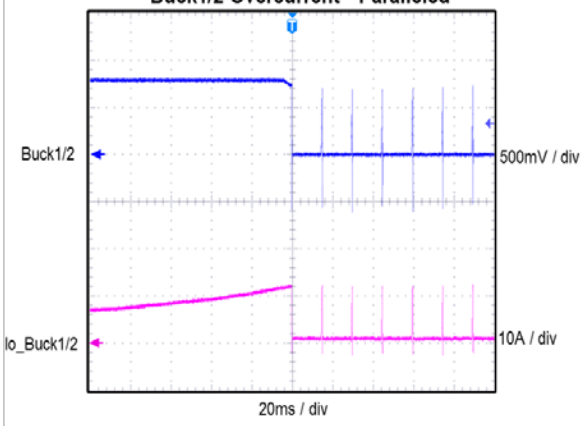
Buck7 Overcurrent



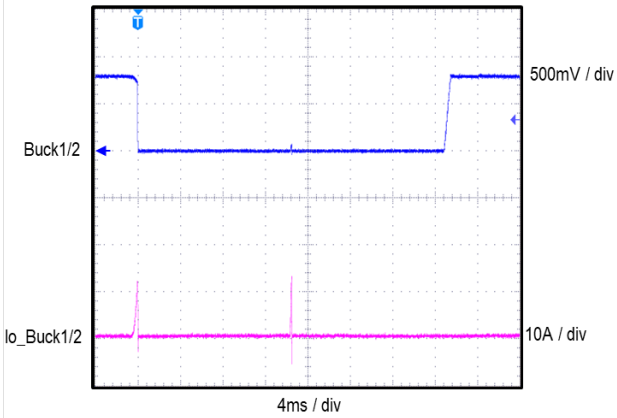
CMI 102
Buck7 Short Circuit



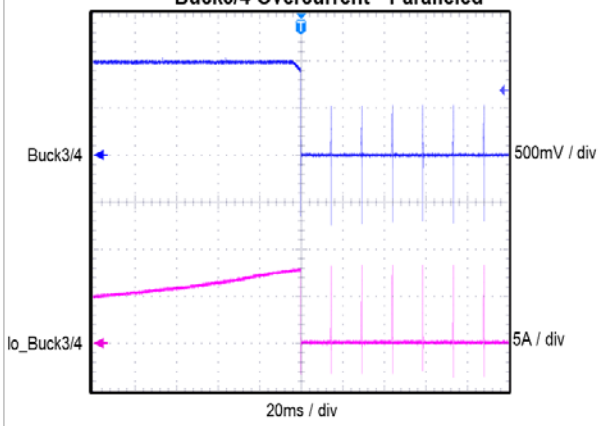
CMI 102
Buck1/2 Overcurrent - Paralleled



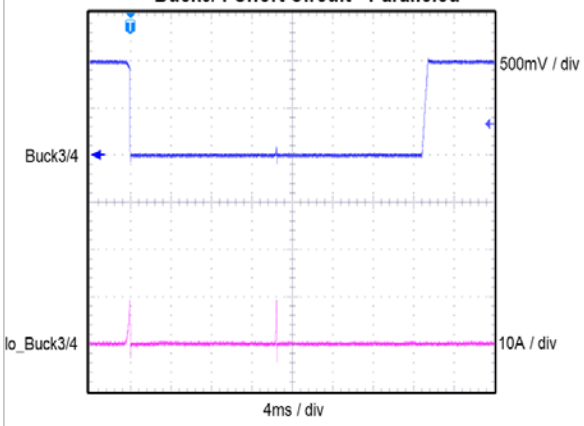
CMI 102
Buck1/2 Short Circuit - Paralleled



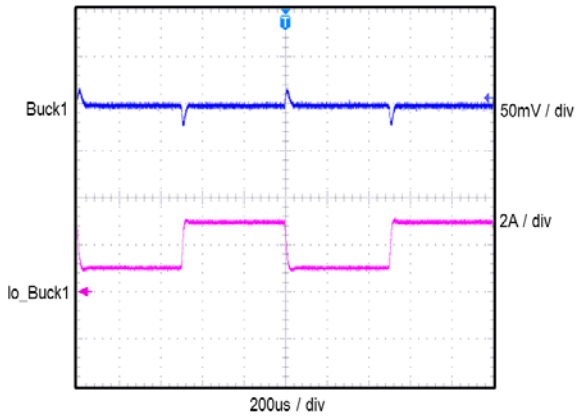
CMI 102
Buck3/4 Overcurrent - Paralleled



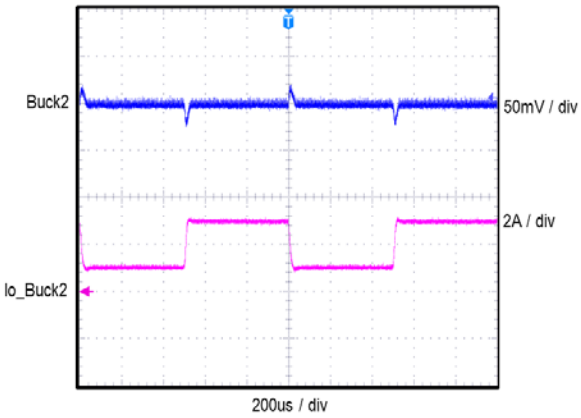
CMI 102
Buck3/4 Short Circuit - Paralleled



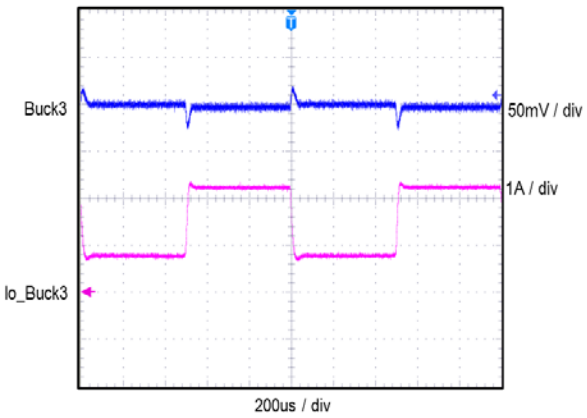
CMI 102
Buck1 Load Transient



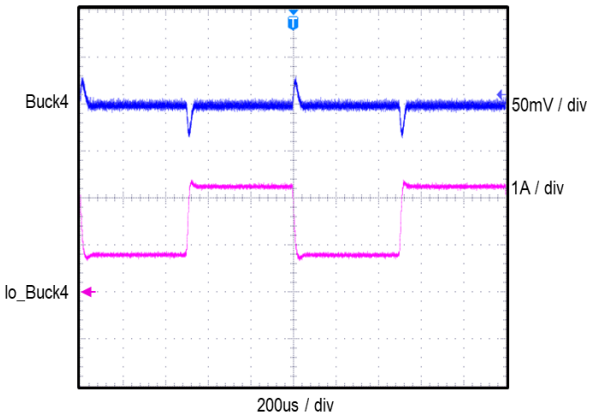
CMI 102
Buck2 Load Transient



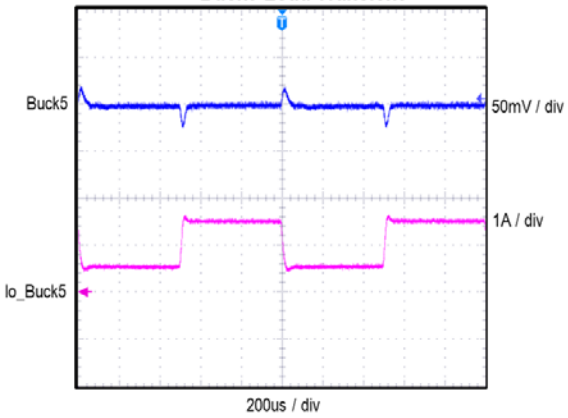
CMI 102
Buck3 Load Transient



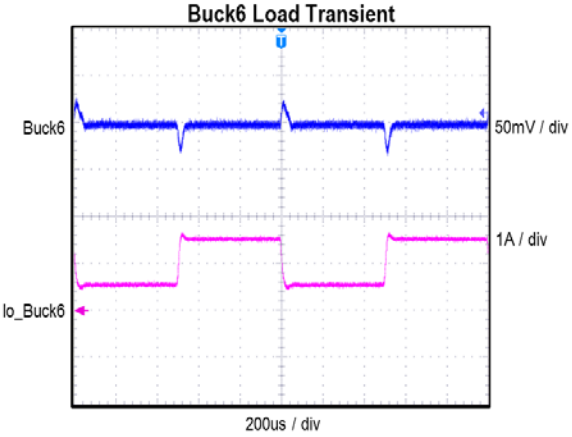
CMI 102
Buck4 Load Transient

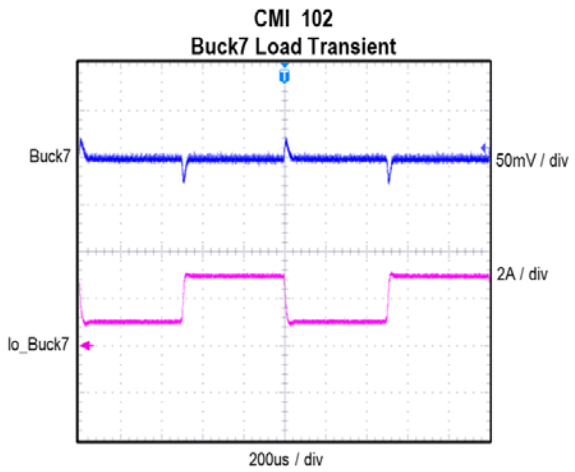


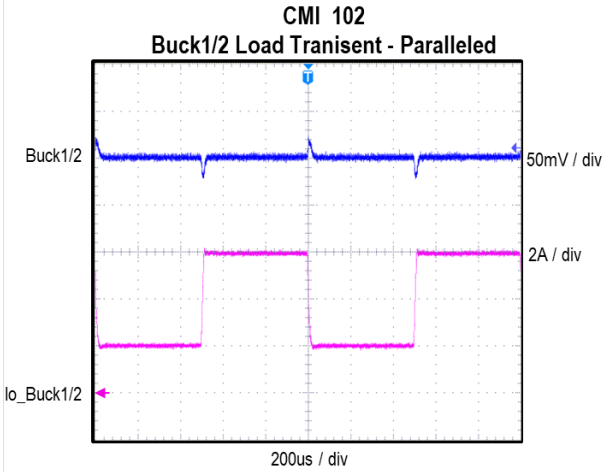
CMI 102
Buck5 Load Transient

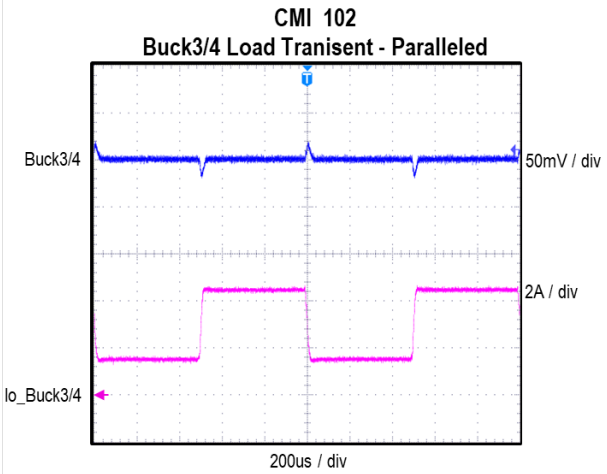


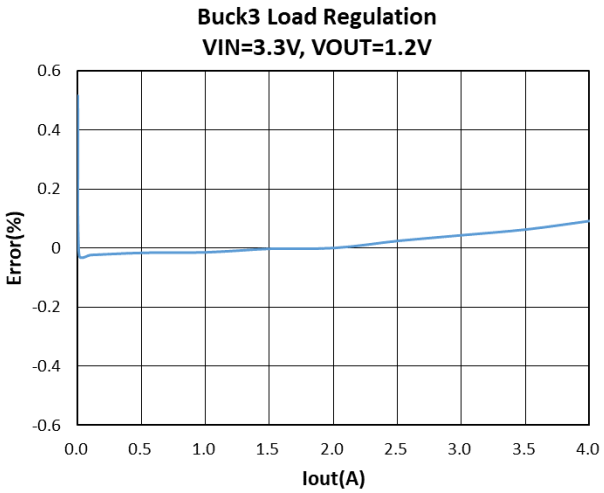
CMI 102
Buck6 Load Transient

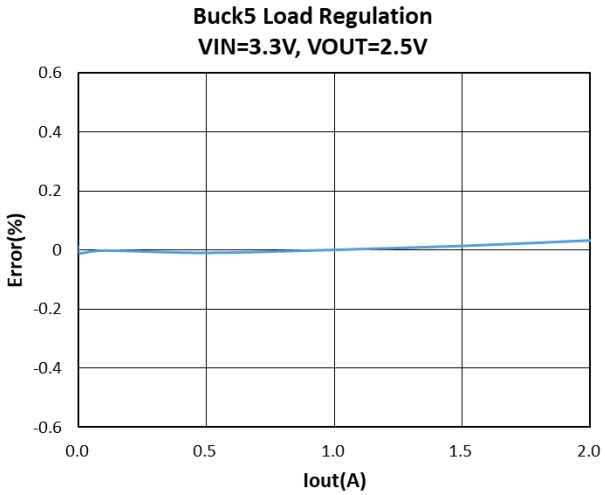


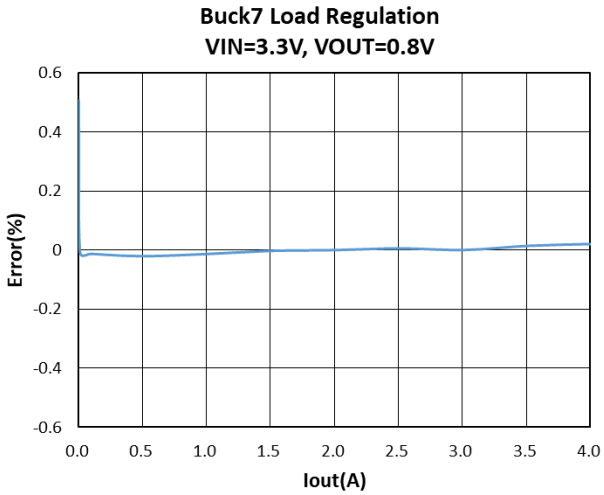




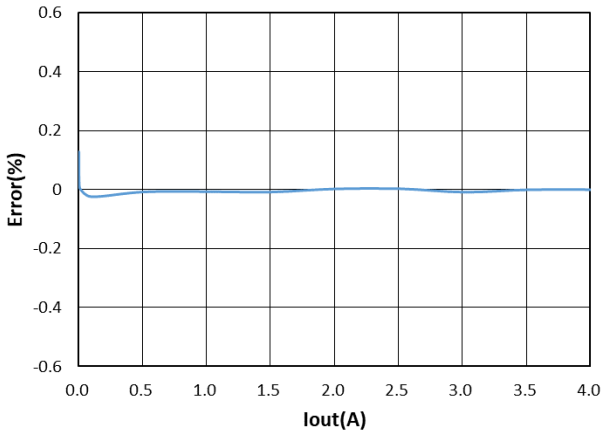




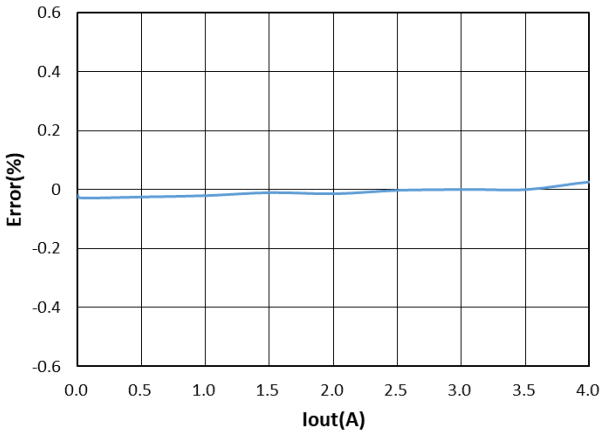




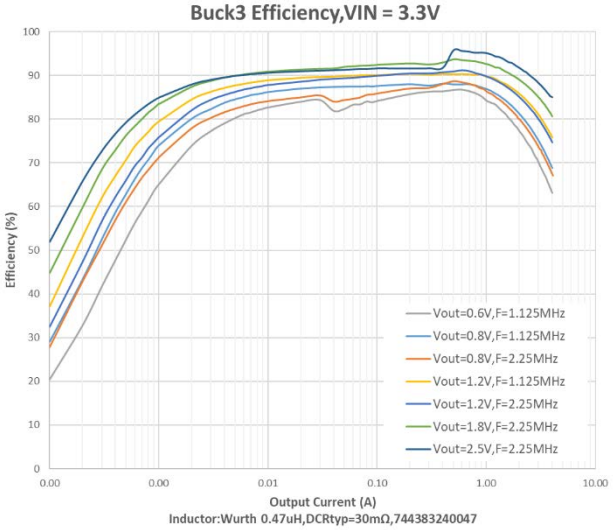
Buck1/2 Paralled Load Regulation
VIN=3.3V, VOUT=0.8V



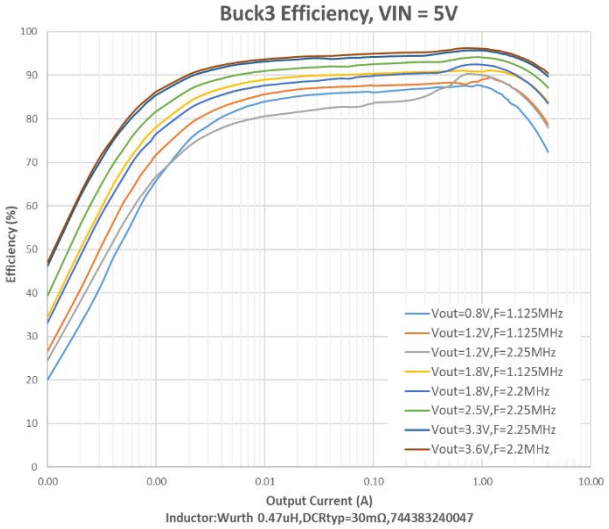
Buck3/4 Paralled Load Regulation
VIN=3.3V, VOUT=1.8V



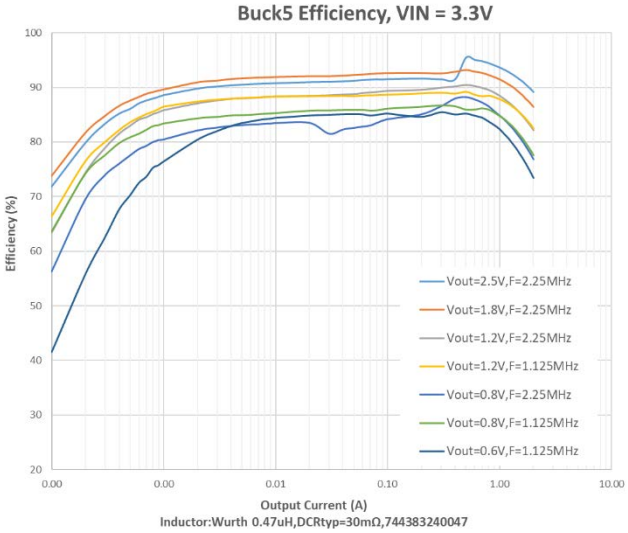
Buck3 Efficiency,VIN = 3.3V



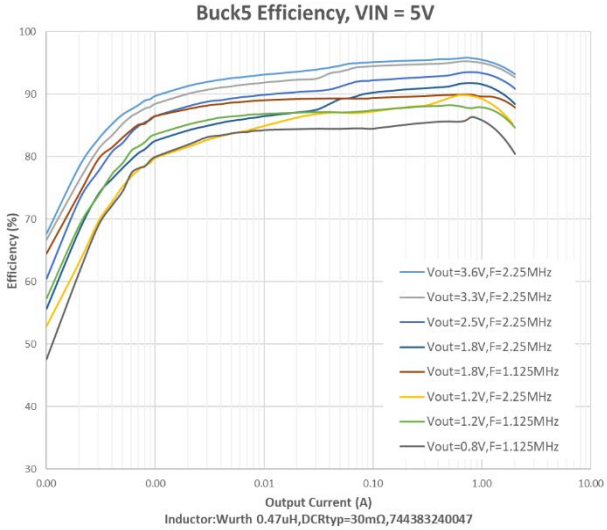
Buck3 Efficiency, VIN = 5V



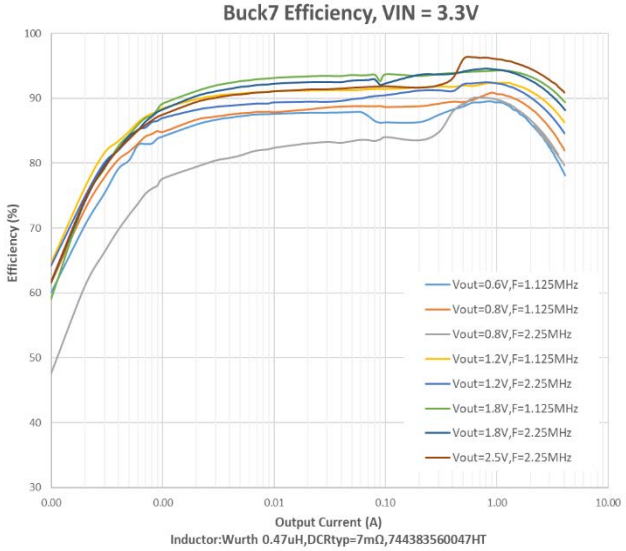
Buck5 Efficiency, VIN = 3.3V



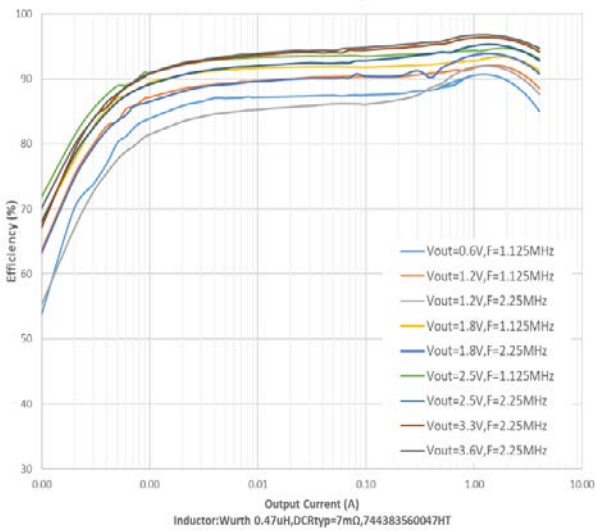
Buck5 Efficiency, VIN = 5V



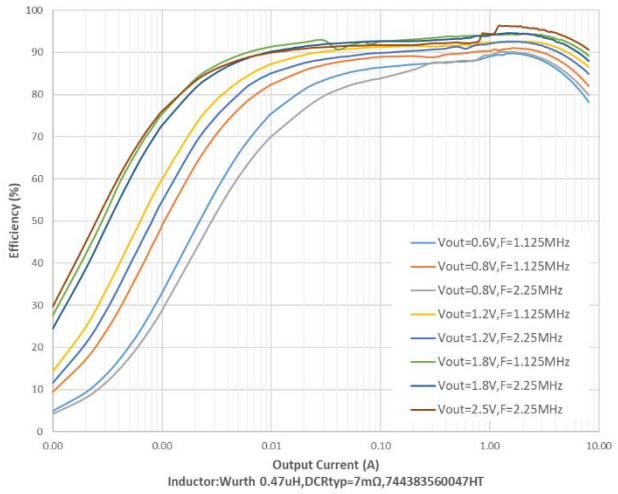
Buck7 Efficiency, VIN = 3.3V



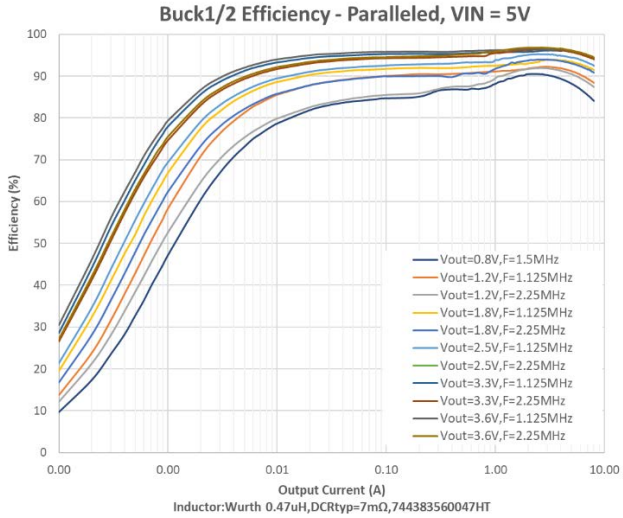
Buck7 Efficiency, VIN = 5V



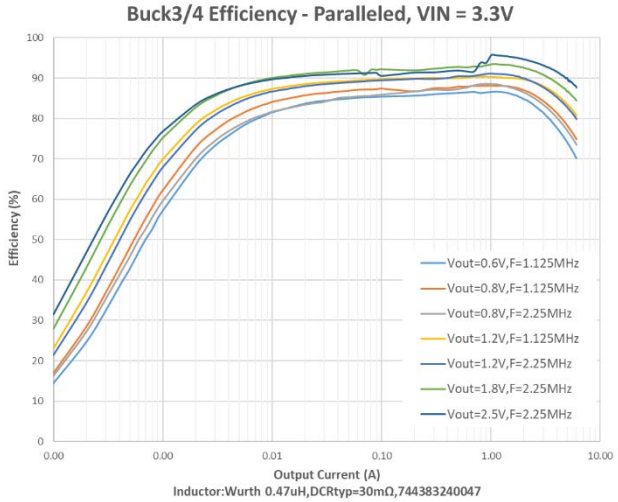
Buck1/2 Efficiency - Paralleled, VIN = 3.3V



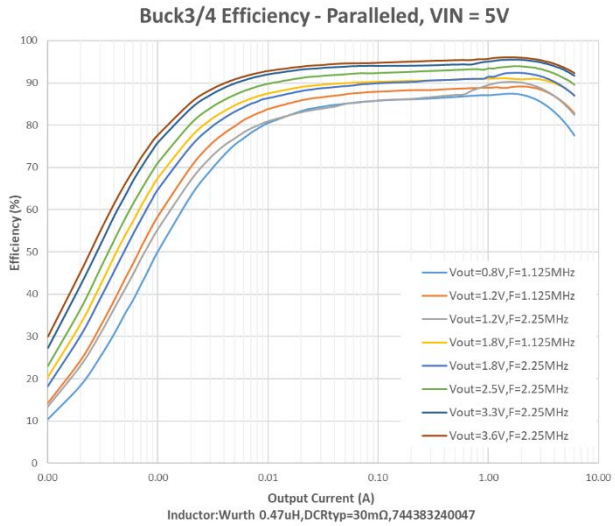
Buck1/2 Efficiency - Paralleled, VIN = 5V



Buck3/4 Efficiency - Paralleled, VIN = 3.3V



Buck3/4 Efficiency - Paralleled, VIN = 5V



This section provides the basic default configuration settings for each available ACT88760 CMI options. IC functionality in this section supersedes functionality in the main datasheet. Generating the desired functionality for a custom CMI sometimes requires reassigning internal resources, resulting in removal of base IC functionality. The following sections attempt to describe any removed functionality from the base IC functionality. The user is required to fully test all required functionality to ensure the CMI fully meets their requirements.

CMI 102: ACT88760-102.E2T

CMI 102.E2T is optimized for general IC evaluation. CMI 102. Is intended to be used as a starting point for general IC evaluation. After evaluating this IC, contact Qorvo for available custom IC options. CMI 102.E2T operates with 5V input voltage.

The following tables describe the ACT88760-102.E2T IC settings.

Voltage and Currents

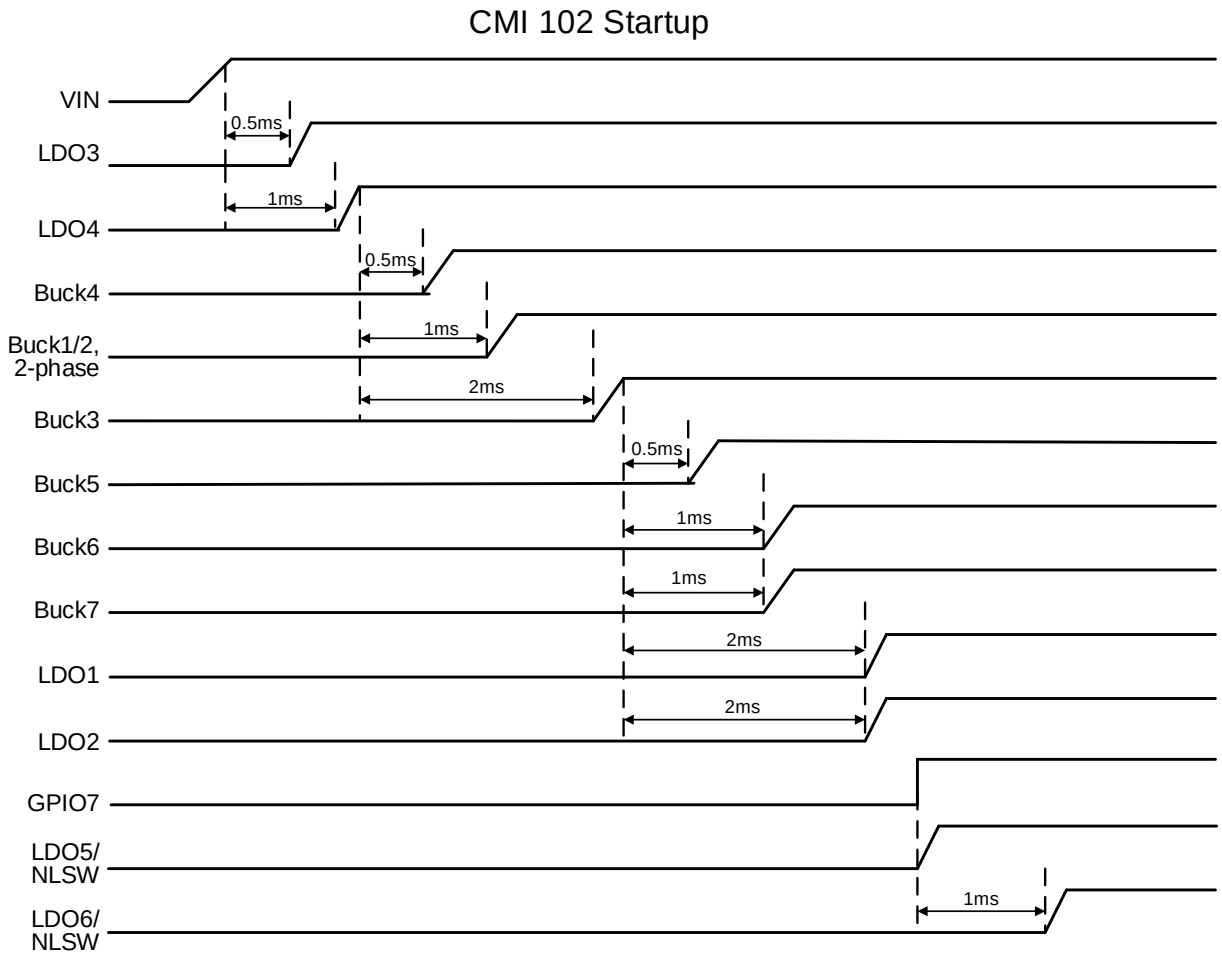
Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Voltage VSET2 (V)	DVS Voltage VSET2 (V)	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	Fsw (kHz)
Buck 1/2, 2-phase	0.8	0.75	0.7	0.65	OFF	OFF	5	1500
Buck3	1	0.9	n/a	n/a	OFF	OFF	4.5	1500
Buck4	1.8	1.8	n/a	n/a	OFF	OFF	4.5	2250
Buck5	2.7	2.5	n/a	n/a	OFF	OFF	3	2250
Buck6	3.3	3.3	n/a	n/a	OFF	ON VSET0	3	2250
Buck7	0.8	0.75	0.7	0.65	OFF	ON VSET0	5	1500
LDO1	1.8	n/a	n/a	n/a	OFF	OFF	0.81	n/a
LDO2	1.2	n/a	n/a	n/a	OFF	OFF	0.81.	n/a
LDO3	3.3	n/a	n/a	n/a	OFF	ON VSET0	0.41	n/a
LDO4	3.3	n/a	n/a	n/a	OFF	ON VSET0	0.41	n/a
LDO5	NLSW	n/a	n/a	n/a	OFF	OFF	0.41	n/a
LDO6	NLSW	n/a	n/a	n/a	OFF	OFF	0.41	n/a
EXT_EN	OFF	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (µs)	Soft-Start (us)	Shutdown Delay (us)
LDO3	1	UVLO	500	320	0
LDO4	2	UVLO	1000	320	0
Buck4	3	LDO4	500	500	1000
Buck1/2, 2-phase	4	LDO4	1000	500	0
Buck3	5	LDO4	2000	500	0
Buck5	6	Buck3	500	500	1000
Buck6	7	Buck3	1000	500	0
Buck7	7	Buck3	1000	500	0
LDO1	8	Buck3	2000	320	2000
LDO2	8	Buck3	2000	320	2000
LDO5/ NLSW	9	GPIO7	0	320	4000
LDO6/ NLSW	10	GPIO7	1000	320	4000

Voltage Thresholds

Setting	Voltage Threshold
UVLO	2.7V
SYSMON	3V
SYSWARN	3.1V
POK_OV	5.6V
VIN_OV	5.8V



SLEEP Mode

There is no GPIO programmed as SLEEP mode, use I2C can enter SLEEP Mode by setting 0x07h bit6 SLEEP=1.

PWREN/DPSLP

GPIO6 is programmed as the PWREN input, PWREN can be used to control the DPSLP state. Apply power supply to VIN with GPIO6=High, system startup as the power on sequence, after power on, pull GPIO6=Low, system enter DPSLP mode, pull GPIO6=high, system exit DPSLP mode.

nRESET

GPIO2 is programmed as nRESET output with 40ms from Buck3 POK. Will have external pull up. Internal pull up to VIO is okay as VIO is powered by LDO6 externally.

DVS Mode

GPIO3 is programmed as the Buck1/2/7 DVS input1, GPIO4 is programmed as the Buck1/2/7 DVS input2, together with GPIO3 and GPIO4, they can control Buck1/2/7 output DVS from VSET0 to VSET3.

GPIO5 is programmed as the DVS input for Buck3/4/5/6.

LED Driver

GPIO10 is programmed as an output LED driver with default 0mA sink current. The sink current can be changed by 0x33h GPIO10_ILED[3:0].

GPIO1 (pin C6) – nIRQ

GPIO1 is an open drain output for nIRQ.

GPIO2 (pin E5) – nRESET

GPIO2 is an open drain output for nRESET. nRESET gated by the logical AND of all the selected rails with 20ms delay.

GPIO3 (pin B5) – Buck1/2/7 DVS input1

GPIO3 is programmed as the DVS input1 signal for Buck1/2/7.

GPIO4 (pin B7) – Buck1/2/7 DVS input2

GPIO4 is programmed as the DVS input2 signal for Buck1/2/7. Together with GPIO3, they can control Buck1/2/7 DVS from VSET0 to VSET3.

GPIO5 (pin D7) – Buck3/4/5/6 DVS input

GPIO5 is programmed as the DVS input signal for Buck3/4/5/6.

GPIO6 (pin E7) – PWREN

GPIO6 is programmed as the PWREN input, PWREN can be used to control the DPSLP state.

GPIO7 (pin C4) – EXT_PG

GPIO7 is programmed as an EXT_PG for LDO5/6.

GPIO8 (pin D4) – SYSWARN output

GPIO8 is programmed as an open drain output for SYSWARN.

GPIO9 (pin E4) – SYSMON output

GPIO9 is programmed as an open drain output for SYSMON.

GPIO10 (pin F4) – LED Driver

GPIO10 is programmed as a LED driver with 0mA default sink current.

GPIO11 (pin F6) – SLEEP

GPIO11 is programmed as the SLEEP Mode input.

I2C Address

The CMI 102 7-bit Slave I2C address (for Master, GPIOs, Buck1-6) is 0x25h. This results in 0x4Ah for a write address and 0x4Bh for a read address. The CMI 102 7-bit Slave I2C address (for Buck7, LDO1-6) is 0x28h. This results in 0x50h for a write address and 0x51h for a read address.

CMI 104: ACT88760-104T

The ACT88760-104T is a joint development between Qorvo and Inuitive. It is directly compatible with Inuitive's NU4000 AI Video Processor voltages and sequencing requirements. Inuitive uses the ACT88760-104 to power their NU4000 on their M4.3V reference design. The NU4000C1 SoC is a High-Performance 3D imaging and Vision Processor that's implemented using the TSMC 12nm process. The NU4000C1 architecture is designed as an integrated platform that contains enriched sub-systems and provides accelerated image processing features such as, Depth (3D) Imaging, Objects Recognition and Tracking, and other computer vision algorithms. The ACT88760-104 is optimized for a 5V input voltage. More details about Inuitive's NU4000C1 can be found on the Inuitive website.

The following tables describe the ACT88760-104T IC settings.

Voltage and Currents

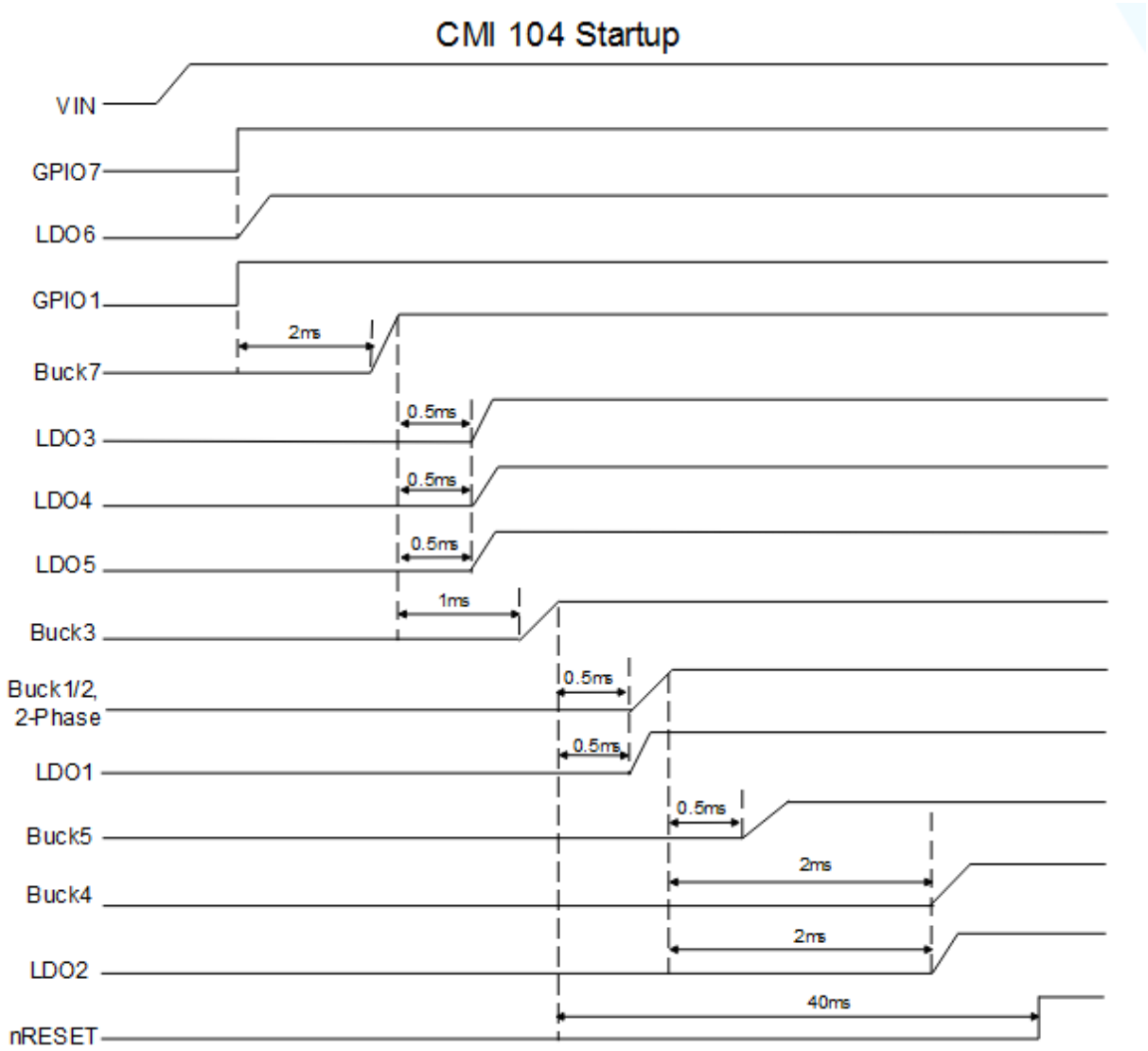
Rail	Active Mode Voltage VSET0 (V)	DVS Voltage VSET1 (V)	DVS Voltage VSET2 (V)	DVS Voltage VSET2 (V)	Sleep Mode Voltage (V)	DPSLP Mode Voltage (V)	Current Limit (A)	Fsw (kHz)	Output Voltage Range
Buck 1/2, 2-phase	0.8	0.8	0.8	0.8	OFF	OFF	5	1125	Low
Buck3	1.8	1.8	n/a	n/a	OFF	OFF	4.5	2250	High
Buck4	1.1	1.1	n/a	n/a	OFF	OFF	4.5	2250	Low
Buck5	1.2	1.2	n/a	n/a	OFF	OFF	3	2250	High
Buck6	1.2	1.2	n/a	n/a	OFF	OFF	3	2250	High
Buck7	3.3	3.3	3.3	3.3	OFF	OFF	5	2250	High
LDO1	0.8	n/a	n/a	n/a	OFF	OFF	0.81	n/a	Low
LDO2	1.8	n/a	n/a	n/a	OFF	OFF	0.81.	n/a	High
LDO3	2.8	n/a	n/a	n/a	OFF	OFF	0.41	n/a	High
LDO4	2.8	n/a	n/a	n/a	OFF	OFF	0.41	n/a	High
LDO5	2.8	n/a	n/a	n/a	OFF	OFF	0.41	n/a	High
LDO6	1.8	n/a	n/a	n/a	OFF	ON VSET0	0.41	n/a	High
EXT_EN	OFF	n/a	n/a	n/a	n/a	n/a	n/a	n/a	n/a

Startup and Sequencing

Rail	Sequence Order	Sequencing Input Trigger	StartUp Delay (µs)	Soft-Start (us)	Shutdown Delay (us)
LDO6	1	GPIO7	0	250	0
Buck7	2	GPIO1	2000	500	8000
LDO3	3	Buck7	500	250	500
LDO4	3	Buck7	500	250	500
LDO5	3	Buck7	500	250	500
Buck3	4	Buck7	1000	500	2000
Buck1/2, 2-phase	5	Buck3	500	500	2000
LDO1	5	Buck3	500	250	2000
Buck5	6	Buck1	500	500	4000
Buck4	7	Buck1	2000	500	1000
LDO2	7	Buck1	2000	250	1000
Buck6 ISP -OFF	n/a	n/a	500	500	0

Voltage Thresholds

Setting	Voltage Threshold
UVLO	2.7V
SYSMON	2.8V
SYSWARN	3V
POK_OV	5.6V
VIN_OV	5.8V



SLEEP Mode

GPIO11 is SLEEP Mode input. Will be pulled up to VIN by external resistor. When GPIO11=L, all regulators OFF.

DPSLP Mode

There is no GPIO programmed as DPLSP mode, use I2C can enter DPSLP Mode by setting 0x07h bit4 DPSLP=1.

PWRON

GPIO1 is programmed as the PWRON input. Pulled low to turn off ALL outputs (except LDO6) based on the OFF sequence setting. Pulled high to allow all outputs (except LDO6) to turn on based on the input trigger setting. After power up the PWRON may be controlled by external host. Note that if the IC is powered by CIPS, the PWRON function is masked, it can't control regulators on/off.

nRESET

GPIO2 is programmed as nRESET output with 40ms delay from Buck3 POK. Will have external pull up. Internal pull up to VIO is okay as VIO is powered by LDO6 externally.

DVS Mode

There is no DVS function in this CMI.

EXT_PG

GPIO7 is programmed as an EXT_PG input to turn on LDO. In normal operation, GPIO7 will always be pulled high and LDO6 will be "always ON". LDO6 is on when both GPIO7 (EXT_PG) and GPIO11 (SLEEP) are high.

GPIO1 (pin C6) – PWRON

GPIO1 is the digital input for PWRON.

GPIO2 (pin E5) – nRESET

GPIO2 is an open drain output for nRESET. nRESET gated by Buck3 POK with 40ms delay.

GPIO3 (pin B5) – Not used

GPIO3 is not used. It is programmed as an open drain output and is high impedance.

GPIO4 (pin B7) – nIRQ

GPIO4 is an open drain output for nIRQ.

GPIO5 (pin D7) – Not used

GPIO5 is not used. It is programmed as an open drain output and is high impedance.

GPIO6 (pin E7) – Not used

GPIO6 is not used. It is programmed as an open drain output and is high impedance.

GPIO7 (pin C4) – EXT_PG

GPIO7 is programmed as an EXT_PG input to turn on LDO. In normal operation, GPIO7 will always be pulled high and LDO6 will be "always ON". LDO6 is on when both GPIO7 (EXT_PG) and GPIO11 (SLEEP) are high.

GPIO8 (pin D4) – Not used

GPIO8 is not used. It is programmed as an open drain output and is high impedance.

GPIO9 (pin E4) – Not used

GPIO9 is not used. It is programmed as an open drain output and is high impedance.

GPIO10 (pin F4) – Not used

GPIO10 is not used. It is programmed as an open drain output and is high impedance.

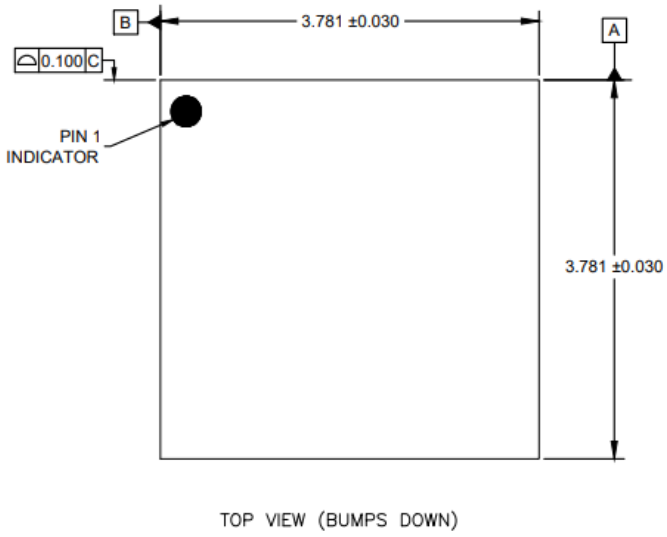
GPIO11 (pin F6) – SLEEP

GPIO11 is programmed as the SLEEP Mode input.

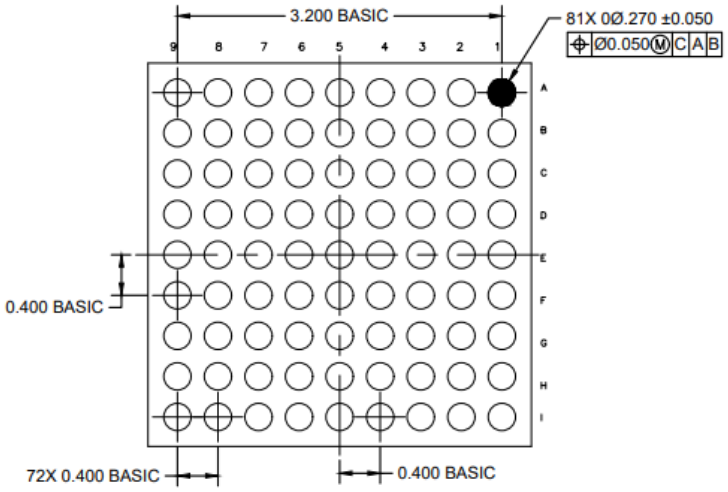
I2C Address

The CMI 104 7-bit Slave I2C address (for Master, GPIOs, Buck1-6) is 0x25h. This results in 0x4Ah for a write address and 0x4Bh for a read address. The CMI 104 7-bit Slave I2C address (for Buck7, LDO1-6) is 0x28h. This results in 0x50h for a write address and 0x51h for a read address.

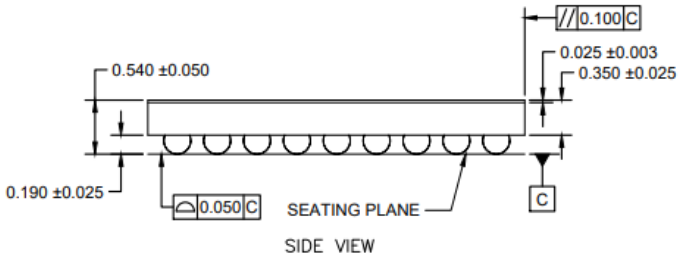
PACKAGE OUTLINE AND DIMENSIONS



TOP VIEW (BUMPS DOWN)



BOTTOM VIEW (BUMPS UP)



SIDE VIEW

Product Compliance

This part complies with RoHS directive 2011/65/EU as amended by (EU) 2015/863.

This part also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com **Tel: 1-844-890-8163**

Email: customer.support@qorvo.com

For technical questions and application information:

Email: appsupport@qorvo.com

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