ACT86600

Hybrid PMIC for Enterprise Storage and Computing

BENEFITS and FEATURES

- Wide operating voltage range
  - Vin = 2.7V to 14.4V
  - Withstand input voltage up to 16V
  - Vout = 0.6V to 5.26V
- Complete Integrated Power Solution
  - Two 6A DC-DC buck converters
  - Two 4A DC-DC buck converters
  - One 0.5A DC-DC buck converter
  - One 0.6A DC-DC Buck-Boost converter
  - Integrated Power FETs
- High efficiency
  - Up to 96% efficiency
  - Single stage 12V conversion
  - Low Quiescent current, <300uA
- Excellent dynamic response
  - Programmable switching frequency
  - Small inductor sizes
  - Fast transient response
  - Proprietary COT control algorithm
- High current, Multi-phase functionality
  - Single or multiphase phase outputs
  - 8A and 12A multiphase outputs
  - Staggered phasing in 2-phase operation
- Highly configurable
  - 400KHz – 1.9MHz Frequency Range.
  - Near constant frequency operation.
  - Accepts wide inductor values and sizes.
- Easy system level design
  - Configurable sequencing
  - Independent On & Off sequencing control.
  - Sequencing with external power supplies
  - Seven programmable GPIOs
  - I2C Interface with password protection.
  - Reset /Power Good Output
- Flexible System Level Design
  - Versatile GPIO functions
  - Multiple Sleep modes
  - Soft / Hard Reset Functions
  - Watchdog Supervision
  - Interrupt function available.
  - I2C Safety bits to enhance immunity against spurious I2C transactions.
- Fault protection
  - Input UV and OV Monitoring for each buck input.
  - Input and Output UV and OV Detection
  - Interrupt Controller and fault monitoring options.
  - Resistor-less Over Current Protection (OCP)
  - System voltage monitoring.
  - Small form factor 6X6mm FCOL QFN Package.

APPLICATIONS

- Solid-State Drives
- Microcontroller Applications
- FPGA
- Personal Navigation Devices

GENERAL DESCRIPTION

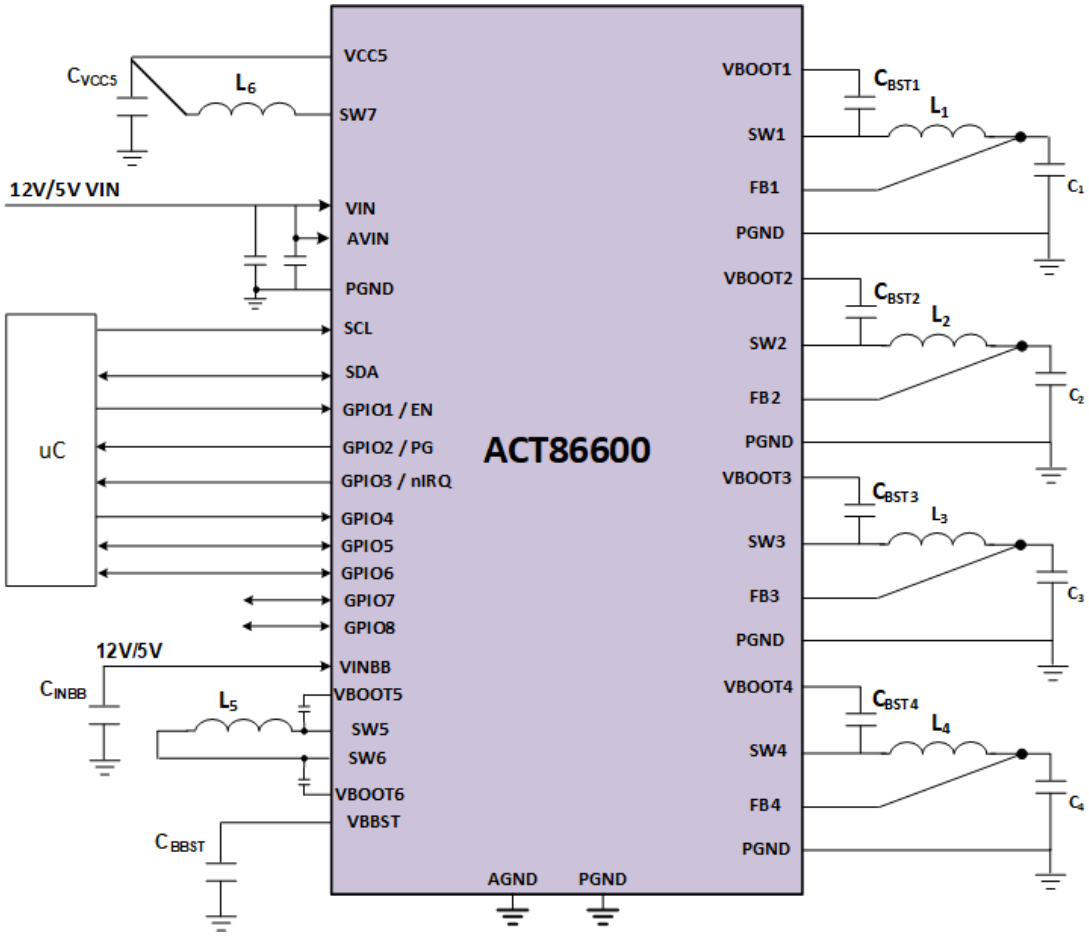
The ACT86600 PMIC is an integrated ActivePMU power management unit. It is highly flexible and can be reconfigured via I^2C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc.

The core of the device includes 4 high power DC/DC step down converters, a lower power step down converter and a buck-boost converter. Each regulator can be configured for a wide range of output voltages through the I^2C interface.

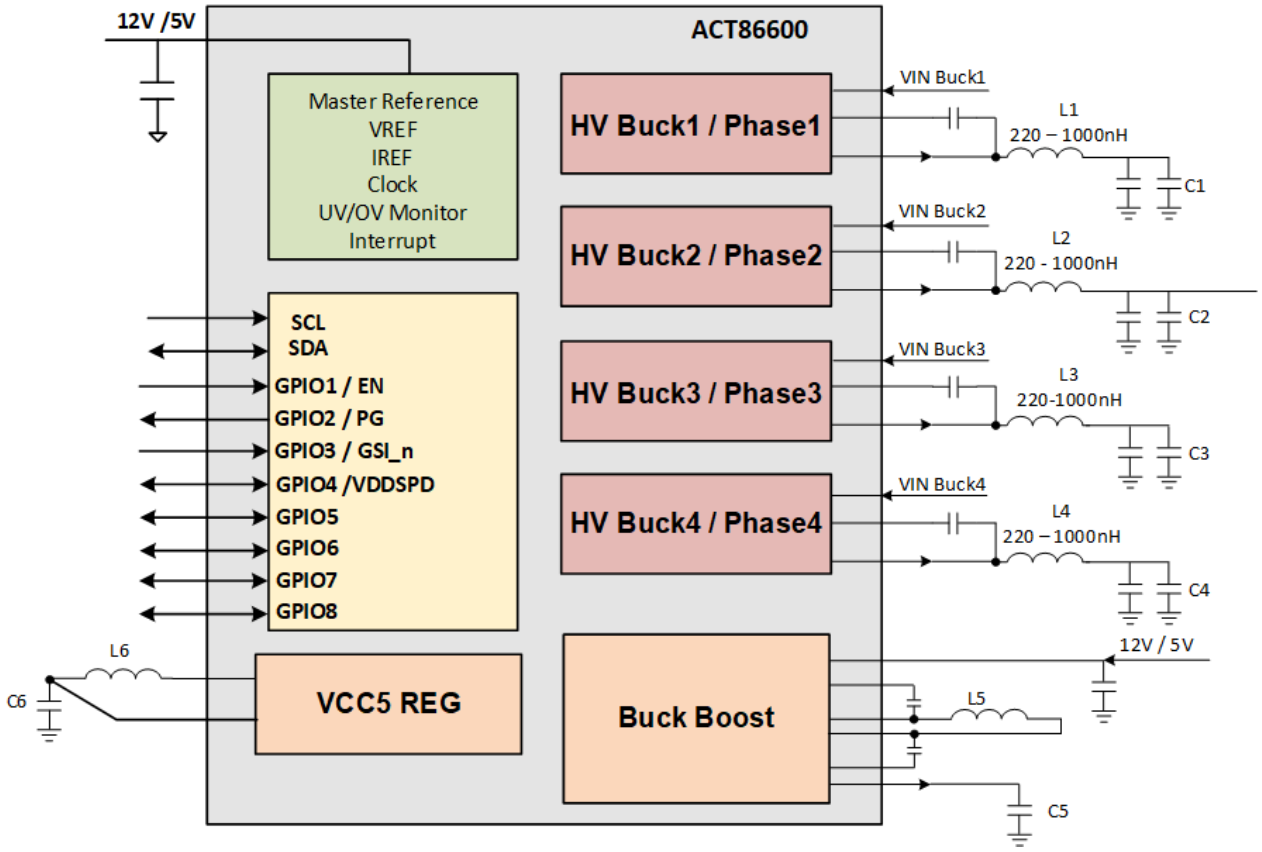
The ACT86600 is a high voltage PMIC that is optimized for single stage voltage conversion from 12V input power sources. It operates with a 2.7V to 14.4V input voltage and can withstand 16V input voltage surges. The four high current regulators can be configured as single phase outputs, or can be paralleled for up to 12A dual phase with outputs.

The ACT86600 PMIC is available in a 6 x 6 mm 48 pin QFN package.

TYPICAL APPLICATION DIAGRAM

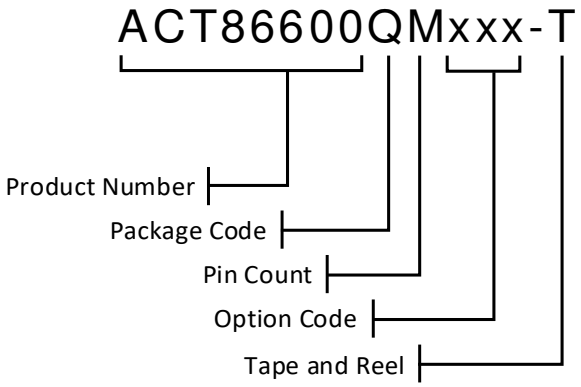


FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	Input Voltage	V_{BUCK1}	V_{BUCK2}	V_{BUCK3}	V_{BUCK4}	V_{CC5}	V_{BBST}
ACT86600QM101-T	12V	0.8V	1.2V	1.8V	3.3V	5.0V	12V



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Qorvo components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that comply with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator “Q” represents QFN

Note 4: Pin Count designator “M” represents 48 pins

Note 5: “xxx” represents the CMI (Code Matrix Index) option. The CMI identifies the IC’s default register settings

Note 6: See the CMI Option section in the back of the datasheet for a more detailed description of each CMI’s settings.

PIN CONFIGURATION

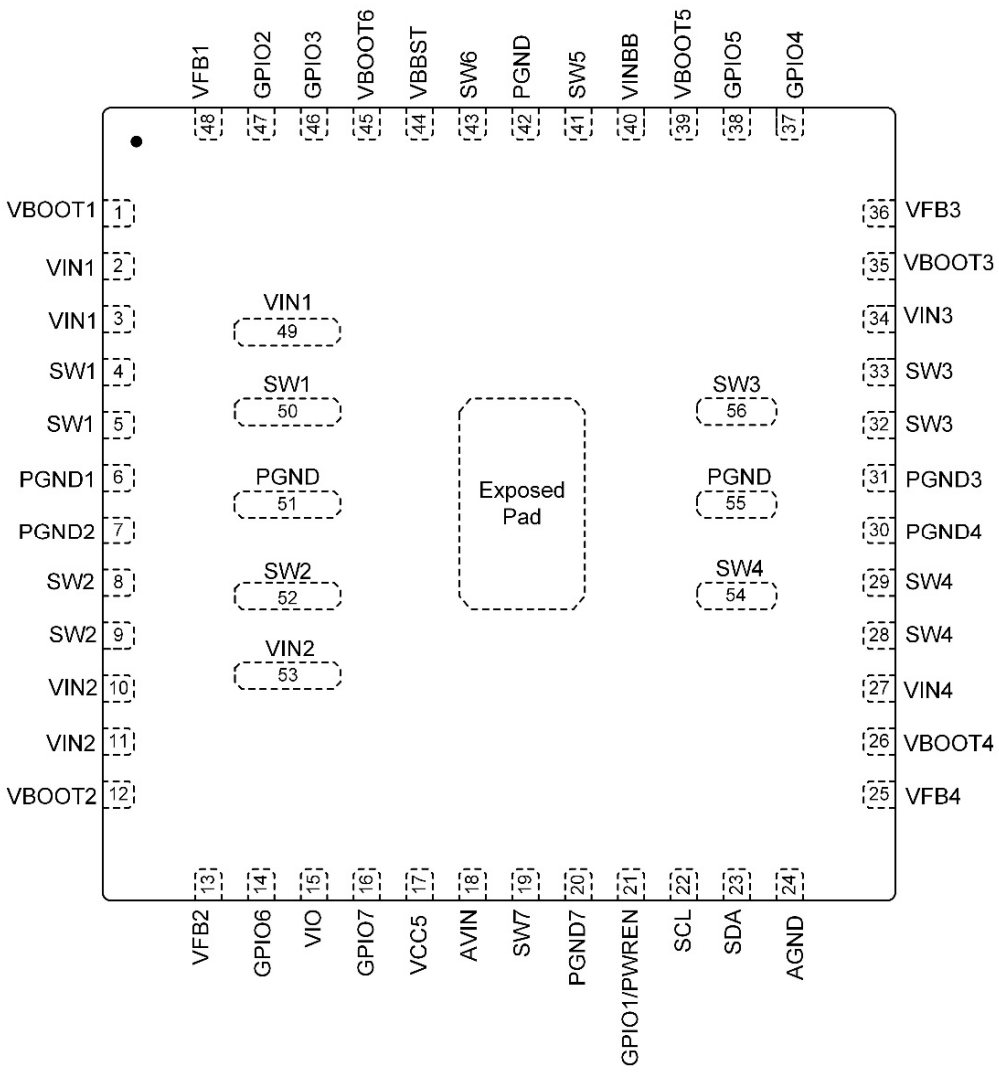


Figure 1: Pin Configuration – Top View (pins down) 48pin FCOL QFN Package 6mm x 6mm

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	VBOOT1	Boot strap voltage for Buck1 regulator
2	VIN1	Dedicated input power input to Buck1 regulator
3	VIN1	Dedicated input power input to Buck1 regulator
4	SW1	Switch pin for Buck1 regulator
5	SW1	Switch pin for Buck1 regulator
6	PGND1	Power Ground for Buck1 regulator
7	PGND2	Power Ground for Buck2 regulator
8	SW2	Switch pin for Buck2 regulator
9	SW2	Switch pin for Buck2 regulator
10	VIN2	Dedicated input power input to Buck2 regulator
11	VIN2	Dedicated input power input to Buck2 regulator
12	VBOOT2	Boot strap voltage for Buck2 regulator
13	VFB2	Output and feedback pin for Buck2 regulator
14	GPIO6	GPIO6 pin. It is configurable with the default function based on CMI
15	VIO	VIO pin
16	GPIO7	GPIO7 pin. It is configurable with the default function based on CMI
17	VCC5	5.0V Output from PMIC / PMIC power source used to power the PMIC internally.
18	AVIN	Analog input power for the PMIC
19	SW7	Switch pin for VCC5 generating switching regulator
20	PGND7	Power Ground for the VCC5 regulator. It is also used for the AVIN ground reference.
21	GPIO1	GPIO1 pin. It is configurable with default configuration based on the CMI. This GPIO can be used as either the PWREN or Enable function.
22	SCL	I^2C Serial Clock Pin
23	SDA	I^2C Serial Data pin
24	AGND	Analog Ground
25	VFB4	Output and feedback pin for Buck4 regulator
26	VBOOT4	Boot strap voltage for Buck4 regulator
27	VIN4	Dedicated input power input to Buck4 regulator
28	SW4	Switch pin for Buck4 regulator
29	SW4	Switch pin for Buck4 regulator
30	PGND4	Power Ground for Buck4 regulator
31	PGND3	Power Ground for Buck3 regulator

32	SW3	Switch pin for Buck3 regulator
33	SW3	Switch pin for Buck3 regulator
34	VIN3	Dedicated input power input to Buck3 regulator
35	VBOOT3	Boot strap voltage for Buck3 regulator
36	VFB3	Output and feedback pin for Buck3 regulator
37	GPIO4	GPIO4 pin. It is configurable with the default function based on CMI
38	GPIO5	GPIO5 pin. It is configurable with the default function based on CMI
39	VBOOT5	Boot strap voltage for buck boost (connect capacitor between VBOOT5 and SW5 pin)
40	VINBB	Dedicated input power pin for the Buck-Boost regulator
41	SW5	Switch pin for Buck-Boost regulator. SW5 is on the buck side of the regulator.
42	PGND	Power Ground for Buck-Boost regulator
43	SW6	Switch pin for Buck-Boost regulator. SW6 is on the boost side of the regulator.
44	VBBST	Output of the buck boost stage. Boost followed by a step-down stage
45	VBOOT6	Boot strap voltage for Buck-Boost (connect capacitor between VBOOT6 and SW6 pin)
46	GPIO3	GPIO3 pin. It is configurable with the default function based on CMI. Typically used for nIRQ.
47	GPIO2	GPIO2 pin. It is configurable with the default function based on CMI. Typically use for nRESET.
48	VFB1	Output and feedback pin for Buck1 regulator
49	VIN1	Dedicated input power input to Buck1 regulator
50	SW1	Switch pin for Buck1 regulator
51	PGND	Power Ground
52	SW2	Switch pin for Buck2 regulator
53	VIN2	Dedicated input power input to Buck2 regulator
54	SW4	Switch pin for Buck4 regulator
55	PGND	Power Ground
56	SW3	Switch pin for Buck3 regulator
Exposed Pad	EP	Exposed Pad. Must be soldered to PGND on PCB.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
All Pins to GND unless stated otherwise below	-0.3 to 6.0	V
AVIN to AGND	-0.3 to 18	V
VCC5 to AGND	-0.3 to 6.0	V
SW7 to PGND	-1.0 to AVIN + 1.0	V
VIN1,2,3,4 to PGND	-0.3 to 16.0	V
SW1,2,3,4 to PGND	-1.0 to VIN1,2,3,4 + 1.0	V
VBOOT1,2,3,4 to SW1,2,3,4 (VBOOT1 to SW1, VBOOT2 to SW2 etc.)	-0.3 to SW1,2,3,4 + 6.0	V
VFB1,2,3,4 to AGND	-0.3 to 6.0	V
VINBB to PGND	-0.3 to 16.0	V
VBBST to PGND	-0.3 to 16.5	V
SW5 to PGND	-1.0 to VINBB + 1.0	V
SW6 to PGND	-1.0 to VBBST + 1.0	V
VBOOT5 to SW5	-0.3 to SW5 + 6.0	V
VBOOT6 to SW6	-0.3 to SW6 + 6.0	V
SCL, SDA to AGND	-0.3 to 6.0	V
GPIO1,2,3,4,5,6,7 to AGND	-0.3 to 6.0	V
AGND, PGND	-0.3 to + 0.3	V
Junction to Ambient Thermal Resistance (Note 2)	20	°C/W
Junction to Case Thermal Resistance (Note 2)	2.3	°C/W
Operating Junction Temperature	-40 to 150	°C
Storage Temperature	-55 to 150	°C
V_{ESD}, Electrostatic Discharge, Human Body Model (HBM) per JEDEC JS-001	2000	V
V_{ESD}, Electrostatic Discharge, Charged Device Model (CDM) per JEDEC JS-002.	500	V

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: Measured on Qorvo Evaluation Kit

RECOMMENDED OPERATING CONDITIONS

PARAMETER	Value	UNIT
All Pins to GND unless stated otherwise below	0 to 5.0	V
AVIN to AGND	5.0 to 12.0	V
VCC5 to AGND	5.0	V
SW7 to PGND	-0.8 to AVIN + 0.8	V
VIN1,2,3,4 to PGND	5.0 to 12.0	V
SW1,2,3,4 to VIN1,2,3,4 (SW1 to VIN1, SW2 to VIN2 etc.)	-0.8 to VIN1-4 + 0.8	V
VBOOT1,2,3,4 to SW1,2,3,4 (VBOOT1 to SW1, VBOOT2 to SW2 etc.)	0 to SW1-4 + 5.0	V
VFB1,2,3,4 to AGND	0.6 to 5.0	V
VINBB to PGND	5.0 to 12.0	V
VBBST to PGND	1.8 to 16.0	V
SW5 to PGND	-0.8 to VINBB + 0.8	V
SW6 to PGND	-0.8 to VBBST + 0.8	V
VBOOT5 to SW5	0 to SW5 + 5.0	V
VBOOT6 to SW6	0 to SW6 + 5.0	V
SCL, SDA to AGND	0 to 5.0	V
GPIO1,2,3,4,5,6,7 to AGND	0 to 5.0	V
AGND, PGND	0	V
Operating Junction Temperature	-10 to 105	°C

ELECTRICAL CHARACTERISTICS: GENERAL PURPOSE I/O

(VIO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1,2,3,4,5,6,7 Input Low (V_{IL})	V_{VIO} = 1.8V			0.35	V
GPIO1,2,3,4,5,6,7 Input High (V_{IH})	V_{VIO} = 1.8V	1.25			V
GPIO1,2,3,4,5,6,7 Input Low (V_{IL})	V_{VIO} = 3.3V			0.5	V
GPIO1,2,3,4,5,6,7 Input High (V_{IH})	V_{VIO} = 3.3V	1.65			V
GPIOx Open Drain Leakage Current.	Pulled up to 5V			1	µA
GPIOx Open Drain Output Low.	I_{OL} = 1mA			0.35	V
GPIO2,3,4,5 Output Low, (V_{OL})	I_{OL} = 0.25mA, CMOS or push-pull output configuration.			0.35	V
GPIO2,3,4,5 Output High, (V_{OH})	I_{OH} = 0.25mA, CMOS or push-pull output configuration.	V_{VIO}-0.35			V
GPIOx Deglitch Time (falling)	Note 1		20		µs
GPIOx Deglitch Time (rising)	Note 1		10		µs
VIO Operating Range	Note 2	1.6		5.0	V
GPIOx, Pull up resistor to VIO, GPIOx = GPIO1,2,3…7.	Note3		200		kΩ

Note 1: Guaranteed by design only

Note 2: VIO is the reference level for GPIOs when configured as open drain outputs or as inputs.

Note 3: GPIO1 has option to connect internal pullup resistor to VCC5.

ELECTRICAL CHARACTERISTICS - SYSTEM CONTROL

(VIN = 12V, VCC5 = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
AVIN, VIN1,2,3,4 Input Voltage Range	HV Input pin, typical pin voltage, PMIC power from VIN1.	2.7		14.4	V
VIN1,2,3,4 Input UV Threshold, rising	VIN > VIN_UV (Rising) turns on regulators		2.9		V
VIN1,2,3,4 Input UV Threshold, falling	VIN < VIN_UV (Falling) turns off regulators		2.7		V
VIN1,2,3,4 Input UV Threshold, hysteresis		0.1	0.2	0.3	V
VIN1,2,3,4 Input UV detection deglitch time			100		µs
VIN1,2,3,4 Input OV Threshold, rising	VINOV_SEL = 0	-4%	5.8	+4%	V
	VINOV_SEL = 1	-4%	15.0	+4%	V
VIN1,2,3,4 Input OV Threshold, hysteresis	As percentage of VINx voltage		3		%
AVIN Input OV Threshold, rising (Note 2)	VINOV_SEL = 0	-5%	6.15	+5%	V
	VINOV_SEL = 1	-5%	16.0	+5%	V
AVIN Input OV Threshold, hysteresis.	percentage of AVIN Input OV voltage threshold		3		%
VCC5 nPOR Rising Threshold	VCC5>VCC5_nPOR (Rising) allows to turn on regulators.	2.45	2.6	2.75	V
VCC5 nPOR Hysteresis	VCC5<VCC5_nPOR (Falling) turns off regulators, NVM reload.		200		mV
VIN1,2,3,4 Input OV detection deglitch time.	(Note 1)		100		µs
VINBB Input Voltage Range		2.7		14.4	V
VINBB Input UV Threshold, rising			3.0		V
VINBB Input UV Threshold, falling			2.8		V
VINBB Input UV Threshold, hysteresis			0.2		V
VINBB Input UV detect deglitch time	(Note 1)		100		µs
VINBB Input OV Threshold, rising (Not user adjustable)	VIN_OV_OPT = 0	-6%	5.8	+6%	V
	VIN_OV_OPT = 1	-6%	15.0	+6%	V
VINBB Input OV Threshold, hysteresis	percentage of VINBB rising OV threshold		3		%
VINBB Input OV detect deglitch time	(Note 1)		100		µs
AVIN UV Threshold Rising. AVIN rising threshold triggers the power on sequence.	VINMON [2:0] = 000.		3.0		V
	VINMON [2:0] = 001		3.2		V
	VINMON [2:0] = 010		3.4		V
	VINMON [2:0] = 011		3.6		V
	VINMON [2:0] = 100		3.8		V
	VINMON [2:0] = 101		4.0		V

	VINMON [2:0] = 110	8.0		V
	VINMON [2:0] = 111	9.0		V
AVIN UV Warning Interrupt Threshold Falling (tracks rising threshold)	VINMON [2:0] = 000.	2.8		V
	VINMON [2:0] = 001	3.0		V
	VINMON [2:0] = 010	3.2		V
	VINMON [2:0] = 011	3.4		V
	VINMON [2:0] = 100	3.6		V
	VINMON [2:0] = 101	3.8		V
	VINMON [2:0] = 110	7.0		V
	VINMON [2:0] = 111	8.0		V
AVIN UV Shutdown Threshold	AVIN voltage below which regulators are forced to shut down		2.7	V
AVIN, Operating Supply Current	All Regulators Enabled but no load, buck-boost regulator is disabled. Low power mode enabled.	300	400	µA
	All Regulators Enabled but no load, buck-boost regulator is disabled. Low power mode disabled.	2.15		mA
	AVIN=5.0V, VCC5 = 5.0V, All Regulators Enabled but no load, buck-boost regulator is disabled. Bypass [] = 1. Low power mode enabled.	520	680	µA
	AVIN=5.0V, VCC5 = 5.0V, All Regulators Enabled but no load, buck-boost regulator is disabled. Bypass [] = 1. Low power mode disabled.	3.2		mA
AVIN, Operating Supply Current	All Regulators Enabled but no load, buck-boost regulator is enabled with no load. Low power mode enabled.	800	1200	µA
	All Regulators Enabled but no load, buck-boost regulator is enabled with no load. Low power mode disabled.	2.25		mA
AVIN, Operating Supply Current	One HV Regulator turned ON. Buck-Boost regulator is disabled. Low power mode enabled for HV Regulator and VCC5 regulator.	150		µA
	One HV Regulator turned ON. Buck-Boost regulator is disabled. Low power mode disabled for HV Regulator and VCC5 regulator.	0.85		mA
AVIN, Operating Supply Current	AVIN=12V, VCC5 = 5.0V. All other regulators disabled. Low power mode enabled.	100		µA
	AVIN=12V, VCC5 = 5.0V. All other regulators disabled. Low power mode disabled.	450		µA
	AVIN=5.0V, VCC5 = 5.0V. All other regulators disabled. Bypass [] =1	100		µA

Thermal Warning Temperature	Temperature rising		125		°C
Thermal Warning Hysteresis			25		°C
Thermal Shutdown Temperature	Temperature rising		155		°C
Thermal Shutdown Hysteresis			25		°C
Thermal Shutdown Deglitch (Note 1)	Enable and disable timing	75	100	125	µs
Power Up Delay after initial AVIN ramp.	Time from AVIN > AVIN UV rising threshold to PG for first regulator (Bucks). (zero delay setting)		2000		µs
Transition time from Deep Sleep (DPSLP) State to Active State	Time from PWREN pin low to high transition (exit DPSLP State) to time when the first regulator turns ON with minimum turn on delay configuration.		600		µs
Transition time from Sleep State (SLEEP) to Active State	Time from I²C command to clear SLEEP EN register bit (exit SLEEP state) to time when the first regulator turns ON with minimum turn on delay configuration.		600		µs
Regulator Programmable Startup Delay Timings between turn on events.	ONDLY=000 ONDLY=001 ONDLY=010 ONDLY=011 ONDLY=100 ONDLY=101 ONDLY=110 ONDLY=111		0 0.25 0.5 1 2 4 8 16		ms
Regulator Programmable Turn Off Delay	Configurable in 1ms steps between 0ms to 15ms	0		15	ms
nRESET, Delay Timings	Configurable to 20, 40, 60 or 100ms.	20		100	ms
Retry time after entering UVOVFLT state	Time when all regulators are forced off before trying ON sequence again		100		ms
Watch dog timer	Monitors I²C inactivity and time out function		8		s
Hard reset wait timer	Hard reset turns off the regulators, waits in the reset state for a “hard-reset time delay” and restarts the on sequence.		0.5		s

Note 1: Guaranteed by design only.

Note 2: When AVIN > AVIN_OV threshold, the system moves to the RESET operating state to turn-off all regulators. VCC5 regulator (Or LDO if the AVIN_OV_SEL=0) continues to function even when AVIN is higher than AVIN_OV to retain the VCC5 output and keep the PMIC powered on.

BUCK1/2 STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(VIN = 12V, VCC5 = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN1,2, Operating Input Voltage		2.7		V_{IN_OV}	V
VFB1,2, Programmable Output Voltage Range	Configurable in 20mV steps, (Note 1)	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Maximum Allowable Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, VFB1,2 = 1.2V.			6.0	A
Standby Supply Current	VFB1,2 >= 103%, Regulator Enabled, VFB1,2 = 1.8V, No Load, Low Power Mode enabled		40		µA
	Regulator Enabled, VFB1,2 = 1.8V, No Load. Lower Power Mode Disabled		410		
Shutdown Current	Regulator Disabled		1		µA
DC Output Voltage Accuracy	0.6V < VFB1,2 < 1.25V, I_{OUT} = 4A (Continuous Conduction, CCM)	-12.5	VNOM	12.5	mV
	VFB1,2 >= 1.25V, I_{OUT} = 4A (Continuous Conduction, CCM)	-1	VNOM	1	%
	0.6V < VFB1,2 < 1.25V, I_{OUT} = 10mA, (Discontinuous Conduction Mode, DCM) Low power mode disabled	-25	VNOM	25	mV
	VFB1,2 >= 1.25V, I_{OUT} = 10mA, Discontinuous Conduction Mode, DCM. Low power mode disabled.	-2	VNOM	2	%
	0.6V < VFB1,2 < 1.25V, No Load, Discontinuous Conduction Mode, DCM. Low power mode enabled.		VNOM+2		%
	VFB1,2 >= 1.25V, No Load, Discontinuous Conduction Mode, DCM.	0	VNOM+2	4	%
Line Regulation	VFB1,2 = 1.8V, VIN1,2 = 5.0V to 13.0V, (Continuous Conduction or CCM mode)		0.15		%
Load Regulation	VFB1,2 = 1.8V, 2.0A to 6.0A (Continuous Conduction or CCM mode)		0.1		%
Power Good Threshold / POK	VFB1,2 Rising, POK [] = 1	87	90	93	%VNOM
	VFB1,2 Falling, POK [] = 0	84	87	90	%VNOM
Power Good Hysteresis / POK	VFB1,2 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VFB1,2 Rising, relative to regulation point	107	113	117	%VNOM
Overvoltage Fault Hysteresis	VFB1,2 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency Range, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB1,2 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB1,2 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB1,2 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB1,2 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB1,2 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB1,2 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB1,2 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB1,2 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB1,2 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB1,2 = 2.5V		1.3		MHz

	Freq = 1010, VIN = 12.0V, VFB1,2 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB1,2 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB1,2 = 3.3V		1.6		MHz
	Freq = 1101, VIN = 12.0V, VFB1,2 = 3.3V		1.7		MHz
	Freq = 1110, VIN = 12.0V, VFB1,2 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB1,2 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
T_{MIN}, Minimum on Time			65	85	ns
Soft-Start Period T_{SS}	5% to 95% VNOM		1000	1500	µs
T_{start}, Time from EN to PG	Time from enable to PGOOD		1200		µs
Peak Current Limit, Cycle-by-Cycle	ILIM set = 00		6		A
	ILIM set = 01		7		A
	ILIM set = 10 (Note 3)		8		A
	ILIM set = 11 (Note 3)		9		A
Peak Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-10		10	%
Valley Current Limit, Cycle-by-Cycle	ILIM set = 00		5		A
	ILIM set = 01		6		A
	ILIM set = 10		7		A
	ILIM set = 11		8		A
Valley Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-10		10	%
LS FET reverse conduction current limit			3		A
Current Limit, Shutdown	% compared to Peak Current Limit, cycle-by-cycle	115	125	135	%
Current Limit, Warning	% compared to Peak Current Limit, cycle-by-cycle	70	80	90	%
HS FET On-Resistance	I_{SW} = 1A, V_{CC5} = 5.0V		30		mΩ
LS FET On-Resistance	I_{SW} = 1A, V_{CC5} = 5.0V		11		mΩ
SW Leakage Current (Note 2)	V_{IN} = 12.0V, V_{SW} = 0V		5		µA
	V_{IN} = 12.0V, V_{SW} = 12.0V		10		µA
Dynamic Voltage Scaling Rate	Configurable in 5mV steps		0.02		mV/us
	Configurable in 20mV steps		0.08		mV/us
Output Pull Down Resistance	Pull Down resistance is only connected when DISPLDN[] = 0 and the regulator is turned off			10	Ohms

Note 1: VFB1,2 settings of 5.25V or higher not recommended. Lifetime reliability guaranteed for output settings less than 5.25V.
Note 2: The current leakage from SW is not from Power FETs but from active circuitry associated with the SW node of the regulators.
Note 3: Applicable for VIN < 10V. Do not use these settings when VIN > 10V

BUCK3/4 STEP-DOWN DC/DC ELECTRICAL CHARACTERISTICS

(VIN = 12V, VCC5 = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN3,4 Operating Input Voltage		2.7		V_{IN_OV}	V
VFB3,4 Programmable Output Voltage Range	Configurable in 20mV steps, (Note 1)	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Maximum Allowable Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, VFB3,4 = 1.2V			4.0	A
Standby Supply Current	VFB3,4 >= 103%, Regulator Enabled, VFB3,4 = 1.8V, No Load. Low Power Mode Enabled		40		µA
	Regulator Enabled, VFB3,4 = 1.8V, No Load. Low Power Mode Disabled		410		µA
Shutdown Current	Regulator Disabled		1.0		µA
Output Voltage Accuracy	0.6V < VFB3,4 < 1.25V, I_{OUT} = 3A (Continuous Conduction, CCM)	-12.5	VNOM	12.5	mV
	VFB3,4 >= 1.25V, I_{OUT} = 3A (Continuous Conduction, CCM)	-1	VNOM	1	%
	0.6V < VFB3,4 < 1.25V, I_{OUT} = 10mA (Discontinuous Conduction Mode, DCM) Low power mode disabled	-25	VNOM	25	mV
	VFB3,4 >= 1.25V, I_{OUT} = 10mA (Discontinuous Conduction Mode, DCM) Low power mode disabled	-2	VNOM	2	%
	0.6V < VFB3,4 < 1.25V, No Load (Discontinuous Conduction Mode, DCM) Low power mode enabled		VNOM+2		%
	VFB3,4 >= 1.25V, No Load (Discontinuous Conduction Mode, DCM) Low power mode enabled	0	VNOM+2	4	%
Line Regulation	VFB3,4 = 1.8V, VIN3,4 = 5.0V to 13.0V, PWM Regulation		0.15		%
Load Regulation	VFB3,4 = 1.8V, PWM Regulation, 2.0A to 4.0A		0.10		%
Power Good Threshold / POK	VFB3,4 Rising, POK [] = 1	87	90	93	%VNOM
	VFB3,4 Fallng, POK [] = 0	84	87	90	%VNOM
Power Good Hysteresis	VFB3,4 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VFB3,4 Rising, relative to regulation point	107	113	117	%VNOM
Overvoltage Fault Hysteresis	VFB3,4 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB3,4 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB3,4 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB3,4 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB3,4 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB3,4 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB3,4 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB3,4 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB3,4 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB3,4 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB3,4 = 2.5V		1.3		MHz

	Freq = 1010, VIN = 12.0V, VFB3,4 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB3,4 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB3,4 = 3.3V		1.6		MHz
	Freq = 1101, VIN = 12.0V, VFB3,4 = 3.3V		1.7		MHz
	Freq = 1110, VIN = 12.0V, VFB3,4 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB3,4 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
T_{MIN}, Minimum on Time			65	85	ns
Soft-Start Period T_{SS}	5% to 95% VNOM		1000	1500	µs
T_{start}, Time from EN to PG	Time from enable to PGOOD		1200		µs
Peak Current Limit, Cycle-by-Cycle	ILIM set = 00		4		A
	ILIM set = 01		5		A
	ILIM set = 10		6		A
	ILIM set = 11 (Note 3)		7		A
Peak Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-10		10	%
Valley Current Limit, Cycle-by-Cycle	ILIM set = 00		3		A
	ILIM set = 01		4		A
	ILIM set = 10		5		A
	ILIM set = 11		6		A
Valley Current Limit, Cycle-by-Cycle Accuracy	At default ILIM setting	-10		10	%
LS FET reverse conduction current limit			3		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	70	80	90	%
HS FET On-Resistance	I_{SW} = 1A, V_{CC5} = 5.0V		30		mΩ
LS FET On-Resistance	I_{SW} = 1A, V_{CC5} = 5.0V		17		mΩ
SW Leakage Current (Note 2)	V_{IN} = 12.0V, V_{SW} = 0V		5		µA
	V_{IN} = 12.0V, V_{SW} = 12.0V		10		µA
Dynamic Voltage Scaling Rate	Configurable in 5mV steps		0.02		mV/us
	Configurable in 20mV steps		0.08		mV/us
Output Pull Down Resistance	Pull Down resistance is only connected when DISPLDN[ ] = 0 and the regulator is turned off			10	Ohms

Note 1: VFB3,4 settings of 5.25V or higher not recommended. Lifetime reliability guaranteed for output settings less than 5.25V.
Note 2: The current leakage from SW is not from Power FETs but from active circuitry associated with the SW node of the regulators.
Note 3: Applicable for VIN < 10V. Do not use these settings when VIN > 10V.

BUCK BOOST DC/DC REGULATOR ELECTRICAL CHARACTERISTICS:

(VBBST = 12.0V, VIN Boost = 12.5V, VCC5 = 5.0V, TA = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN Buck Boost Operating Input Voltage		2.7		$V_{VIN\_OV\_OPT}$	V
VBBST Programmable Output Voltage Range	Buck-Boost Mode, Configurable in 50mV steps	9.6	11	15.95	V
VBBST Output Step Size	Buck-Boost Mode		50		mV
VBBST Programmable Output Voltage Range	Buck Mode, $V_{BBST} < V_{INBB}*0.7$	1.0	1.8	4.175	V
VBBST Output Step Size	Buck Mode, $V_{BBST} < V_{INBB}*0.7$		25		mV
VBBST Output Voltage Accuracy, Buck boost mode.	VINBB = 12.0V, 0.4A, VBBST = 11.0V	-2		2	%
	VINBB = 12.0V, 0.1A, VBBST = 11.0V	-2		2	%
	VINBB = 12.0V, 10mA, VBBST = 11.0V	-4		4	%
	VINBB = 12.0V, 1mA, VBBST = 11.0V	-4		4	%
VBBST Output Voltage Accuracy, Boost Mode	VINBB = 5.0V, 0.4A, VBBST = 12.0V	-2		2	%
	VINBB = 5.0V, 0.1A, VBBST = 12.0V	-2		2	%
	VINBB = 5.0V, 10mA, VBBST = 12.0V	-4		4	%
	VINBB = 5.0V, 1mA, VBBST = 12.0V	-4		4	%
VBBST Output Voltage Accuracy, Buck Mode	VINBB = 12.0V, 0.4A, VBBST = 1.8V	-2		2	%
	VINBB = 12.0V, 0.1A, VBBST = 1.8V	-2		2	%
	VINBB = 12.0V, 10mA, VBBST = 1.8V	-4		4	%
	VINBB = 12.0V, 1mA, VBBST = 1.8V	-4		4	%
VBBST Operating Mode threshold	VIN rising threshold to enter buck-boost mode. BBST_THRESH = 0	7.1	7.5	7.9	V
	VIN falling hysteresis to enter boost mode. BBST_THRESH = 0		0.375		V
	VIN rising threshold to enter buck-boost mode. BBST_THRESH = 1	8.0	8.5	9	V
	VIN falling hysteresis to enter boost mode. BBST_THRESH = 1		0.425		V
Maximum Allowable Continuous Output Current	VINBB = 12.0V, 4.7µH, Switching frequency = 1.125MHz, VBBST = 11.0V.			0.60	A
	VINBB = 5.0V, 4.7µH, Switching frequency = 1.125MHz, VBBST = 12.0V.			0.60	A
	VINBB = 3.3V, 4.7µH, Switching frequency = 1.125MHz, VBBST = 12.0V.			0.43	A
	VINBB = 5.0V, 4.7µH, Switching frequency = 1.125MHz, VBBST = 1.8V.			1.85	A
I_q, Supply Current.	$VBBST_>$= 103% of regulated output voltage, Buck Boost mode, VINBB = 12V VBBST = 11.0V, No Load		620		µA
	$VBBST_>$= 103% of regulated output voltage, Boost mode, VINBB = 5V VBBST = 12.0V, No Load		630		µA
	$VBBST_>$= 103% of regulated output voltage, Buck mode, VINBB = 12V VBBST = 1.8V, No Load		570		µA
Shutdown Current	Regulator Disabled			1	µA
SW5 leakage from VINBB and VBBST (input or output) (Note 1)	SW5 = 0V, VINBB =12V		12		µA
	SW5 = 12V, VINBB =12V		20		µA
SW6 leakage from VINBB and VBBST (input or output) (Note 1)	SW6 = 0V, VBBST =12V		12		µA
	SW6 = 12V, VBBST =12V		20		µA

Line Regulation (DC)	VBBST = 12V, VIN = 3V-11V, I_{out} = 200mA.		0.10		%
Load Regulation	VBBST = 12.0V, VIN = 5.0V, 0.1A to 0.5A.		0.15		%
Power Good Threshold	VBBST Rising, relative to regulation point	81	86	91	%VNOM
Power Good Hysteresis	VBBST Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VBBST Rising, relative to regulation point	107	112	117	%VNOM
Overvoltage Fault Hysteresis	VBBST Falling, relative to regulation point		3		%VNOM
Switching Frequency, CCM - Continuous Conduction Mode.	VIN = 5.0V, VBBST = 12.0V, HALF_FRE=1	-10%	562.5	+10%	kHz
	VIN = 5.0V, VBBST = 12.0V, HALF_FRE=0	-10%	1125	+10%	kHz
SW5 and SW6 minimum ON-Time	(Note 2)		130		ns
Fixed SW5 duty cycle in buck boost mode.	9.6V < VBBST < 10.4V, based on VBBST output settings		60		%
	10.4V < VBBST < 11.2V, based on VBBST output settings		65		%
	11.2V < VBBST < 13.6V, based on VBBST output settings		70		%
	13.6V < VBBST < 15.95V, based on VBBST output settings		80		%
Soft-Start Period T_{SS}	5% to 95% VNOM, VBBST = 12.0V		10		ms
VINBB to SW5 FET Current Limit Settings, Cycle-by-Cycle	ILIM set = 00		1.2		A
	ILIM set = 01		1.7		A
	ILIM set = 10		2.1		A
	ILIM set = 11, Boost Mode		2.5		A
Current Limit Accuracy	At default current limit settings	-15		+15	%
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	110	122.5	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	70	80	90	%
HS1 FET On-Resistance	I_{SW} = 0.5A, VINBB = 12.0V, V_{CC5} = 5.0V,		110		mΩ
HS2 FET On-Resistance	I_{SW} = 0.5A, VINBB = 12.0V, V_{CC5} = 5.0V,		110		mΩ
LS1 FET On-Resistance	I_{SW} = 0.5A, VINBB = 12.0V, V_{CC5} = 5.0V,		100		mΩ
LS2 FET On-Resistance	I_{SW} = 0.5A, VINBB = 12.0V, V_{CC5} = 5.0V,		120		mΩ
Output Pull Down Resistance	Pull Down resistance is only connected when DISPLDN[ ] = 0 and the regulator is turned off		20		Ohms

Note 1: The current leakage from SW is not from Power FETs but from active circuitry associated with the SW node of the regulators.
Note 2: Guaranteed by design.

BUCK1/2 STEP-DOWN DC/DC – 2 PHASE OPERATION ELECTRICAL CHARACTERISTICS

(Parallel Mode for 2-phase operation, VIN1,2 = 12.0V, VCC5 = 5.0V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN1,2 Operating Input Voltage		2.7		V_{IN_OV}	V
VFB1 Programmable Output Voltage Range	Configurable in 20mV steps	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	V
Maximum Allowable Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, VFB1,2 = 1.2V.			12.0	A
Standby Supply Current	VFB1 >= 103%, Regulator Enabled, VFB1 = 1.8V, No Load. Low Power Mode Enabled.		80		µA
	Regulator Enabled, VFB1 = 1.8V, No Load. Low Power Mode Disabled.		820		µA
Shutdown Current	Regulator Disabled		2.0		µA
Output Voltage Accuracy	0.6V < VFB1 < 1.25V, I_{OUT} = 6A (Continuous Conduction, CCM)	-12.5	VNOM	12.5	mV
	VFB1 >= 1.25V, I_{OUT} = 6A (Continuous Conduction, CCM)	-1	VNOM	1	%
	0.6V < VFB1 < 1.25V, I_{OUT} = 10mA, (Discontinuous Conduction Mode, DCM) Low Power Mode Disabled	-25	VNOM	25	mV
	VFB1 >= 1.25V, I_{OUT} = 10mA (Discontinuous Conduction Mode, DCM) Low Power Mode Disabled	-2	VNOM	2	%
	0.6V < VFB1 < 1.25V, No Load (Discontinuous Conduction Mode, DCM) Low Power Mode Enabled		VNOM+2		%
	VFB1 >= 1.25V, No Load (Discontinuous Conduction Mode, DCM) Low Power Mode Enabled		VNOM+2	4	%
Line Regulation	VFB1 = 1.8V, VIN1,2 = 5.0V to 13.0V, PWM Regulation		0.15		%
Load Regulation	VFB1 = 1.8V, PWM Regulation, 4.0A to 8.0A		0.1		%
Power Good Threshold / POK	VFB1 Rising, POK [ ] = 1	87	90	93	%VNOM
	VFB1 Falling, POK [ ] = 0	84	87	90	%VNOM
Power Good Hysteresis	VFB1 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VFB1 Rising, relative to regulation point	107	113	117	%VNOM
Overvoltage Fault Hysteresis	VFB1 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB1 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB1 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB1 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB1 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB1 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB1 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB1 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB1 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB1 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB1 = 2.5V		1.3		MHz
	Freq = 1010, VIN = 12.0V, VFB1 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB1 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB1 = 3.3V		1.6		MHz
	Freq = 1101, VIN = 12.0V, VFB1 = 3.3V		1.7		MHz

	Freq = 1110, VIN = 12.0V, VFB1 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB1 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
Soft-Start Period T_{SS}	5% to 95% VNOM		1000	1500	µs
T_{start}, Time from EN to PG	Time from enable to PGOOD		1200		µs
Peak Current Limit (per phase), Cycle-by-Cycle	ILIM set = 00, per single phase		6		A
	ILIM set = 01, per single phase		7		A
	ILIM set = 10, per single phase (Note 2)		8		A
	ILIM set = 11, per single phase (Note 2)		9		A
Peak Current Limit, Cycle-by-Cycle Accuracy (per phase)	At default ILIM setting	-10		10	%
Valley Current Limit (per phase), Cycle-by-Cycle	ILIM set = 00		5		A
	ILIM set = 01		6		A
	ILIM set = 10		7		A
	ILIM set = 11		8		A
Valley Current Limit (per phase), Cycle-by-Cycle Accuracy	At default ILIM setting	-10		10	%
LS FET reverse conduction current limit (per phase)			3		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	70	80	90	%
HS On-Resistance, phase 1	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		30		mΩ
LS On-Resistance, phase 1	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		11		mΩ
HS On-Resistance, phase 2	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		30		mΩ
LS On-Resistance, phase 2	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		11		mΩ
SWx Leakage Current (Note 1)	V_{IN} = 12.0V, V_{SWx} = 0V		5		µA
	V_{IN} = 12.0V, V_{SWx} = 12.0V		10		µA
Dynamic Voltage Scaling Rate	Configurable in 5mV steps		0.02		mV/us
	Configurable in 20mV steps		0.08		mV/us
Output Pull Down Resistance	Pull Down resistance is only connected when DISPLDN[] = 0 and the regulator is turned off			10	Ohms

Note 1: The current leakage from SW is not from Power FETs but from active circuitry associated with the SW node of the regulators.
Note 2: Applicable for VIN < 10V. Do not use these settings when VIN > 10V

BUCK3/4 STEP-DOWN DC/DC – 2 PHASE OPERATION ELECTRICAL CHARACTERISTICS

(Parallel Mode for 2-phase operation, VIN1,2 = 12.0V, VCC5 = 5.0V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN3,4 Operating Input Voltage		2.7		V_{IN_OV}	V
VFB3 Programmable Output Voltage Range	Configurable in 20mV steps	0.6		5.26	V
	Configurable in 5mV steps	0.6		1.875	
Maximum Allowable Continuous Output Current	DC current output, 0.47µH, Switching frequency = 1.0MHz, VFB3 = 1.2V.			8.0	A
Standby Supply Current, Low Power Mode Enabled	VFB3 >= 103%, Regulator Enabled, VFB3 = 1.8V, No Load. Low Power Mode Enabled.		80		µA
	Regulator Enabled, VFB3 = 1.8V, No Load. Low Power Mode Disabled.		820		µA
Shutdown Current	Regulator Disabled		2		µA
Output Voltage Accuracy	0.6V < VFB1 < 1.25V, I_{OUT} = 6A (Continuous Conduction, CCM)	-12.5	VNOM	12.5	mV
	VFB1 <= 1.25V, I_{OUT} = 6A (Continuous Conduction, CCM)	-1	VNOM	1	%
	0.6V < VFB1 < 1.25V, I_{OUT} = 10mA, (Discontinuous Conduction Mode, DCM) Low Power Mode Disabled	-25	VNOM	25	mV
	VFB1 <= 1.25V, I_{OUT} = 10mA (Discontinuous Conduction Mode, DCM) Low Power Mode Disabled	-2	VNOM	2	%
	0.6V < VFB1 < 1.25V, No Load (Discontinuous Conduction Mode, DCM) Low Power Mode Enabled		VNOM+2		%
	VFB1 >= 1.25V, No Load (Discontinuous Conduction Mode, DCM) Low Power Mode Enabled		VNOM+2	4	%
Line Regulation	VFB3 = 1.8V, VIN3,4 = 5.0V to 13.0V, PWM Regulation		0.15		%
Load Regulation	VFB3 = 1.8V, PWM Regulation, 4.0A to 8.0A		0.10		%
Power Good Threshold / POK	VFB3 Rising, POK [ ] = 1	87	90	93	%VNOM
	VFB3 Falling, POK [ ] = 0	84	87	90	%VNOM
Power Good Hysteresis	VFB3 Falling, relative to regulation point		3		%VNOM
Overvoltage Fault Threshold	VFB3 Rising, relative to regulation point	107	113	117	%VNOM
Overvoltage Fault Hysteresis	VFB3 Falling, relative to regulation point		3		%VNOM
Emulated Switching Frequency, CCM - Continuous Conduction Mode.	Freq = 0000, VIN = 12.0V, VFB3 = 1.0V		0.4		MHz
	Freq = 0001, VIN = 12.0V, VFB3 = 1.0V		0.5		MHz
	Freq = 0010, VIN = 12.0V, VFB3 = 1.0V		0.6		MHz
	Freq = 0011, VIN = 12.0V, VFB3 = 1.2V		0.7		MHz
	Freq = 0100, VIN = 12.0V, VFB3 = 1.2V		0.8		MHz
	Freq = 0101, VIN = 12.0V, VFB3 = 1.2V		0.9		MHz
	Freq = 0110, VIN = 12.0V, VFB3 = 1.8V		1.0		MHz
	Freq = 0111, VIN = 12.0V, VFB3 = 1.8V		1.1		MHz
	Freq = 1000, VIN = 12.0V, VFB3 = 1.8V		1.2		MHz
	Freq = 1001, VIN = 12.0V, VFB3 = 2.5V		1.3		MHz
	Freq = 1010, VIN = 12.0V, VFB3 = 2.5V		1.4		MHz
	Freq = 1011, VIN = 12.0V, VFB3 = 2.5V		1.5		MHz
	Freq = 1100, VIN = 12.0V, VFB3 = 3.3V		1.6		MHz
	Freq = 1101, VIN = 12.0V, VFB3 = 3.3V		1.7		MHz

	Freq = 1110, VIN = 12.0V, VFB3 = 3.3V		1.8		MHz
	Freq = 1111, VIN = 12.0V, VFB3 = 3.3V		1.9		MHz
Emulated switching frequency accuracy	At the default switching frequency setting	-20		20	%
Soft-Start Period T_{SS}	5% to 95% VNOM		1000	1500	µs
T_{start}, Time from EN to PG Current Limit (per phase), Cycle-by-Cycle	Time from enable to PGOOD		1200		µs
Peak Current Limit, Cycle-by-Cycle Accuracy (per phase)	ILIM set = 00, per single phase		4		A
	ILIM set = 01, per single phase		5		A
	ILIM set = 10, per single phase		6		A
	ILIM set = 11, per single phase (Note 2)		7		A
Peak Current Limit (per phase), Cycle-by-Cycle Accuracy Valley Current Limit (per phase), Cycle-by-Cycle	At default ILIM setting	-10		10	%
Valley Current Limit (per phase), Cycle-by-Cycle Accuracy	ILIM set = 00		3		A
	ILIM set = 01		4		A
	ILIM set = 10		5		A
	ILIM set = 11		6		A
Valley Current Limit (per phase), Cycle-by-Cycle Accuracy	At default ILIM setting	-10		10	%
LS FET reverse conduction current limit (per phase)			3		A
Current Limit, Shutdown	% compared to Current Limit, cycle-by-cycle	115	125	135	%
Current Limit, Warning	% compared to Current Limit, cycle-by-cycle	70	80	90	%
HS On-Resistance, phase 1	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		30		mΩ
LS On-Resistance, phase 1	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		17		mΩ
HS On-Resistance, phase 2	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		30		mΩ
LS On-Resistance, phase 2	I_{SW} = 1A, V_{CC5} = 5.0V, T_j < 55^{O}C		17		mΩ
SWx Leakage Current (Note 1)	V_{IN} = 12.0V, V_{SWx} = 0V		5		µA
Dynamic Voltage Scaling Rate	V_{IN} = 12.0V, V_{SWx} = 12.0V		10		µA
Dynamic Voltage Scaling Rate	Configurable in 5mV steps		0.02		mV/us
Output Pull Down Resistance	Configurable in 20mV steps		0.08		mV/us

Note 1: The current leakage from SW is not from Power FETs but from active circuitry associated with the SW node of the regulators.
Note 2: Applicable for VIN < 10V. Do not use these settings when VIN > 10V

VCC5 REGULATOR ELECTRICAL CHARACTERISTICS

(AVIN powers the VCC5 Regulator, AVIN = 12.0V, VCC5 = 5.0V, T_A = 25°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range	VCC5 Regulator input voltage	2.7		18.0	V
Output Voltage Range Linear Mode (LDO Mode)	Linear Mode Regulation voltage - LDO Mode.VCC5_SET [1:0] = 00.		4.75		V
	Linear Mode Regulation voltage - LDO Mode.VCC5_SET [1:0] = 01.		5.00		V
	Linear Mode Regulation voltage - LDO Mode.VCC5_SET [1:0] = 10.		5.10		V
	Linear Mode Regulation voltage - LDO Mode.VCC5_SET [1:0] = 11.		5.25		V
Output Voltage accuracy (LDO mode)	PMIC internal load + 250mA External Load current applied. (At default voltage setting)	-4		+4	%
Output Voltage Range PWM Mode (Buck Mode)	PWM Mode Regulation voltage. VCC5_SET [1:0] = 00. Buck Mode.		4.9		V
	PWM Mode Regulation voltage. VCC5_SET [1:0] = 01. Buck Mode.		5.0		V
	PWM Mode Regulation voltage. VCC5_SET [1:0] = 10. Buck Mode.		5.1		V
	PWM Mode Regulation voltage. VCC5_SET [1:0] = 11. Buck Mode.		5.3		V
Output Voltage accuracy (Buck mode)	PMIC internal load + 250mA External Load current applied. (At default voltage setting)	-3		3	%
Dropout voltage	Linear Mode, I = 400mA, VCC5 = 95% of regulation point.			250	mV
Maximum Output Current	AVIN = 12.0V, VCC5 = 5.0V			500	mA
	AVIN = 5.5V, VCC5 = 5.0V, LDO Mode			500	mA
Enter miniBK Mode threshold, (AVIN rising)	The threshold starts miniBK Mode		7.0		V
Exit miniBK Mode threshold, (AVIN falling)	The threshold stops miniBK Mode		6.5		V
DC Line Regulation, Steady state condition.	VCC5 = 5.0V, AVIN = 6.5V to 18V, PWM Regulation		0.20		%
	VCC5 = 5.0V, AVIN = 5.25V to 7.0V		0.10		%
DC Load Regulation, Steady state condition.	VCC5 = 5.0V, AVIN = 12.0V, Load current varied from 0.01A to 0.5A.		0.10		%
	VCC5 = 5.0V, AVIN = 5.5V, Load current varied from 0.01A to 0.5A.		0.15		%
HS PMOS on Resistance	VCC5 = 5.0V, AVIN = 12.0V		300		mΩ
LS NMOS on Resistance	AVIN = 12.0V		100		mΩ
Soft-start slew rate	Output start from 0 to 5.0V		400		µs
Current limit	Cycle-by-cycle, Buck Mode	1.6	2.0	2.4	A

	LDO Mode (Linear Mode)	0.5	0.7	1.0	A
Emulated Switching frequency	VIN1 = 12.0V, VCC5 = 5.0V, L = 1.0µH, Load = 500mA.		2.4		MHz
Startup Delay	Time from AVIN > 7.0V to PG internal signal from VCC5. Buck Mode.		500	800	µs

I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VIN_IO = 1.8V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	VIO= 1.8V			0.5	V
SCL, SDA Input High	VIO= 1.8V	1.25			V
SDA Leakage Current	SDA=V_{SYS}			0.1	µA
SDA Output Low	IOL = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note 1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Fall Time SDA, T_{off}	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns
I²C Internal Pull Up resistors	(Note 4)		10		kΩ

Notes 1: Comply to I2C timings for 1MHz operation - “Fast Mode Plus”

Notes 2. No internal timeout for I2C operations, however, I2C communication state machine will be reset when entering COLD, Sleep, OVUVFLT, and THERMAL states to clear any transactions that may have been occurring when entering the above states.

Notes 3. Device Address is configurable (0x25h, 0x27h, 0x67h, 0x6Bh)

Notes 4. Configurable to pullup to VIO or VCC5

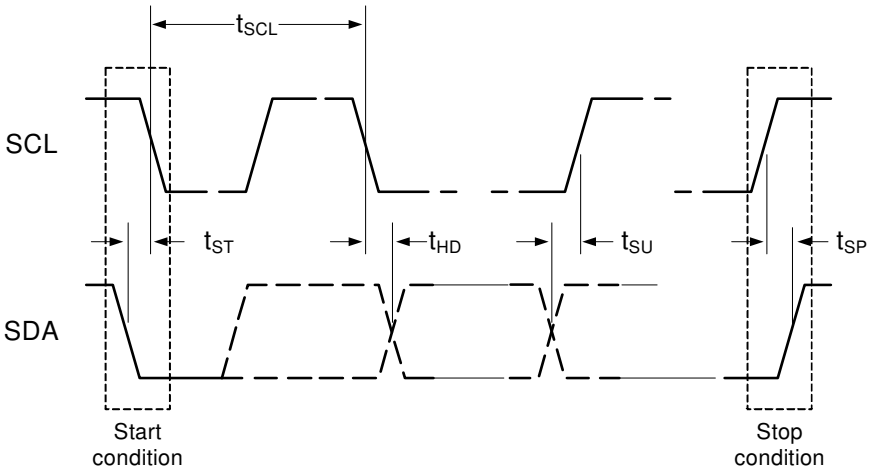


Figure 2: I²C Data Transfer

SYSTEM CONTROL INFORMATION

General

The ACT86600 PMIC is a high voltage input, single-chip, integrated power management solution. It is ideally suited to power enterprise solid state drives (SSD) and computing power and memory and storage from 12V input rails. It integrates four high voltage, high power DC/DC, two with 4A outputs and two with 6A outputs. It also has a buck-boost and an always on buck supply. It incorporates seven GPIOs to maximize system level flexibility. Its master controller manages startup sequencing, timing, voltages, slew rates, sleep states, and fault conditions. I²C configurability allows system level changes without the need for costly PCB changes.

It is highly flexible and can be reconfigured via I²C for multiple applications without the need for PCB changes. The low external component count and high configurability significantly speeds time to market. Examples of configurable options include output voltage, startup time, slew rate, system level sequencing, switching frequency, sleep modes, operating modes etc.

The high voltage step-down regulators use a proprietary control architecture that is based on a constant on-time (COT) topology. It is designed for high efficiency, has programmable switching frequency options, and is suitable for high conversion ratios to support output voltages down to 0.6V. The regulators are optimized for single stage voltage conversion from 12V input power sources.

The proprietary architecture allows the regulators to work at near constant frequency at any given operating point. In continuous conduction mode (CCM), the regulators operate at a nearly constant frequency across load. The switching frequency is selectable to allow system optimization and to accommodate a variety of inductor values and sizes. When load current is reduced and the regulators operate in discontinuous conduction mode (DCM), the IC automatically reduces switching frequency to maintain high efficiency. This results in high efficiency across the entire output current range. The quiescent current under no load conditions is minimal and also contributes to the high efficiency achieved under light loads conditions.

Buck1 and Buck2 each provide 6A outputs. These two outputs can be operated in parallel to provide a 12A, dual phase output. Buck3 and Buck4 each provide 4A outputs and can be operated in parallel to provide an 8A output.

BBST, the buck-boost converter, provides up to 0.6A. BBST can also be configured for buck only operation for lower output voltages. It is optimized for maximum efficiency with a 12V input (unregulated) to a 12V regulated output that is typical in SSD applications. The always-on supply, VCC5, is a buck converter that efficiently generates the ACT86600 internal bias supply from the system input voltage. It can also be used to power additional external circuitry.

The ACT86600 contains seven configurable GPIOS available that can be programmed to implement a variety of system functions. They can be programmed to generate interrupts - as an interrupt request pin (nIRQ pin), to control and sequence external regulators, to enable or disable internal regulators, as input lines to control entry or exit from low power states such as SLEEP and deep sleep (DPSLP) modes and other such system related functions. Two of the GPIOs can also function as current sinks to drive LEDS. The GPIOs can also be used to perform dynamic voltage scaling or DVS for the buck regulators. This function allows the user to scale the output voltage of buck regulators high during normal operation and regulate at a lower voltage to conserve power during SLEEP or DPSLP cases.

The ACT86600 master controller monitors all outputs and reports faults via I²C and hardwired status signals. Faults can be masked, and fault levels and responses are configurable via I²C.

Many of the ACT86600 pins and functions are configurable. The IC's default functionality is defined by the default CMI (Code Matrix Index), but much of this functionality can be changed via I²C. The GPIOs can be configured as enable inputs, reset outputs, dynamic voltage (DVS) inputs, LED drivers, etc. The GPIO configuration is specifically defined for each ACT86600 orderable part number. The first part of the datasheet describes basic IC functionality and default pin functions. The end of the datasheet provides the configuration and functionality specific to each CMI version. Contact Qorvo for additional information about other configurations.

I2C Serial Interface

To ensure compatibility with a wide range of systems, the ACT86600 uses standard I2C commands. The ACT86600 operates as a slave device and can be factory configured to one of four 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x25h	010 0101b	0x4Ah	0x4Bh
0x27h	010 0111b	0x4Eh	0x4Fh
0x67h	110 0111b	0xCEh	0xCFh
0x6Bh	110 1011b	0xD6h	0xD7h

There is no timeout function in the I²C packet processing state machine, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

The IC implements a special register passcode that enables I²C write transactions. This prevents accidental register changes. Enable I²C write functionality by writing a value of 0xAAh to register 0x0Ah (Unlock Register Key). Change this register to any other value to prevent accidental changes to the I²C register values.

The IC also gives the customer the ability to read the CMI version via I²C. Register 0x19h bits [7:4] contain this info.

I²C Registers

The ACT86600 contains an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, sequencing, fault thresholds, fault masks, etc. These registers are what give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings, startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please contact Qorvo for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

I²C Write Protection

The IC implements I²C write protection to prevent accidental changes to the register settings. Writing the value 0xAAh into to register 0x0Ah unlocks the registers and allows the user to modify the register settings. After completing any required configuration changes, write any value other than 0xAA into register 0x0Ah to lock the registers again.

Coding Matrix Index (CMI)

The ACT86600 contains a CMI configuration that allows tremendous flexibility. The CMI allows the ACT86600 to be configured and optimized for many different systems and applications.

The default CMI configuration can be modified via I²C commands and can therefore be altered by host processor firmware at any time. At system startup, the host processor can access the internal registers any time after VCC5 is powered up and the IC is in the RESET state. This allows the ACT86600 startup sequence and all other configurable parameters to be modified before the startup sequence begins. This enables tremendous system level flexibility.

Firmware intervention or control is not typically necessary in most cases. This is especially true if the default CMI is optimized at the factory for the system. Please contact Qorvo for custom options and minimum order quantities.

ENABLE OPERATING MODES

The ACT86600 can be factory configured into one of two modes: PWREN and Always-On. Note that these modes are factory configured and cannot be changed by the user. The Ordering Table and the CMI Options section at the end of the datasheet shows the operating mode for each CMI option.

Always-On Operating Mode

The Always-On operating mode allows the IC to automatically start the turn-on sequence when the AVIN input voltage rises above a specific threshold. Turn on does not require any GPIOs or microprocessor inputs.

The outputs automatically turn off when the input voltage drops below the threshold. The AVIN UVLO threshold is set by the AVINMON register bits REG0x0F[2:1].

Table 1: AVIN UVLO Settings

AVINMON[2:0]	AVIN UVLO Threshold (V)
000	3.0
001	3.2
010	3.4
011	3.6
100	3.8
101	4.0
110	8.0
111	9.0

PWREN Operating Mode

The PWREN operating mode requires either GPIO or microprocessor inputs to enable the outputs. If power is applied with PWREN held low, the outputs do not turn on. When PWREN is pulled high, the IC starts the turn on sequencing. If PWREN is pulled up to a logic high when input power is applied, the outputs automatically start the turn on sequencing.

A typical enable sequence is initiated when power is applied and the PWREN pin is asserted high. After power is applied to the system processor, it then holds PWREN high to keep the IC turned on. The CMI can also be configured to allow the processor to pull another GPIO high to keep the system turned on. After the system is up and running, the processor can pull PWREN low to put the IC into DPSLP mode. As with the power enable sequence, a typical disable sequence is initiated when the user de-asserts the PWREN input to enter DPSLP state.

STATE MACHINE

Figure 6 shows the internal state machine. The ACT86600 features a variety of control sequences that are optimized for supporting system power up, power down and SLEEP/STANDBY and DPSLP states. The IC has two low power states, SLEEP and DPSLP, which all the user to user configurable low power functionality to optimize system efficiency. The PMIC can be configured for many types of processors. It should also be noted that each of SLEEP or DPSLP states can be configured via I^2C to be different every time one of these modes is entered. These offer versatile low power modes that allow the system designer the possibility of emulating several low power mode combinations with a single configurable state of the PMIC.

RESET State

In the RESET state, the ACT86600 is waiting for the input voltage on AVIN to be within a valid range defined by the AVIN_UV and AVIN_OV thresholds. All regulators are off in RESET. All reset outputs are asserted low. All volatile registers are reset to defaults and Non-Volatile registers are reset to programmed defaults. The IC transitions from RESET to POWER SEQUENCE START when the input voltage enters the valid range. The IC transitions from any other state to RESET if the AVIN voltage exceeds the UV or OV thresholds. The IC also enters this state after seven attempts to restart due to an output voltage fault. It is important to note any transition to RESET returns all volatile and non-volatile registers to their default states.

POWER SEQUENCE START State

The POWER SEQUENCE START state is a transitional state while the regulators are starting. The IC does not operate in this state. The IC enters this state when it exits the RESET, SLEEP, and DPSLP states. Typical operation is to transition from POWER SEQUENCE to POWER ON. However, the customer can transition directly from POWER SEQUENCE to either SLEEP or DPSLP by setting the proper conditions to do so. These conditions are described in the SLEEP and DPSLP sections.

SLEEP State (PWREN / Always-On configuration)

The ACT86600 supports SLEEP mode operation in both the PWREN configuration and the Always-On configurations. In the PWREN configuration, the SLEEP state is accessible by I²C or a GPIO pin or both. The SLEEP state is a user configurable low power state. The IC can have default SLEEP mode settings, but the user can also modify these settings on-the-fly anytime during operation. This allows the user system to customize the SLEEP mode settings for multiple operating conditions.

When entering SLEEP state, the outputs can be programmed to regulate to VSET0 or VSET1, or they can be programmed to be turned off. The outputs immediately transition to the programmed setting when entering SLEEP state. When exiting SLEEP state, any output that was turned off will startup with its programmed turn-on delay.

The IC uses an I²C register bit, ENTER_SLEEP, default value to determine whether it can enter the SLEEP state with I²C bus or a GPIO. If ENTER_SLEEP = 0, then both I²C and a GPIO are required to enter SLEEP mode. If ENTER_SLEEP = 1, then only a GPIO input is required to enter SLEEP mode.

The I²C register bit, SLEEP_MODE, determines if SLEEP mode is entered with a logical AND of the GPIOs or a logical OR of the GPIOs and the ENTER_SLEEP bit. When SLEEP_MODE = 0, the IC uses the AND function. When it = 1, the IC uses the OR function. Note that SLEEP_MODE bit is not user configurable.

The conditions to enter and exit the SLEEP state are simplified and summarized in figure 1 and table 2

Note that an output can be programmed to go to the VSET1 voltage in either SLEEP or DPSLP mode, but not in both modes. If the output must go to the VSET1 voltage in both SLEEP and DPSLP modes, program it to go to VSET1 in SLEEP mode. Then manually change the VSET0 prior to entering DPSLP.

Table 2: SLEEP Mode Settings with SLEEP_MODE I²C Bit = 0 (AND mode)

SLEEP_EN I²C bit	ENTER_SLEEP I²C bit	GPIO1	GPIO2	Operating Mode
0	x	x	x	ACTIVE
1	x	0	0	ACTIVE
1	x	0	1	ACTIVE
1	x	1	0	ACTIVE
1	x	1	1	SLEEP

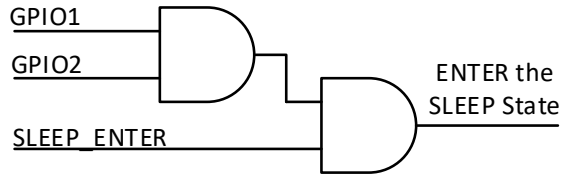


Figure 1. SLEEP State Entry Logic with SLEEP_MODE I²C Bit = 0 (AND mode)

Table 3: SLEEP Mode Settings with SLEEP_MODE I²C Bit = 1 (OR mode)

SLEEP_EN I²C bit	ENTER_SLEEP I²C bit	GPIO1	GPIO2	Operating Mode
0	x	x	x	ACTIVE
1	1	0	0	SLEEP
1	1	0	1	SLEEP
1	1	1	0	SLEEP
1	1	1	1	SLEEP

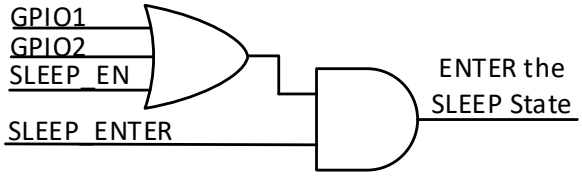


Figure 2. SLEEP State Entry Logic with SLEEP_MODE I²C Bit = 1 (OR mode)

DPSLP State (PWREN configuration)

The ACT86600 also supports a DPSLP state in both the PWREN and Always-On configurations. The conditions to enter DPSLP are different in each case. Like the SLEEP state, the DPSLP state is a user configurable low power state that has both default settings and gives the user the ability to modify these settings on-the-fly anytime during operation.

When entering DPSLP state, the outputs can be programmed to regulate to VSET0 or VSET1, or they can be turned off. The outputs immediately transition to the programmed setting when entering DPSLP state. When exiting DPSLP state, any output that was turned off will startup with its programmed turn on delay.

Note that an output can be programmed to go to the VSET1 voltage in either SLEEP or DPSLP mode, but not in both modes. If the output must go to the VSET1 voltage in both SLEEP and DPSLP modes, program it to go to VSET1 in SLEEP mode. Then manually change the VSET0 prior to entering DPSLP.

In the PWREN configuration, the DPSLP state can be entered with I²C, with the PWREN pin, or both.

The IC uses an I²C register bit, DPSLP MODE, default value to determine whether it can enter DPSLP state with I²C and the PWREN pin, or just the PWREN pin. If DPSLP MODE = 0, then entering DPSLP requires setting the I²C bit DPSLP_EN = 1 and then pulling the PWREN pin low. This option is best for systems with I²C available. If DPSLP MODE = 1, then the IC only needs the PWREN pin to enter the DPSLP state. For applications without I²C, use the DPSLP MODE = 1 setting. In this situation, the falling edge of PWREN puts the IC into the DPSLP state. Pulling PWREN high exits DPSLP state in both cases. Note that the DPSLP MODE bit is set at the factory and is not user adjustable.

While PWREN is low and the IC is in DPSLP state, if the DPSLP_EN bit gets reset due to OV/UV or THERMAL faults, the IC exits the DPSLP state and goes to the POWER ON/Active state. To re-enter DPSLP state, the PWREN pin must be toggled high then toggled back to low again to re-enter DPSLP.

The conditions to enter and exit the DPSLP state with the PWREN Configuration are simplified and summarized in figure 3 and table 3.

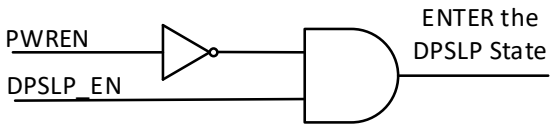


Figure 3. PWREN Configuration - DPSLP State Entry Logic with DPSLP_MODE I²C Bit = 0

DPSLP State (Always-On configuration)

In the Always-On configuration there is no PWREN. In this case DPSLP mode can be entered or exited using GPIOs or I²C or both much like the SLEEP state entry and exit. Note that the SLEEP state entry and exit is independent of the PWREN or "Always-On" configuration and the control logic to enter and exit SLEEP state is similar in both PWREN and "always on" configurations.

The DPSLP_EN bit must be set to a logic 1 before the IC enters DPSLP mode. This bit can be factory set to either a 0 or a 1. It can be overwritten by the user during operation to enable or disable DPSLP mode.

The IC uses an I²C register bit, DPSLP MODE, default value to determine whether it enters DPSLP mode with the logic "AND" or "OR" of the GPIO inputs. If DPSLP MODE = 0, the GPIOs are an "AND" function. If it = 1, then the GPIOs are an "OR" function. Note that even if the GPIOs inputs are in the correct state to enable DPSLP mode, the DPSLP_EN bit must also be set high to enter DPSLP mode.

The conditions to enter and exit the DPSLP state in the Always On Configuration are simplified and summarized in figure 4 and table 4.

Table 4: DPSLP Mode Settings with DPSLP_MODE I²C Bit = 0

DPSLP_EN I²C bit	GPIO1	GPIO2	Operating Mode
0	x	x	ACTIVE
1	0	0	ACTIVE
1	0	1	ACTIVE
1	1	0	ACTIVE
1	1	1	DPSLP

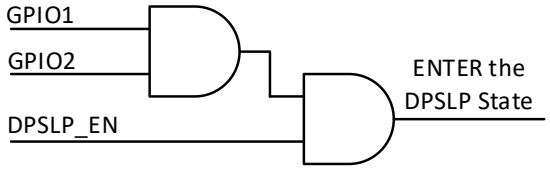


Figure 4. Always-On Configuration - DPSLP State Entry Logic with DPSLP_MODE I²C Bit = 0

Table 5: DPSLP Mode Settings with DPSLP_MODE I²C Bit = 1

DPSLP_EN I²C bit	GPIO1	GPIO2	Operating Mode
0	x	x	DPSLP
1	0	0	ACTIVE
1	0	1	DPSLP
1	1	0	DPSLP
1	1	1	DPSLP

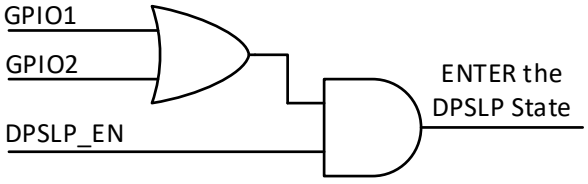


Figure 5. Always-On Configuration - DPSLP State Entry Logic with DPSLP_MODE I²C Bit = 1

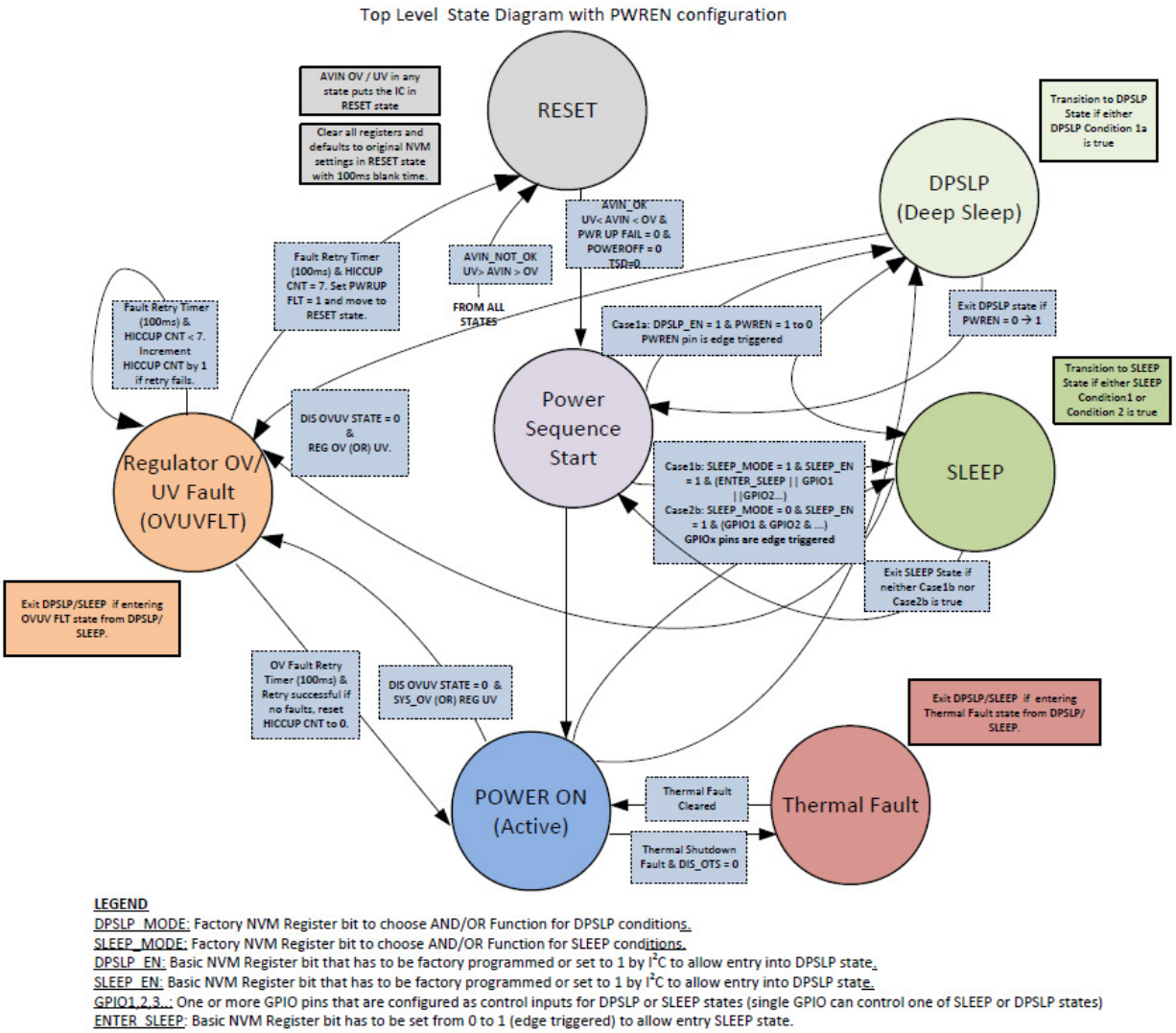


Figure 6: State Diagram with GPIO1 configured as PWREN Input

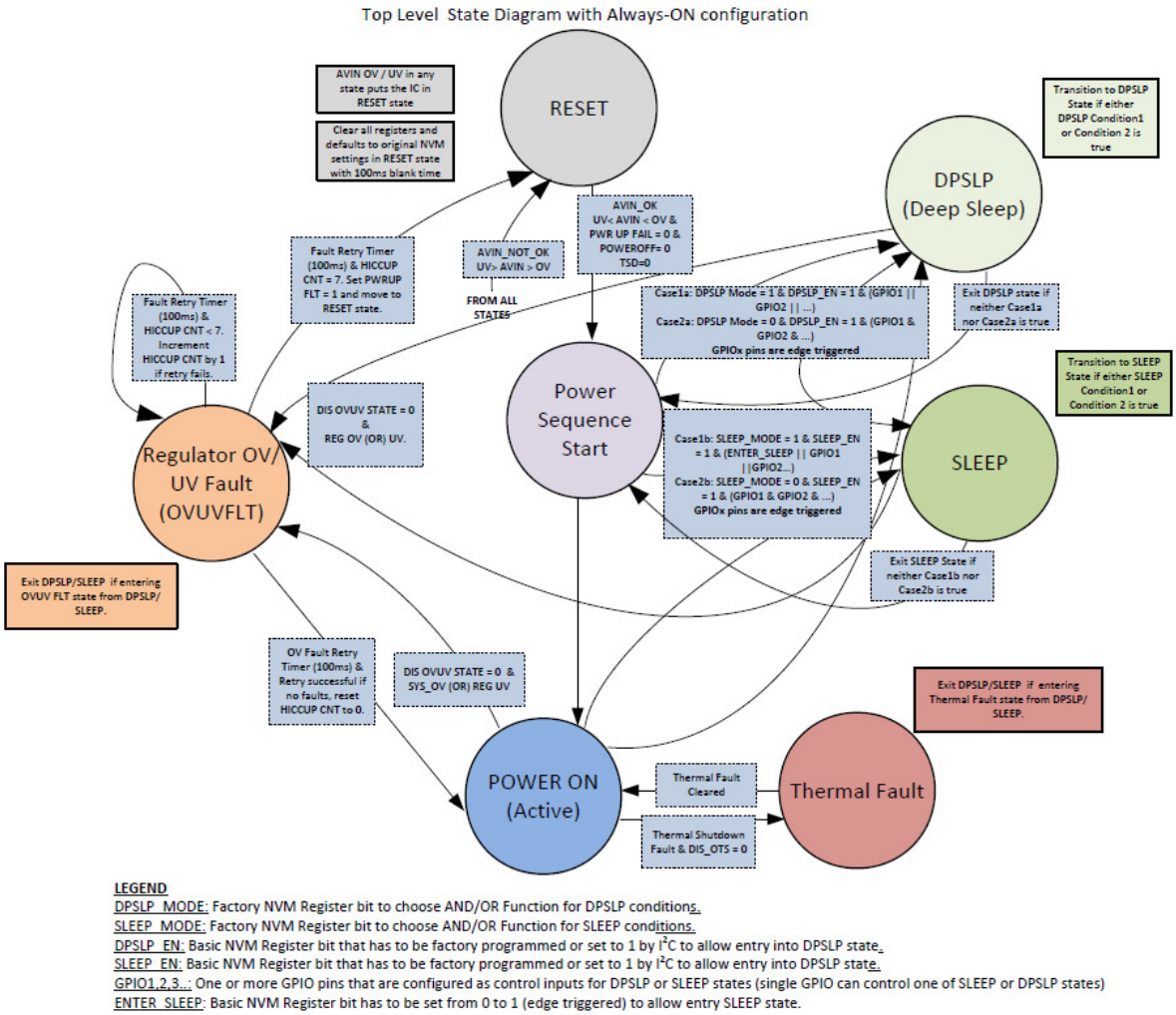


Figure 7: State Diagram without the PWREN Input pin (“always-on mode”)

THERMAL FAULT State

The ACT8660 transitions to the THERMAL FAULT State when the IC's temperature is higher than Thermal shutdown threshold (155 Deg). This is also referred to as Over Temperature Shutdown (OTS). This temperature threshold is not adjustable. In this state, all regulators are shut down.

There are two control bits that determine the behavior of all the regulators when an over temperature condition occurs. These are DIS_OTS and DIS_OTS_VCC5. DIS_OTS controls the behavior of all regulators except the VCC5 output. DIS_OTS_VCC5 only controls the VCC5 regulator.

DIS_OTS = 0, DIS_OTS_VCC5 = 0. With these setting, all outputs turn off during an OTS condition. If the loading in VCC5 is high enough to discharge the voltage below the IC's POR voltage (~2.4V) before the IC restarts, the IC restarts from the RESET State and all I²C registers reset to their default values. If VCC5 does not discharge below ~2.4V before the IC restarts, the I²C registers retain their values.

DIS_OTS = 0, DIS_OTS_VCC5 = 1. This is the typical configuration. This setting assumes that there is no external loading on the VCC5 output and the VCC5 output is intended for only powering the PMIC. With these conditions, faults on VCC5 are unlikely. When an overtemperature condition occurs, all regulators (not including VCC5) power off. They turn back on when the OTS condition clears. Note that VCC5 remains on through this process. This setting assumes that fault conditions (shorted output) on the VCC5 output are unlikely and therefore does not guarantee protection on the VCC5 output during OTS events. There is a current limit circuit that limits the VCC5 current, but VCC5 does not shut down during OTS events. In this configuration, a shorted VCC5 output that could be causing an OTS condition will cause the VCC5 output to continue to remain on through the OTS conditions.

DIS_OTS = 1, DIS_OTS_VCC5 = 0. The buck and buck-boost regulators remain on, but VCC5 turns off. When VCC5 shuts down during OTS, the VCC5 capacitor gets discharged to the undervoltage (POR) level and then an internal pre-regulator turns on to power VCC5 back up again (power cycle VCC5 and the PMIC). The internal pre-regulator has a pull up or charging current limit of 40mA typically and is turned on after the POR level has been reached during discharge of the VCC5 output.

DIS_OTS = 1, DIS_OTS_VCC = 1. The IC does not enter OTS and all outputs stay on.

If the mini-buck regulator is not used and AVIN is supplied with an external 5V supply, VCC5 is just a bypassed output from AVIN. DIS_OTS_VCC5 should be set to 1 so VCC5 is not turned off during the OTS.

Note that the DIS_OTS and DIS_OTS_VCC5 bits are not user configurable.

FUNCTIONAL DESCRIPTION

The ACT86600 is a feature rich IC that provides a lot of system level flexibility. The sections below describe the different IC functions.

Sequencing

The ACT86600 provides the end user with extremely versatile sequencing capability that can be optimized for many different applications. Each of the five outputs (not including VCC5) has four basic sequencing parameters: input trigger, turn-on delay, turn-off delay, and output voltage. Each of these parameters is controlled via the ICs internal registers.

The ACT86600 can use its GPIOs to control external regulators which allows it to seamlessly integrate additional external power supplies into the overall startup sequencing. This allows the PMIC to behave like a single but larger power management system by controlling both internal and external regulators. The GPIOs can also managing low power modes such as the SLEEP and DPSLP states which eliminates the need for external logic or microcontrollers that may otherwise be needed for system power management or safety monitoring.

The default settings are controlled by the IC's CMI, which is shown at the end of this datasheet. Contact Qorvo for custom sequencing configurations. Refer to the Qorvo Application Note, AN119, ACT86600 Register Definitions, for full details on the I²C register map functionality and programming ranges.

Input trigger. The input trigger for a regulator is the event that turns that regulator on. Each output can have a separate input trigger. The input trigger can be the internal power ok (POK) signal from one of the other regulators, the internal VIN POK signal, or an external signal applied to a GPIO pin. This flexibility allows a wide range of sequencing possibilities, including having some of the outputs be sequenced with an external power supply or a control signal from the host. As an example, if the Buck2 input trigger is Buck1, Buck2 will not turn on until Buck1 is in regulation. Input triggers are defined at the factory and can only be changed with a custom CMI configuration. The GPIOx outputs can be connected to an internal power supply's POK signal and used to trigger external supplies in the overall sequencing scheme. The GPIOx inputs can also be connected to an external power supply's power good output and used as an input trigger for an ACT86600 supply.

Turn-on Delay. The turn-on delay is the time between an input trigger going active and the output starting to turn on. Each output's turn-on delay is configured via its I²C bit ON DELAY. Turn-on delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Turn-off Delay. The turn-off delay is the time between an input trigger going inactive and the output starting to turn off. Each output's turn-off delay is configured via its I²C bit OFF DELAY. Turn-off delays can be changed after the IC is powered on, but they are volatile and reset to the factory defaults when power is recycled.

Softstart Time. The softstart time is the time it takes an output to ramp from 5% to 95% of its programmed voltage. All HV Buck converters have a fixed 1ms softstart time. The Buck-boost has a fixed 10ms softstart time. The VCC5 output has a fixed 1ms softstart time.

Output Voltage. The output voltage is each regulator's desired voltage. Each output voltage (not including the VCC5 output) is programmed via its I²C bits VSET0 and VSET1. The output regulates to VSET0 in ACTIVE mode. They can be programmed to regulate to VSET1 in DVS, SLEEP, and DSPSLP modes. The VCC5 output voltage is controlled by the VCC5_SET register. Each output's voltage can be changed after the IC is powered on, but the new setting is volatile and is reset to the factory defaults when power is recycled. Output voltages can be changed on the fly. If a large output voltage change is required, it is best to make multiple smaller changes. This prevents the IC from detecting an instantaneous over or under voltage condition because the fault thresholds are immediately changed, but the output takes time to respond.

Dynamic Voltage Scaling

On-the-fly dynamic voltage scaling (DVS) is available for the four buck regulators and the buck-boost regulator. The VCC5 output does not have DVS capability. DVS can be implemented with either the I²C interface or a GPIO. DVS allows systems to save power by quickly adjusting the microprocessor performance level when the workload changes. Note that DVS is not a different operating state. DVS is just a different output voltage in while the IC operates in the ACTIVE state. Each buck converter operates at its VOUT0 voltage in normal operation and operates at its VOUT1 voltage when the DVS input trigger is active. DVS can be implemented in four ways.

The first method is to individually put each buck converter in DVS by manually writing a new voltage regulation setpoint into its VOUT0 register.

The second method implements DVS for all buck converters at one time via a single GPIO input. The IC's

specific CMI determines the specific GPIO used for DVS. This setting can be modified with a custom CMI.

The third method implements DVS for all buck converters at one time via I²C. This function requires EN_DVS_I2C = 1. Then enable DVS via a single I²C write to one of the three following bits:

DVS_FROM_I2C_DB9

DVS_FROM_I2C_DB10

DVS_FROM_I2C_DB11

The specific bit required to enter DVS is determined by each IC's CMI settings.

The fourth method enables DVS when the IC enters the SLEEP state. When GB_SLEEP_CONTROL_DB9 = 1, then any condition that puts the IC into the SLEEP state also puts the IC into DVS mode.

For fault free operation, the user must ensure output load conditions plus the current required to charge the output capacitance during a DVS rising voltage condition does not exceed the current limit setting of the regulator. As with any power supply, changing an output voltage too fast can require a current higher than the current limit setting. The user must ensure that the voltage step, slew rate, and load current conditions do not result in an instantaneous loading that results in a current limit condition.

Note that the EN_DVS_BY_I2C and GB_SLEEP_CONTROL_DB9 bits are not user configurable.

Enable / Disable Control

During normal operation, each output may be enabled or disabled via the I²C interface or a GPIO. The specific I²C command or GPIO is CMI specific. Note that disabling a regulator that is used as an input trigger to another regulator may or may not disable the other regulators following it, depending on the specific CMI settings. Contact Qorvo if different functionality is needed. Each output has a load discharge function designed to quickly pull the output voltage to ground when the converter is disabled. The circuit connects an internal resistor (10ohm for Buck1,2,3,4 and 20ohms for the buck-boost) from the output to PGND when the converter is disabled.

Input Voltage Monitoring (SYSMON)

The ACT86600 monitors the voltage on the AVIN pin. The AVIN pin can be connected to one of the VINx input pins and the IC will monitor both over voltage and undervoltage conditions. Based on the IC's configuration, if AVIN reaches the UV or OV thresholds, the IC either shuts down the ACT86600 or asserts the nRESET pin low. The SYSMON function is intended to monitor the system's input voltage and alert the system when the supply voltage drops below a configurable threshold voltage before but is still above minimum allowable operating voltage. It also detects overvoltage conditions and either shuts down or alerts the system by pulling nRESET low.

Fault Protection

The ACT86600 contains several levels of fault protection, including the following:

Output Overvoltage

Output Undervoltage

Output Current Limit and short circuit

Thermal Warning

Thermal Shutdown

There are three types of I²C register bits associated with each fault condition: fault flag bits, fault bits, and mask bits. The fault flag bits display the real-time fault status. Their status is valid regardless of the fault mask bit setting. The mask bits either block or allow the fault to affect the fault bit. Each potential fault condition can be masked via I²C if desired. Any unmasked fault condition results in the fault bit going high, which asserts the nIRQ pin. nIRQ is typically active low. The nIRQ pin only de-asserts after the fault condition is no longer present and the corresponding fault bit is read via I²C. Note that masked faults can still be read in the fault flag bit. Refer to the Qorvo Application Note describing the Register Map for full details on I²C functionality and programming ranges.

nIRQ (Interrupt)

The interrupt function is typically used to drive the interrupt input of the system processor. Many of the ACT86600's functions support interrupt-generation as a result of various conditions. These are typically masked by default but may be unmasked via the I²C interface. For more information about the available fault conditions, refer to the appropriate sections of this datasheet. nIRQ can be triggered from:

1. Die temperature warning
2. Any regulator exceeding peak current limit for 16 cycles after soft start or a UV/OV condition.
3. Input goes above OVP threshold or falls below the UV threshold
4. Watch Dog timer expiring

If any of these faults occur the nIRQ output is asserted active low. After nIRQ pin is asserted, an I²C read of the interrupt status registers clears the interrupt provided the interrupting condition is removed. If the interrupting condition is still present, nIRQ stays asserted and the interrupt status bit stays set.

The ICs specific CMI determines which GPIOx is used for the nIRQ pin. nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor.

nRESET

The ACT86600 provides a reset function to issue a master reset to the system CPU/controller. nRESET is immediately asserted low when either the VINx or AVIN voltage is above or below the UV or OV thresholds or any power supply that is connected to the nRESET functionality goes below its Power Good threshold.

The input to the nRESET signal is typically tied to all regulators whose outputs are necessary for the system controller and I/O signals to function properly. Configurable register bits in each regulator determine if that regulator's POK signal controls the nRESET signal. In general, the behavior of the nRESET output is such that the nRESET output is low if any one of the Power Okay (POK) signals from the controlling regulators is low. In other words, if any one of the controlling regulator outputs is not okay, the nRESET output is asserted low. A regulator's POK signal can be low (not asserted) when the regulator is enabled and the output is not in regulation. Disabled regulators do not affect the nRESET signal, even if its POK signal is configured to control the nRESET output. This is because, a disabled regulator's POK signal is disabled and held high. A regulator's POK signal becomes active low when the regulator is enabled. It stays low during softstart until the output voltage reaches 90% of the target regulation voltage.

The ACT86600 generates an internal reset signal, nRESETI. nRESETI is the logical equivalent of the functional "AND" of all the regulator POK signals that are set to control the nRESET output. When a regulator that is tied to the nRESET output is enabled, its POK signal typically goes low for the time between its enable signal going high to the time its output voltage reaches ~90% of the target output voltage. During this time, the nRESETI signal also goes low. On every rising transition of the nRESETI signal, a timer is started to wait for a delay set by the RST_DLY [] control bits. This nRESET delay can be 20, 40, 60 or 100ms. The nRESET output is a de-glitched version of nRESETI. nRESET follows the nRESETI signal on the falling edge but the rising edge is delayed by RST_DLY. nRESET is deasserted high following the reset delay after nRESETI goes high.

All regulator outputs that control the nRESET signal must be configured to turn on within the "nRESET delay time" of each other during the power on sequence. This requirement ensures that nRESET has a single low to high transition after a power on sequence. nRESET will then stay asserted for the programmed delay time after the last power supply goes into regulation.

The IC's specific CMI configures which power supplies are connected to the nRESET functionality. The IC's CMI also programs the specific GPIOx pin used for the reset functionality.

EXT_EN

The ACT86000 provides an external power supply enable function, EXT_EN. EXT_EN is used to control an external regulator or to provide a control signal to other system components. It is used as part of the sequencing profile and can be programmed to have different input triggers as well as delay times. EXT_EN and EXT_PG allow the IC to fully incorporate one or more external power supplies into the startup sequence. The IC's CMI programs the specific GPIOx pin used for the EXT_EN functionality.

EXT_PG

The ACT86600 provides an external power good input function, EXT_PG. This function is used as an input trigger from an external power supply. EXT_PG can be used as the input trigger to turn on ACT86600 power supplies. EXT_EN and EXT_PG allow the IC to fully incorporate one or more external power supplies into the startup sequence. The IC's CMI programs the specific GPIOx pin used for the EXT_EN functionality.

AVIN UVP and OVP CONTROL

The AVIN pin implements both undervoltage and overvoltage detection. When AVIN detects a UV or OV condition, it generates a fault condition and triggers an under-voltage protection (UVP) or over-voltage protection (OVP) function.

An overvoltage condition is latched and turns all outputs off until the over voltage condition is removed, and the interrupt or fault status is read using I²C. Both UV and OV detection can be programmed to generate interrupts if desired. The typical UV and OV deglitch times are 70µs and 200µs respectively.

VINx UVP and OVP CONTROL

The ACT86600 monitors each individual VINx pin for both undervoltage and overvoltage conditions. If a VINx input UV or OV condition is detected, the IC generates

an interrupt if that input's VIN_UV or VIN_OV mask bit is not set. This asserts the nIRQ pin active low. If the mask bit is set, then the UV/OV condition is detected and recorded but does not generate the interrupt. Tables 6 and 7 show this functionality.

Option 1 – VIN_UVOV=11. This option disables all UV/OV shutdown. Regulators remain on or off as currently programmed. Note that if the input voltage to an output goes below the voltage required for that output to stay in regulator, the output voltage may drop out and generate an output undervoltage condition.

Option 2 – VIN_UVOV=10. This option keeps the outputs on or off as currently programmed. The IC shuts down all outputs except for VCC5 and restarts 100ms after the VINx fault is no longer present.

Option 3 – VIN_UVOV=01. This option turns off the output voltage with the VINx fault condition. The output restarts after 14ms. The fault has no effect on the other outputs. The nRESET signal does not go low, even if the output with the fault drives the nRESET signal. If the output is part of the sequencing input for another regulator, that regulator may or may not turn off. This is CMI dependent.

Option 4 – VIN_UVOV=00. This option turns off both the output voltage with the VINx fault condition and the system. The IC transitions to the OVUVFLT state and attempts a restart after 100ms. If the fault is no longer present, the IC transitions back to the ACTIVE state. If the fault is still present, the IC waits another 100ms and attempts to restart. After seven restart attempts, the IC transitions to the RESET state and sets the system power failure fault flag (PWR_FAIL). The PMIC does not retry the power on sequence once this flag is set unless the flag is cleared using an I²C command or reset by removing and applying power to the PMIC.

Note that if the IC enters the UVOVFLT state with one regulator turned off, it waits 14ms to restart. If it enters the UVOVFLT state with all regulators turned off, it waits 100ms to restart.

Table 6. Input Undervoltage and Overvoltage Fault Control

VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	Buck Regulator Action	System Action
1	1	No Action	No Action
1	0	No Action	Shut Down System, retry after 100ms
0	1	Shut down buck, retry after 14 ms	No Action
0	0	shut down buck	Shut Down System, retry after 100ms

Table 7. Output Undervoltage and Overvoltage Fault Control

UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	Buck Regulator Action	System Action
1	1	No Action	No Action
1	0	No Action	Shut Down System, retry after 100ms
0	1	Shut down buck, retry after 14 ms	No Action
0	0	shut down buck	Shut Down System, retry after 100ms

Output Voltage Under/Over Voltage

The ACT86600 monitors each individual output voltage for under voltage and over voltage conditions. If an output enters an UV/OV fault condition, the IC shuts down all outputs for 100ms and restarts with the programmed power up sequence. If an output is in current limit, it is possible that its voltage can drop below the UV threshold which also shuts down all outputs. If that behavior is not desired, mask the appropriate fault bit. Each output still provides its real-time UV/OV fault status via its fault flag, even if the fault is masked. Masking an OV/UV fault just prevents the fault from being reported via the IRQ pin. A UV/OV fault condition pulls the nRESET pin low. Note that the IC's specific CMI sets the defaults for which regulators mask the UV and OV fault conditions.

The under-voltage condition on the output of each regulator is reported via a Power OK or POK signal

which is high only when the regulator output is typically within 90% to 110% of the target regulation voltage. The POK signal from each regulator can be used for sequencing other regulators in a programmable order to ensure safe turn on and turn off. It can also be used to drive a GPIO output.

Watch-Dog Supervision

The ACT86600 features a watchdog supervisory function to reset the system if the host microprocessor locks up. The 8s internal watchdog timer is enabled by setting either of the I²C bits WDSREN [] or WDPCEN [] to 1. WDSREN stands for Watch Dog Soft Reset Enable and WDPCEN stands for Watch Dog Power Cycle Enable. Once enabled, the 8s watchdog timer is reset whenever there is I²C activity. If no I²C transaction is detected for 8s, the watchdog timer expires and the PMU either performs a soft-reset or power cycle, depending on whether WDSREN [] or WDPCEN [] bit is set. If the IC performs a soft-reset, it toggles the nRESET pin, but the IC retains the latest programmed I²C settings. If the IC performs a power cycle, all outputs turn off and the IC restarts with the default I²C register settings.

Software-Initiated Power Cycle

ACT86600 supports a software-initiated power cycle. This power cycle is initiated by setting the MR [] bit to 1. This power cycle turns off all outputs and transitions the state machine to the RESET State. Note that this resets the MR bit back to 0.

Output Current Limit

The ACT86600 incorporates a three-level overcurrent protection scheme for the buck converters and a single level scheme for the LDOs. For the buck converters, the overcurrent current threshold refers to the peak switch current. The first protection level is when a buck converter's peak switch current reaches 80% of the Cycle-by-Cycle current limit threshold for greater than 16 switching cycles. Under this condition, the IC reports the fault via the appropriate fault flag bit. If the fault is unmasked, it asserts the nIRQ pin. The next level is when the current increases to the Cycle-by-Cycle threshold. The buck converter limits the peak switch current in each switching cycle. This reduces the effective duty cycle and causes the output voltage to drop, potentially creating an undervoltage condition. When the overcurrent condition results in an UV condition, and UV is not masked, the IC turns off all supplies for 100ms and restarts. The third level is when the peak switch current reaches 122% of the Cycle-by-Cycle current limit threshold. This immediately shuts down the regulator and waits 14ms before restarting.

The overcurrent fault limits for the buck converters are adjustable via I²C. Overcurrent fault reporting can be masked via I²C, but the overcurrent limits are always active and will shut down the IC when exceeded.

Thermal Warning and Thermal Shutdown

The ACT86600 monitors its internal die temperature and reports a warning via nIRQ when the temperature rises above the Thermal Interrupt Threshold of typically 135 deg C. It reports a fault when the temperature rises above the Thermal Shutdown Temperature of typically 155 deg C. A temperature fault shuts down all outputs unless the fault is masked. Both the fault and the warning can be masked via I2C. The temperature warning and fault flags still provide real-time status even if the faults are masked. Masking just prevents the faults from being reported via the nIRQ pin.

PIN DESCRIPTIONS

Many of the ACT86600 input and output pins are configurable via CMI configurations. The following descriptions refer to basic pin functions and capabilities. Refer to the CMI Options section in the back of the datasheet for specific pin functionality for each CMI.

VINx

VINx pins are the dedicated input power to the buck converters. Each buck converter's input can be connected to a different voltage to optimize system level performance if desired. Each VINx undervoltage threshold is fixed at ~2.9V rising and ~2.7V falling. The overvoltage thresholds can be independently configured for each regulator's input source. This is set by the PVIN_OV_OPT register bits. These are not user adjustable. The different OV settings give the ACT86600 very high flexibility to be used in a variety of different configurations.

Each buck converter's VINx must be bypassed directly to its dedicated PGNDx on the top PCB layer with a at least a 10µF capacitor.

AVIN

AVIN is the power supply to the fixed VCC5 regulator. AVIN should be connected either 5.0V or the highest available power supply of the chip. Because VCC5 powers the IC and the gate drivers, Connecting AVIN to 5V or higher results in the best overall efficiency. Using a voltage lower than 5V can result in lower than expected efficiency because the lower input voltage does not provide sufficient gate drive strength to fully turn on the internal FETs. Note that AVIN must be connected to a voltage equal to or higher than the highest input voltage on the VINx pins.

VBOOTx

VBOOTx are the bootstrap pins that provide bias power for the internal FETs. Connect a 22nF or larger capacitor between each VBOOTx pin and its associated SWx pin.

VINBB

VINBB is the dedicated input power pin for the buck-boost converter. VINBB must be bypassed directly to PGND on the top PCB layer with at least a 10µF capacitor.

SW1/2/3/4/7

SW1/2/3/4 are the switch nodes for the main high voltage, high current buck converters. SW7 is the switch node for the VCC5 buck converter. They connect directly to the buck inductors on the top layer.

SW5/6

SW5/6 are the switch nodes for the buck-boost converter. They connect directly to the buck-boost inductor. SW5 switches when the buck-boost operates in buck or buck-boost mode. SW6 switches when the IC operates in boost or buck-boost mode. Both SW5 and SW6 switch when the buck-boost operates in true buck-boost mode.

VBBST

VBBST is the output voltage of the buck-boost converter.

VCC5

The VCC5 pin serves two purposes. When the VCC5 converter operates in buck or LDO mode, the VCC5 pin operates as the feedback voltage and should be Kelvin connected to the output capacitor. When the VCC5 supply is configured for bypass mode, the VCC5 pin is the output voltage from the IC. In both cases, VCC5 is the input power pin that powers the ICs internal circuitry.

VFBx

The VFBx pins are the feedback pins for the regulators. They should be kelvin connected to the buck output capacitors.

VIO

VIO is the bias supply input to the IC's digital circuitry. It powers the GPIO pins. VIO is typically connected to the VINx pins but can be powered from a different voltage rail if desired. VIO should be bypassed to PGND with a 1µF ceramic capacitor.

SCL, SDA

These are the I^2C clock and data pins to the IC. They have standard I^2C functionality. They are open drain and require a pullup resistor.

GPIOx

The ACT86600 has seven GPIO pins. Each GPIO is programmed for a specific function by the IC's CMI. The available functions are input triggers for sequencing (EXT_PG), output triggers for sequencing external supplies (EXT_EN), nRESET, nIRQ, DVS input, voltage select pins for the voltage regulators, LED drivers, standard GPIOs, and a comparator. The available GPIO functionality includes digital outputs based on a converter's internal POK signal, digital inputs to turn converters on or off, sequencing inputs, and digital inputs to enter SLEEP and DPSLP modes. These configurable options allow both a variety of system functions and flexibility of pin functions. It also allows pin functionality changes on-the-fly.

GPIO1 can be configured with an internal 200kΩ pullup resistor to VIO or to VCC5. When register 0x10h bit 0 = 0, the pullup resistor is disconnected. When register 0x10h bit 0 = 1, the pullup resistor is connected. When register bit VINIO1_SEL = 0, the pullup voltage is VIO. When register bit VINIO1_SEL = 1, the pullup voltage is VCC5.

GPIO2 through GPIO7 can be configured with an internal 200kΩ pullup resistor to VIO. When the GPIOx's bit in register 0x10h = 0, the resistor is disconnected. When it = 1, the resistor is connected.

The standard GPIO function can be configured for open drain and push-pull outputs.

All GPIOx pins are 5.5V tolerant meaning they can go to 5.5V even if VIO is less than 5.5V.

GPIO1 (pin 21) - PWREN

GPIO1 is a specialty pin and can be configured either as a general purpose GPIO or as the power enable pin (PWREN input). When the IC is configured for PWREN mode, GPIO1 must be configured as the PWREN input. When the IC is configured for Always-On Mode, GPIO1 can be configured as a standard GPIO with either open-drain or push-pull output. GPIO1 cannot be configured as an LED driver or a comparator. PWREN is also used to put the IC into DPSLP mode.

GPIO2 (pin 47) - nRESET

GPIO2 is typically configured as the nRESET pin. It can be configured as a standard GPIO. GPIO2 cannot be configured as an LED driver or a comparator.

GPIO3 (pin 46) - nIRQ

GPIO3 is typically configured as the nIRQ pin. It can be configured as a standard GPIO. GPIO3 cannot be configured as an LED driver or a comparator.

GPIO4 (pin 37)

GPIO4 can be configured as a standard GPIO. GPIO4 cannot be configured as an LED driver or a comparator.

GPIO5 (pin 38)

GPIO5 is typically configured as an EXT_EN pin. It can be configured as a standard GPIO. GPIO5 cannot be configured as an LED driver or a comparator.

GPIO6 (pin 14)

In addition to having standard GPIO functionality, GPIO6 can be configured as an LED driver or a comparator. GPIO6 cannot be configured as a push-pull output.

GPIO7 (pin 16)

In addition to having standard GPIO functionality, GPIO7 can be configured as an LED driver or a comparator. GPIO7 cannot be configured as a push-pull output.

GPIO Comparator Functionality

GPIO6 and GPIO7 can be configured as a standard comparator input. The reference voltage is 0.8V. The output of the comparator can be used internally to the IC or routed to one of the available GPIOs to be made external to the IC.

GPIO LED Driver Functionality

GPIO6 and GPIO7 are analog GPIOs and can be configured as LED current sink drivers. In this mode, they function as open-drain current sinks. The GPIOs are 5V pins and the maximum pin voltage on the open drain LED current sinks should be limited to 5.5V or below. In LED current mode, the GPIOs can sink up to 22mA. The following table shows the ISETx I²C setting to program the desired LED sink current.

Table 8. GPIO6 and GPIO7 Current Sink Settings

ISETx [3:0]	ILEDx (mA)
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	10
1010	12
1011	14
1100	16
1101	18
1110	20
1111	22

PGNDx

The PGNDx pins are the switching converter power ground pins. They connect directly to the buck converters' low side FETs. Buck1 uses PGND1. Buck2 uses PGND2, Buck3 uses PGND3. Buck4 uses PGND4. The buck-boot uses PGND7. All PGNDx pins must be connected directly to the IC's exposed pad under the IC. Note that all PGNDx pins are electrically connected.

AGND

AGND is the ground pin for the IC's analog circuitry. AGND must be connected to the IC's exposed pad. The connection between AGND and the exposed pad should not have high currents flowing through it. AGND should be routed as a separate ground plane and connected to the main ground plane in only one location.

HIGH VOLTAGE STEP-DOWN DC/DC REGULATORS

General Description

The ACT86000 contains four fully integrated, high voltage, step-down converters. Buck1/2 are 6A outputs while Buck3/4 are 4A outputs. The buck converters can be operated in parallel to provide higher output currents. They use a proprietary topology based on a Constant ON Time (COT) architecture. They are synchronous step-down converters that use a hysteretic constant on-time mode that enables very low quiescent current during stand-by operation. They allow the use of small external components while emulating a constant frequency PWM mode regulator during continuous current mode operation under high load current situations. The integrated, low Rdson FETs help achieve greater than 95% efficiency. They are internally compensated, requiring only three small external components (Cin, Cout, Lout) for operation. All regulators are available with a variety of standard and custom output voltages, and may be software-controlled via the I2C interface for systems that require advanced power management functions.

The ACT86600 buck regulators are highly configurable and can be quickly and easily reconfigured via I²C. This allows them to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

Dynamically change output voltage

On/Off control

Low power mode

Overcurrent thresholds

Sequencing order and delay times

Refer to the Qorvo Application Note describing the Register Map for full details on I2C functionality and programming ranges.

Each HV Buck has a separate input voltage pin, VINx. This allows the user to supply each regulator with a power source of choice and therefore optimize the power demand from each available power source. For example, each HV regulator can be supplied with either a 12.0V or 5.0V power supply (3.0 – 14.4V typical range). Each HV Buck input voltage OV threshold can be independently configured for a 5.8V or a 15V input. This setting is factory configured to 5.8V or 15V and is not user adjustable.

Operating Mode

By default, the Buck1/2/3/4 regulators operate in a pseudo fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power and improve efficiency at light loads.

To further optimize efficiency and reduce power losses at extremely light loads, an additional lower power mode, LPM, is available. LPM minimizes quiescent current in between switching cycles. Setting I²C bit EN_LPM = 1 enables LPM mode and reduces the quiescent current by approximately 370µA. To minimize load transient drops when going from LPM to full load, the output voltage is increased by 2% in LPM mode. The output voltage ripple increases to approximately 4% of the output voltage. The customer should test both settings in their system and choose the best option to balance power consumption, voltage ripple, and transient response in their system. LPM is enabled when I²C bits EN_LPM = 1.

Synchronous Rectification

Each HV Buck regulator features an integrated synchronous rectifier (or LS FET), maximizing efficiency and minimizing the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, all converters automatically turn on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), each converter can be independently disabled via I²C. Each CMI version requires a different set of commands to disable a converter, so contact the factory for specific instructions if needed. Each converter contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is typically enabled by default. This function is not user selectable.

Soft-Start

The HV BUCK regulators include a fixed 1ms internal soft-start ramp which limits the rate of change of the output voltage. This time is measured from 5% to 95% of the programmed output voltage. This minimizes input inrush current and ensures that the output powers up in a monotonic manner that is independent of current load on the outputs. This circuitry is effective any time the regulator is enabled, as well as during re-try after responding to a short-circuit or other fault condition

Output Voltage Setting

The HV Bucks regulate to the voltage defined by their I²C register VSET0 in normal operation and by VSET1 in DVS mode. Each Buck regulator can be programmed to one of two output voltage ranges: Output-Low Range and Output-High Range.

Each buck converter's output range can be programmed independently of the others. Note that the output voltage range should NOT be changed while the output is enabled. Qorvo does not recommend changing the output voltage range from its default setting because its internal voltage reference is only trimmed to its default setting. When the buck converter's VOUT_OPT bit = 0, that output uses Output-High Range. When VOUT_OPT = 1, that output uses the Output-Low Range.

The programming range for Output-High is 0.6V to 5.26V in 20mV steps.

V_{BUCKx} = 0.6V + VSETx * 0.02V

Where VSETx is the decimal equivalent of the value in each regulator's I²C VSETx register. The VSETx registers contain an unsigned 8-bit binary value. As an example, if Buck 1's VSET0 register contains 00111100b (60 decimal), the output voltage is 1.8V.

Note that the maximum output voltage is 5.26V. If VSETx is programmed higher than 233 decimal, the keeps the programmed value and sets the output voltage to 5.26V.

The programming range for Output-Low is 0.6V to 1.875V in 5mV steps.

V_{BUCKx} = 0.6V + VSETx * 0.005V

Where VSETx is the decimal equivalent of the value in each regulator's I²C VSETx register. The VSETx registers contain an unsigned 8-bit binary value. As an example, if Buck 1's VOUT0 register contains 11110000b (240 decimal), the output voltage is 1.8V.

Qorvo recommends that a buck converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Duty Cycle Limitations / Minimum On-Time

The HV Buck minimum on-time is 50ns. This limits the minimum allowable output voltage. This is a standard limitation for all buck converters with high input voltages and low output voltages. The following equation calculates the maximum allowable switching frequency for a HV Buck design.

$$F_{SW\_max} = \frac{VOUT_{min}}{50ns * VIN_{max}} *$$

Where F_{sw_max} is the maximum allowable switching frequency, $VOUT_{min}$ is the minimum required output voltage, and VIN_{max} is the maximum input voltage on VINx.

Dynamic Voltage Scaling

Each buck converter supports Dynamic Voltage Scaling (DVS). DVS allows the user to optimize the processor's energy to complete tasks by lowering the processor's operating frequency and input voltage when lower performance is acceptable. In normal operation, each output regulates to the voltage programmed in the I²C register VSET0. During DVS, each output regulates to VSET1.

When entering and exiting DVS, the IC's digital logic steps the output setting through each step between the initial and final settings at a rate of 20mV/us in low-output range and 80mV/us in high-output range. During this transition, the regulators' OV and UV thresholds are ignored to avoid triggering false OV or UV faults.

To achieve the fastest transition, the regulator may be temporarily forced into "forced PWM" during the transition. This ensures that the output voltage reaches the new set point as quickly as possible by actively charging or discharging the output capacitor.

The IC can be programmed to enter DVS by I²C, when the IC enters SLEEP mode, or when the IC enters DPSLP mode.

Overcurrent and Short Circuit Protection

Each buck converter provides overcurrent and short circuit protection with built-in foldback protection. Overcurrent protection is achieved with cycle-by-cycle current limiting on both the HS and LS FETs. The HS FET implements peak overcurrent threshold while the LS FET implements valley protection. These thresholds are set by each converter's ILIM I²C register bits.

Table 9. HV Buck Peak and Valley Threshold Settings

ILIM[1:0]	Buck1 and Buck2		Buck3 and Buck4	
	HS FET Peak Current (A)	LS FET Peak Current (A)	HS FET Peak Current (A)	LS FET Peak Current (A)
00	6	5	4	3
01	7	6	5	4
10 (Note 1)	8	7	6	6
11 (Note 1)	9	8	7	6

Note 1: Do use these settings when VINx is > 10V.

If the peak current reaches 75% of the programmed threshold for 16 consecutive switching cycles, the IC asserts nIRQ low if the IWARN_INT_MASK bit set to 0 and changes I²C bit ILIM_WARN = 1 but continues to operate normally. If the peak current reaches the programmed threshold, the IC turns off the power FET for that switching cycle. If the peak current reaches the threshold 16 consecutive switching cycles, the IC asserts nIRQ low if the IFLT_INT_MASK bit set to 0. This condition typically results in shutdown due to an UV condition due to the shortened switching cycle. A short circuit condition that results in the peak switch current being 122.5% of ILIM_SET immediately shuts down the supply and asserts nIRQ low if the ISHUT_INT_MASK bit set to 0. The supply tries to restart in 14ms. If the fault condition is not masked, the IC transitions to the OVUV State, turns off all supplies, and restarts the system in 100ms. The contents of these registers are latched until read via I²C. Overcurrent circuit conditions can be masked via the I²C bit ILIM_STDN_DIS. The IC's specific CMI determines which regulators mask the current limit fault.

Compensation

The HV Buck regulators utilize a proprietary internal compensation scheme to simultaneously simplify external component selection while optimizing transient performance over their full operating range. No external compensation design is required. Simply follow a few simple guidelines described below when choosing the output capacitor and inductor.

Input Capacitor Selection

Each regulator requires a high quality, low-ESR, ceramic input capacitor. Each HV Buck regulator input has separate input pins. Each input can be connected to the same or a different voltage rail. Even if two inputs are connected to the same voltage rail, each VINx pin must have a dedicated input capacitor. 10µF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5V, Z5U, or similar dielectrics is not recommended. Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from the VINx pin to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

Each HV Buck regulator utilizes a Constant on Time, a hysteretic mode hybrid topology, and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. The ACT86600 regulators are optimized for inductor values between 0.22µH to 2.2µH range. Choose inductors with a low DC-resistance, or DCR, for higher efficiency and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum inductor peak current by at least 30%. Additionally, the inductor peak-to-peak current ripple must be carefully considered along with the selected switching frequency before selecting appropriate inductor values with adequate current rating. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The HV Buck regulators are designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. The buck regulators are designed to operate with greater than 44µF of capacitance. To ensure stability, ensure that the actual output capacitance is greater than 44µF. Design for an output ripple voltage less than 1% of the output voltage. The output capacitance can be increased to reduce output voltage ripple and improve load transients if

needed. The following equation calculates the output voltage ripple as a function of output capacitance.

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

Output capacitance affects low power mode behavior and the output capacitor discharge time at turnoff. System level evaluation should be performed to optimize the needed output capacitor value.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications. Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

POK [] and Output Fault Interrupt

Each regulator features an internal Power-OK (POK) output. Each POK output can drive the startup and shutdown sequence of another regulator. It can also drive a GPIO output. The POK output also drives a status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically ~10.0% below the programmed regulation voltage, that regulator's POK [] bit is set to 0.

The POK status bit can be masked if desired. Mask POK by setting the Buck converter's nFLTMSK [ ] bit to 0. When nFLTMSK = 1, the POK fault is not masked. The ACT86600 interrupts the processor when the DC/DC's output voltage falls below the Power-OK (POK) threshold by asserting the nIRQ pin low. nIRQ remains asserted until either the regulator is turned off or the output voltage goes back into regulation and the POK [] bit has been read via I²C. The POK interrupt is cleared when the POK fault condition is no longer present and the microprocessor performs an I²C read of the POK register bit. Note that even if the POK fault is no longer present, the POK bit is latched to 0 until after the I²C read is performed.

High Current Paralleled Outputs

The ACT86600's allows the HV Bucks to be operated in parallel to provide higher output currents. Buck1/2 can be operated in parallel to provide a single 12A output. Buck3/4 can be paralleled to provide an 8A output. Note that Buck1/2 can be operated in single or dual phase mode independently of the Buck3/4. When operated in parallel, the two converters switch out of phase to minimize ripple currents and noise. The output inductor and capacitor requirements are the same as single phase operation. Note that dual phase operation requires a dedicated CMI. The customer cannot modify register setting to change outputs from single to dual or dual to single phase operation

Buck1's register settings are used for Buck1/2 dual phase operation. Buck3's register settings are used for Buck3/4 dual phase operation.

The PCB considerations for dual phase operation are identical to single phase operation. Dual phase operation is achieved by simply connecting the two output voltages together. Differential remote sensing is an available option with dual phase operation.

Differential Remote Sensing Option

Differential remote sensing is an available option with dual phase operation. Differential remote sensing allows the feedback path to compensate for voltage drops in both the positive and negative current path.

Disable differential remote sensing by setting MUL_GNDS_SEL = 0. VFB1, VFB2, VFB3, and VFB4 must all be connected to their output voltages.

Enable differential remote sensing by setting MUL_GNDS_SEL = 1. VFB1 and VFB3 must be connected to their outputs. VFB2 and VFB4 are the negative sensing input and must be connected to the output capacitor ground pin.

The MUL_GNDS_SEL bit is not user configurable.

HV Buck PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow these layout guidelines when designing the ACT86600 PCB. Refer to the Qorvo ACT86600 Evaluation Kit for a layout example.

1. Place the HV Buck and AVIN input capacitors as close as possible to the IC. Connect the capacitors directly to the corresponding VINx input pin and PGNDx power ground pin. Do not use vias to route power between the input capacitors and the IC.

2. Minimize the switch node trace length between each SWx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
4. Connect the PGNDx ground pins and the AGND ground pin directly to the exposed pad under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
5. Connect the VIO input capacitor to the power ground pins. Minimize the distance from this capacitor to VIO, but at a lower priority than the input capacitor placement.
6. Connect each regulator's VFBx pin to its regulation point through the shortest possible path while keeping sufficient distance from switching nodes to prevent noise injection. Shield the VFBx traces from any noisy traces if they are routed near each other. Do not connect VFBx to the output power plane at the inductor. VFBx must be connected at the farthest output capacitor from the inductor or closer to the load bypass capacitors.
7. Connect the exposed pad directly the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat.

BUCK-BOOST REGULATOR

General Description

The ACT86600 contains a fully integrated, high voltage, Buck-boost converter. It can be configured for buck-boost mode or buck-only mode. In buck-boost mode, it provides up to 500mA of output current and operates with a 9.6V to 15.95V output voltage range. In buck-only mode, it provides up to 600mA of output current and operates with a 1V to 4.175V output voltage range. It uses a proprietary control architecture to maximize efficiency. The IC operates with current mode control with a factory selectable 562.5kHz or 1125kHz switching frequency. The integrated low Rdson FETs help achieve 95% efficiency. It is internally compensated, requiring only three small external components (Cin, Cout, Lout) for operation. It may be software controlled via I²C interface. It can be configured in either buck-boost or boost mode.

The Buck-boost converter is highly configurable and can be quickly and easily reconfigured via I²C. This allows it to support changes in hardware requirements without the need for PCB changes. Examples of I²C functionality are given below:

Real-time power good, OV, and current limit status

Ability to mask individual faults

On/Off control

Low power mode

Overcurrent thresholds

Sequencing order and delay times

The Buck-boost has a dedicated input voltage pin, VINBB. This allows the user to supply it with a different power source from the other regulators and therefore optimize the power demand from each available power source. For example, it can be supplied with a 3.3V, 5V, or 12.0V input (3.0 – 14.4V typical range). The Buck-boost input voltage OV threshold can be independently configured to 5.8V or 15V. This setting is factory configured and is not user adjustable.

The Buck-boost is ideally suited for optimizing solid state drive (SSD) power solutions. The input voltage to a 12V SSD can vary as much as +/- 20%. However, an SSD's VPP input rail requires a tightly regulated 12V +/- 3% input voltage. The ACT86660 Buck-boost architecture conditions the unregulated 12V input voltage to provide a tightly regulated 12V output voltage. It does this without the need for additional discrete regulators.

Operating Modes

By default, the Buck-boost regulator operates in a fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power and improve efficiency at light loads.

At light loads, the Buck-boost operates in "burst" or "skip" mode. It automatically skips cycles to minimize switching losses. It enters this mode when the load current drops low enough that the inductor current drops to 0A. This is the transition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). It skips switching cycles as needed to maintain a regulated output voltage when the required duty cycle is less than the minimum on-time. In burst or skip mode, higher efficiency is maintained even at light load conditions by operating the converter and switching only when necessary. The regulator automatically jumps out of skip or burst mode to PWM mode when the load current increases.

The Buck-boost has two factory configurable operating modes: buck-boost mode or buck only. Note that the operating mode is set at the factory and is not user adjustable.

Buck-boost Mode: In this mode, the output voltage can be either higher or lower than the input voltage. All four internal FETs switch to achieve this functionality. When the Buck-boost input voltage is below the voltage threshold set by I²C bit BBST_THRESH, the control algorithm reconfigures the regulator into boost-only mode. This reduces power dissipation by fixing two FETs and using the other two as a boost converter. When the input voltage is greater than this threshold, the buck portion of the buck-boost (SW5) operates with a fixed duty cycle. The control loop modulates the boost portion (SW6) to regulate the output voltage. The transition between these two modes is seamless and does not require user intervention. In buck-boost mode, the output voltage must be higher than 60% of the input voltage.

Buck-only Mode: In this mode, the control algorithm reconfigures the Buck-boost into a buck converter. Two FETs are fixed while the other two operate as a buck converter. This minimizes switching losses and power dissipation. In buck-only mode, the output voltage must be less than 70% of the input voltage.

Synchronous Rectification

The Buck-boost regulator features four fully integrated FETs. This maximizes efficiency and minimizes the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

When power is applied to the IC, the Buck-boost converter automatically turns on according to a pre-programmed sequence. Once in normal operation (ACTIVE state), it can be independently disabled via I²C. Each CMI version requires a different set of commands to disable the Buck-boost, so contact the factory for specific instructions if needed. The Buck-boost contains an optional integrated discharge resistor that actively discharges the output capacitor when the regulator is disabled. The discharge function is typically disabled but is user selectable by the EN_PLDN bit in register 0xC6h.

Soft-Start

The Buck-boost regulator includes a fixed 10ms internal soft-start ramp which limits the rate of change of the output voltage. This time is measured from 5% to 95% of the programmed output voltage. This minimizes input inrush current and ensures that the output powers up in a monotonic manner that is independent of current load on the outputs. This circuitry is effective any time the regulator is enabled, as well as during re-try after responding to a short-circuit or other fault condition.

Output Voltage Setting

The Buck-boost converter regulates to the voltage defined by its I²C register VSET0 in normal operation.

In **Buck-boost** mode, the programming range is 9.6V to 15.95V in 50mV steps.

$V_{BUCK\text{-}BOOST}$ = 9.6V + VSET0 * 0.05V

Where VSET0 is the decimal equivalent of the value in the buck-boost regulator's I²C VSET0 register. The VSET0 registers contain an unsigned 7-bit binary value. As an example, if the VSET0 register contains 0110000b (48 decimal), the output voltage is 12.0V.

In **Buck-only** mode, the programming range is 1V to 4.175V in 25mV steps.

$V_{BUCK\text{-}BOOST}$ = 1V + VSET0 * 0.025V

Where VSET0 is the decimal equivalent of the value in the buck-boost regulator's I²C VSET0 register. The VSET0 register contains an unsigned 7-bit binary value. As an example, if the VSET0 register contains 0100000b (32 decimal), the output voltage is 1.8V.

Qorvo recommends that the Buck-boost converter's output voltage be kept within +/- 25% of the default output voltage to maintain accuracy. Voltage changes larger than +/- 25% may require different factory trim settings (new CMI) to maintain accuracy.

Duty Cycle Limitations / Minimum On-Time

The Buck-boost minimum on-time in buck-only mode is 130ns. This limits the minimum allowable output voltage. This is a standard limitation for all buck converters with high input voltages and low output voltages. Most designs will operate at 1125kHz. However, if a design's calculated on-time is less than 130ns, the converter must be operated at 562.5kHz. The following equation calculates the minimum allowable output voltage in buck-only mode.

$$VOUT_{Min} = 130ns * VIN_{Max} * F_{SW}$$

Where $VOUT_{Min}$ is the minimum allowable output voltage, VIN_{Max} is the maximum input voltage on VINBB, and F_{sw} is the switching frequency.

Dynamic Voltage Scaling

The Buck-boost converter does not support Dynamic Voltage Scaling (DVS).

Overcurrent and Short Circuit Protection

The Buck-boost converter provides overcurrent and short circuit protection. It provides cycle-by-cycle current limit on the Q_{SW5_top} VINBB-to-SW5 FET. The maximum current threshold is set by the ILIM I²C register bits. The following table applies to HS1, the VINBB toSW5 FET.

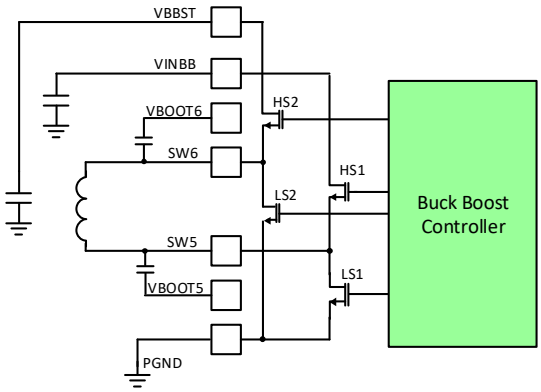


Figure 8. Buck-Boost FETs

Table 10. Buck-Boost Peak Current Threshold Settings

ILIM[1:0]	$Q_{SW5\ top}$ FET Peak Current (A)
00	1.2
01	1.7
10	2.1
11	2.5

If the peak current reaches 80% of the programmed threshold for 16 consecutive switching cycles and the IWARN_INT_MASK bit = 0, the IC asserts nIRQ low and changes the I²C bit ILIM_WARN = 1. It continues to operate normally in this condition.

If the peak current reaches the programmed threshold and the I²C bit IFLT_INT_MASK bit = 0, the IC turns off the power FET for that switching cycle. If the peak current reaches the threshold 16 consecutive switching cycles, the IC asserts nIRQ low. This condition typically results in shutdown due to an UV condition due to the shortened switching cycle. A short circuit condition that results in the peak switch current being 125% of ILIM_SET immediately shuts down the supply and asserts nIRQ low if the I²C bit SHUT_INT_MASK = 0. The supply tries to restart in 14ms. If the fault condition is not masked, the IC transitions to the OVUV State, turns off all supplies, and restarts the system in 100ms.

Compensation

The Buck-boost utilizes a proprietary internal compensation scheme to simultaneously simplify external component selection while optimizing transient performance over their full operating range. No external compensation design is required. Simply follow a few simple guidelines described below when choosing the output capacitor and inductor.

Input Capacitor Selection

The input requires a high quality, low-ESR, ceramic input capacitor. The Buck-boost input voltage can be connected to the same or a different voltage rail from the other converters. Even if it is connected to the same voltage rail, it must have a dedicated input capacitor. 10µF capacitors are typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV. When in buck-mode, the following equations calculates the input ripple.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5V, Z5U, or similar dielectrics is not recommended. Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from the VBBST pin to the capacitor and from the capacitor to PGNDx should as short and wide as possible.

Inductor Selection

The Buck-boost uses a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. The ACT86600 Buck-boost regulator is optimized for a 4.7µH to 6.8µH range. Choose inductors with a low DC-resistance, or DCR, for higher efficiency and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum inductor peak current by at least 30%. Additionally, the inductor peak-to-peak current ripple must be carefully considered along with the selected switching frequency before selecting appropriate inductor values with adequate current rating. The following equations calculate the inductor ripple current in buck-only and boost-only modes.

$$\Delta I_{L(Buck-only)} = \frac{\left(1-\frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

$$\Delta I_{L(Boost-only)} = \frac{\left(1-\frac{V_{IN}}{V_{OUT}}\right) * V_{IN}}{F_{SW} * L}$$

The buck-boost ripple current is the higher of the two following equations.

$$\Delta I_{L(Buck-boost)} = \frac{\left(1 - 0.7 * \frac{V_{VIN}}{V_{OUT}}\right) * V_{IN}}{F_{SW} * L}$$

$$\Delta I_{L(Buck-boost)} = \frac{0.3 * V_{VOUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

The Buck-boost regulator is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. It is designed to operate with 2x22µF capacitors. To ensure stability, ensure that the actual output capacitance is greater than 20µF. Design for an output ripple voltage less than 1% of the output voltage. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed. The following equations calculate the output voltage ripple as a function of output capacitance based on operating mode

$$V_{RIPPLE\ (Buck\text{-}only)} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

$$V_{RIPPLE\ (Boost\text{-}only)} = \frac{I_{OUT} * \left(1 - \frac{V_{IN}}{V_{OUT}}\right)}{F_{SW} * C_{OUT}}$$

$$V_{RIPPLE\ (Buck\text{-}boost)} = \frac{I_{OUT} * \left(1 - 0.7 * \frac{V_{IN}}{V_{OUT}}\right)}{F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, C_{OUT} is the output capacitance after taking DC bias into account, and I_{OUT} is the load current.

Output capacitance affects low power mode behavior and the output capacitor discharge time at turnoff. System level evaluation should be performed to optimize the needed output capacitor value.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5V, Z5U, or similar dielectrics is not recommended. Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from the input pin to the capacitor and from the capacitor to PGND should as short and wide as possible.

POK [] and Output Fault Interrupt

The Buck-boost regulator features an internal Power-OK (POK) status bit that can be read by the system microprocessor via the I²C interface. It can also drive a GPIO output. The POK output also drives a status bit that can be read by the system microprocessor via the I²C interface. If an output voltage is lower than the power-OK threshold, typically ~10.0% below the programmed regulation voltage, that regulator's POK [] bit is set to 0.

The POK status bit can be masked if desired. Mask POK by setting the nFLTMSK [ ] bit to 0. When nFLTMSK = 1, the POK fault is not masked. The ACT86600 interrupts the processor when the Buck-boost output voltage falls below the Power-OK (POK) threshold asserting the nIRQ pin low. nIRQ remains asserted until either the regulator is turned off or the output voltage goes back into regulation and the POK [] bit has been read via I²C. The POK interrupt is cleared when the POK fault condition is no longer present and the microprocessor performs an I²C read of the POK register bit. Note that even if the POK fault is no longer present, the POK bit is latched to 0 until after the I²C read is performed.

Buck-boost PCB Layout Considerations

High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow these layout guidelines when designing the ACT86600 PCB. Refer to the Qorvo ACT86600 Evaluation Kit for a layout example.

1. Place the Buck-boost input and output capacitors as close as possible to the IC. When operating in Buck-boost mode, both the input and output capacitor placement are critical. In boost-only mode, the output capacitor placement should have higher priority. In buck-only mode, the input capacitor should have higher priority. Connect the input capacitors directly to VINBB and PGND. Connect the output capacitors directly to VBBST and PGND. Do not use vias to route power between the capacitors and the IC.
2. Minimize the switch node trace length between each SWx pin and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
4. Connect the PGND ground pin and the AGND ground pin directly to the exposed pad under the IC. The AGND ground plane should be

routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.

5. Connect the exposed pad directly the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions.

VCC5 ALWAYS-ON SUPPLY

The ACT86600 VCC5 supply is a fully integrated, always-on, fixed 5V, bias supply. VCC5 automatically switches operation between buck and LDO mode to optimize efficiency. It efficiently converts higher input voltages into the lower 5V required for internal biasing and gate drives. It operates from inputs as high as 18V. For 5V systems, it can be configured into bypass mode to directly pass the input voltage to the output.as an LDO. It provides up to 500mA and can be used to power additional system circuitry. It uses a proprietary control architecture to maximize efficiency. The emulated switching frequency is fixed at 2400kHz. The integrated low Rdson FETs help achieve 90% efficiency. It is internally compensated, requiring only three small external components (Cin, Cout, Lout) for operation.

VCC5 is designed to optimize solid state drive (SSD) power solutions. A typical 12V system rail must be converted to 5V for biasing the power supply and other circuitry. The buck topology does this efficiently with minimal power loss. This eliminates the need for additional discrete regulators.

Because VCC5 powers the PMIC bias circuitry and the internal gate drivers, its input, AVIN, should be powered by an input voltage that is 5V or higher. This ensures that all the ACT86600 power FETs are driven into full enhancement to get the best on-resistance (RDS_{ON}) and highest efficiencies.

Operating Modes

VCC5 operates in a pseudo fixed-frequency PWM mode at medium to heavy loads, then transition to a proprietary power-saving mode at light loads in order to save power and improve efficiency at light loads.

At light loads, it operates in “burst” or “skip” mode. It automatically skips cycles to minimize switching losses. It enters this mode when the load current drops low enough that the inductor current drops to 0A. This is the transition between continuous conduction mode (CCM) and discontinuous conduction mode (DCM). It skips switching cycles as needed to maintain a regulated output voltage when the required duty cycle is less than the minimum on-time. In burst or skip mode, higher efficiency is maintained even at light load conditions by operating the converter and switching only when necessary. The regulator automatically jumps out of skip or burst mode to PWM mode when the load current increases.

VCC5 has two factory configurable operating modes: buck mode and bypass mode. Note that the operating mode is set at the factory and is not user adjustable.

Buck Mode: In this mode, VCC5 operates as either a buck converter or an LDO. When AVIN is greater than 7V, the control algorithm automatically configures VCC5 into a buck converter. When the input drops below 6.5V, it changes the configuration into an LDO to minimize switching losses. The transition between these two modes is seamless and does not require user intervention.

Bypass Mode: In this mode, the buck power FET is fully turned on and passes AVIN directly to the VCC5 output. This mode is intended for applications with an existing 5V input rail. When using bypass mode, the output inductor is not required. Simply connect the output capacitor directly to VCC5 and leave SW7 floating.

Synchronous Rectification

VCC5 features two fully integrated FETs. This maximizes efficiency and minimizes the total solution size and cost by eliminating the need for external rectifiers.

Enable / Disable Control

VCC5 is an always-on rail and automatically turns on when the input voltage rises above the UVLO threshold. Once in normal operation (ACTIVE state), VCC5 cannot be disabled.

Soft-Start

VCC5 includes a fixed 400µs internal soft-start ramp which limits the rate of change of the output voltage. This time is measured from 0V to 5V. This minimizes input inrush current and ensures that the output powers up in a monotonic manner that is independent of current load on the outputs. This circuitry is effective any time the regulator is enabled, as well as during re-try after responding to a short-circuit or other fault condition.

Output Voltage Setting

VCC5 has a fixed 5V output. This voltage is not user adjustable.

Overcurrent and Short Circuit Protection

VCC5 provides overcurrent and short circuit protection. It provides cycle-by-cycle current limit when in buck mode and current foldback when in LDO mode.

If the peak current reaches the programmed threshold, the IC turns off the power FET for that switching cycle. This condition typically results in shutdown due to an UV condition due to the shortened switching cycle. When VCC5 voltage less than 2.6V the VCC5 regulator automatically switch to LDO mode with current limit foldback to 50mA typical to provide further protection.

Compensation

VCC5 utilizes a proprietary internal compensation scheme to simultaneously simplify external component selection while optimizing transient performance over their full operating range. No external compensation design is required. Simply follow a few simple guidelines described below when choosing the output capacitor and inductor.

Input Capacitor Selection

The input requires a high quality, low-ESR, ceramic input capacitor. VCC5 can be connected to the same or a different voltage rail from the other converters. Even if it is connected to the same voltage rail, it must have a dedicated input capacitor. A 10µF capacitor is typically suitable, but this value can be increased without limit. Smaller capacitor values can be used with lighter output loads. Choose the input capacitor value to keep the input voltage ripple less than 50mV. When in buck-mode, the following equation calculates the input ripple.

$$V_{ripple} = Iout * \frac{\frac{Vout}{Vin} * \left(1 - \frac{Vout}{Vin}\right)}{Fsw * Cin}$$

Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5V, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. The input capacitor must be placed as close to the IC as possible. The traces from AVIN to the capacitor and from the capacitor to PGND should as short and wide as possible.

Inductor Selection

VCC5 uses a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over its full operating range. It requires a 1µH inductor. Choose inductors with a low DC-resistance, or DCR, for higher efficiency and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum inductor peak current by at least 30%. Additionally, the inductor peak-to-peak current ripple must be carefully considered along with the selected switching frequency before selecting appropriate inductor values with adequate current rating. The following equation calculates the inductor ripple current.

$$\Delta I_L = \frac{\left(1 - \frac{V_{OUT}}{V_{IN}}\right) * V_{OUT}}{F_{SW} * L}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{SW} is the switching frequency, and L is the inductor value.

Output Capacitor Selection

VCC5 is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR capacitors. It is designed to operate with greater than 10µF of capacitance. To ensure stability, ensure that the actual output capacitance is greater than 10µF. Design for an output ripple voltage less than 1% of the output voltage. The output capacitance can be increased to reduce output voltage ripple and improve load transients if needed. The following equation calculate the output voltage ripple

$$V_{RIPPLE} = \frac{\Delta I_L}{8 * F_{SW} * C_{OUT}}$$

Where ΔI_L is the inductor ripple current, F_{SW} is the switching frequency, and C_{OUT} is the output capacitance after taking DC bias into account.

The 10µF capacitor is the output capacitor of the buck topology. Note that an additional 0.22µF must be connected directly to the VCC5 pin. This capacitor is a high frequency bypass capacitor that minimizes noise entering the IC.

Two of the most common dielectrics are Y5V and X5R. Whereas Y5V dielectrics are inexpensive and can provide high capacitance in small packages, their capacitance varies greatly over their voltage and temperature ranges and are not recommended for DC/DC applications. X5R and X7R dielectrics are more suitable for output capacitor applications. Be sure to consider the capacitor's DC bias effects and maximum ripple current rating when using capacitors smaller than 0805.

VCC5 PCB Layout Considerations

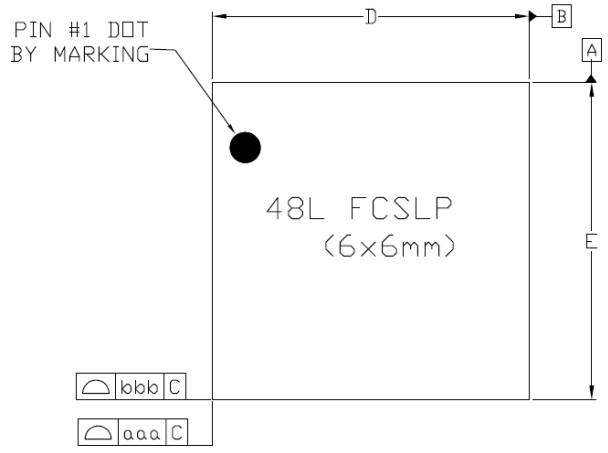
High switching frequencies and large peak currents make PC board layout an important part of step-down DC/DC converter design. A good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Follow these layout guidelines when designing the ACT86600 PCB. Refer to the Qorvo ACT86600 Evaluation Kit for a layout example.

1. Place the AVIN input capacitors as close as possible to the IC. Connect the capacitors directly to the AVIN input pin and PGND power

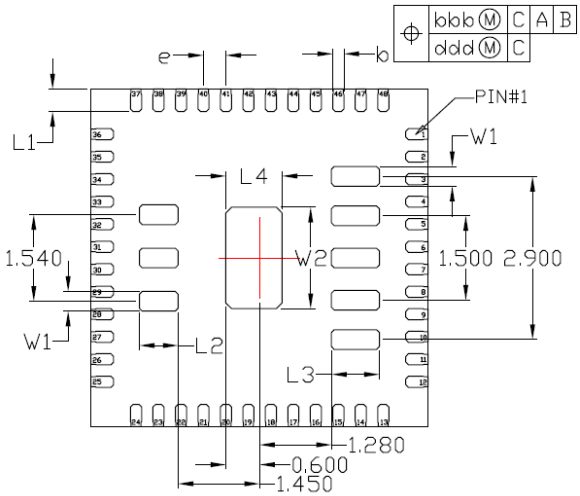
ground pin. Do not use vias to route power between the input capacitors and the IC.

2. Minimize the switch node trace length between SW7 and the inductor. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. The input capacitor and output capacitor grounds should be connected as close together as possible, with short, direct, and wide traces.
4. Connect the PGND ground pin and the AGND ground pin directly to the exposed pad under the IC. The AGND ground plane should be routed separately from the other ground planes and only connect to the main ground plane under the IC at the AGND pin.
5. Connect a 10µF capacitor directly to the VCC5 pin and AGND as close to the IC as possible to minimize noise on VCC5 because it provides power to sensitive analog internal circuitry. Then route the VCC5 net directly to the output capacitor. Do not connect VCC5 to the output power plane at the inductor.
6. Connect the exposed pad directly the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers that allows the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes and adding vias that restrict the radial flow of heat of operating conditions.

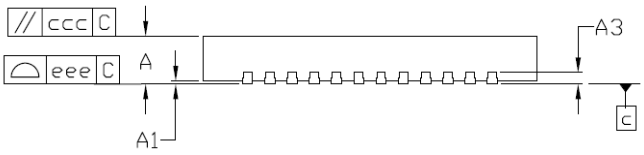
PACKAGE OUTLINE AND DIMENSIONS – 48 PIN QFN



Top View



Bottom View



Side View

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	5.950	6.000	6.050
E	5.950	6.000	6.050
b	0.150	0.200	0.250
e	0.400 BSC		
L1	0.350	0.400	0.450
L2	0.640	0.690	0.740
L3	0.800	0.850	0.900
L4	0.950	1.000	1.050
W1	0.300	0.350	0.400
W2	1.750	1.800	1.850
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

Notes

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5-2009.
2. All DIMENSIONS ARE IN MILLIMETERS.

Contact Information

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