30V, 5A Synchronous Step-Down Converter

LA1315E

Overview


ESOP8

The LA1315E is a fully integrated easy to use synchronous step-down Buck converter, which integrated low on resistance high-side and low-side power MOSFETs. The LA1315E can deliver 5A continued output current efficiently with constant on time (COT) control for fast loop response.

The LA1315E achieves high power conversion efficiency over a wide load range by scaling down the switching frequency under light-load conditions to reduce switching and gate driving losses.

The LA1315E has built-in protection features, such as cycle-by-cycle current limit, hiccup mode short-circuit protection, output over voltage protection, FB open protection and thermal shutdown in case of excessive power dissipation. The LA1315E is available in a space-saving ESOP8 package

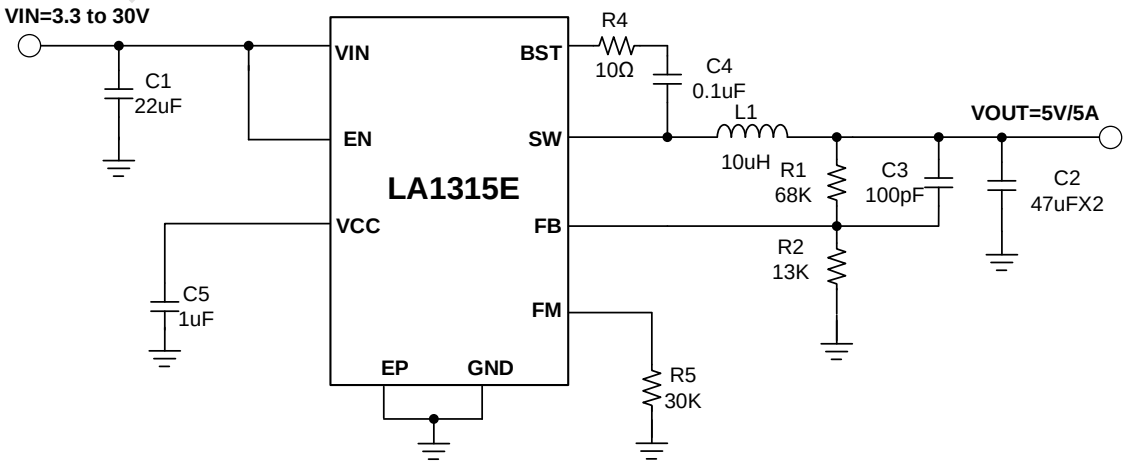
Features

- Wide 3.6V to 30V Input Range
- 43mΩ/27mΩ Power MOSFET
- Support 5A Continuous Output Current
- 350μA Low Quiescent Current
- Constant On Time Control for Fast Loop Response
- 250KHz/300K/400KHz Switching Frequency Selectable
- PFM and Forced PWM Mode Selectable
- Support Up to 100% Duty Cycle
- Output Discharge
- Output Voltage Adjustable from 0.8V
- Support Pre-Biased Output Startup
- Full Protection, OCP, OVP, FB Open Protection, OTP
- Available in a ESOP8 Package

Applications

- Telecom and Networking Systems
- IP Camera
- Automotive Cigarette Lighter Adapter
- Wall Charger
- General Purpose Point-of-Load (POL)

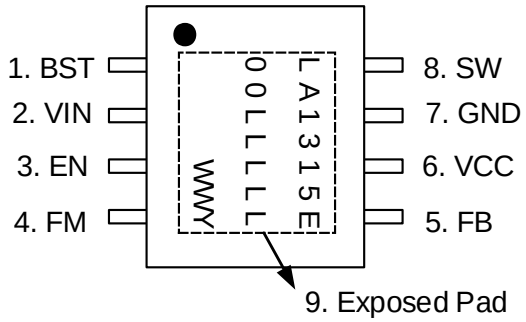
Typical Application Circuits



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1315E	ESOP8	-40 to 125°C	T/R 2500pcs/roll	sales@latticeart.com

Pin Diagram

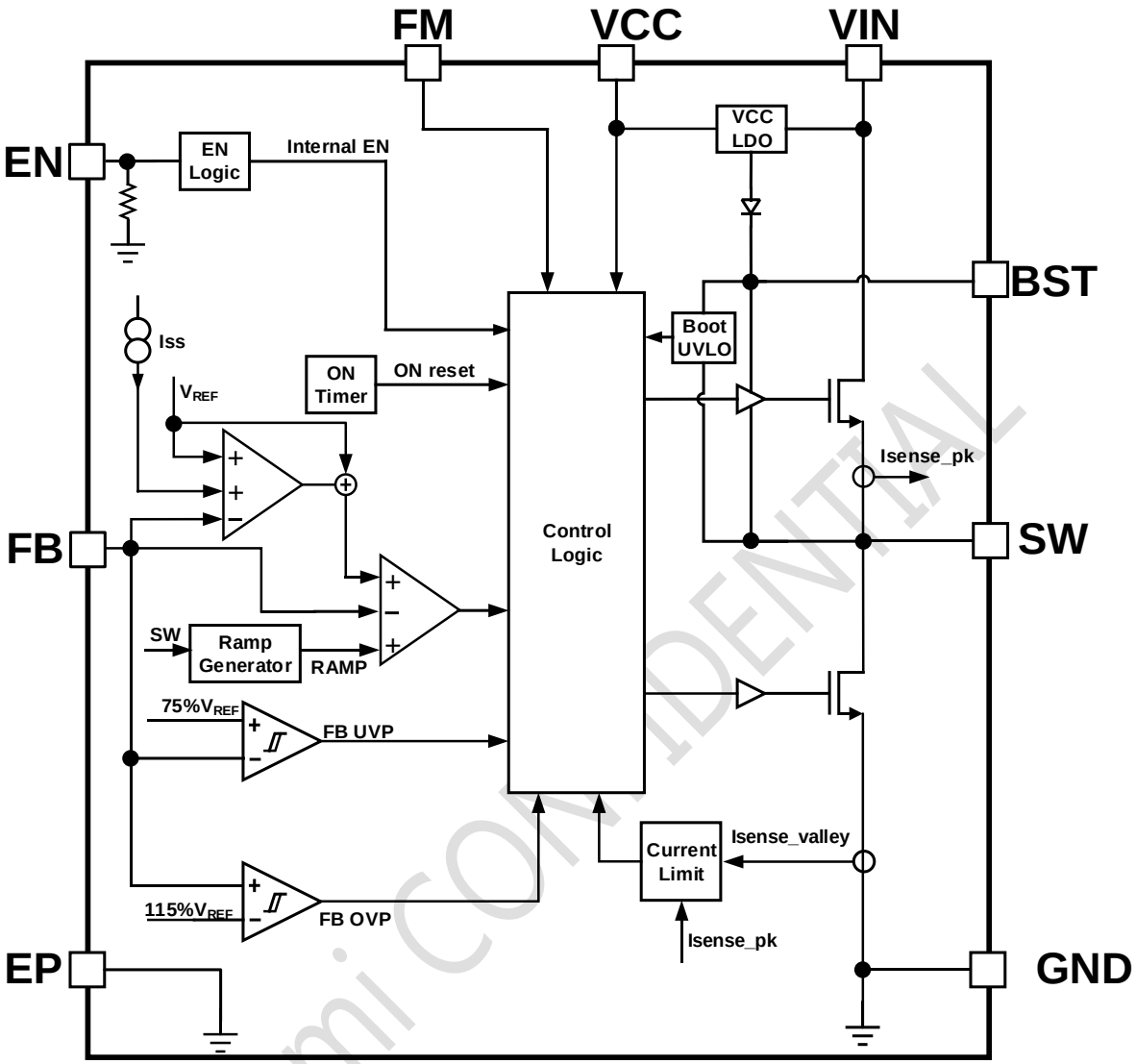


L A 1 3 1 5 E : Lot Number
0 0 L L L L L : Product Code
WWY: Date code

Pin Description

Pin No.	Symbol	Pin Description
1	BST	**Bootstrap pin**. Connect a capacitor between SW and BST pins to form a floating supply across the High-side switch driver. Connect a high quality 100nF capacitor from this pin to the SW pin.
2	VIN	**Input voltage of Buck**. VIN supplies power for the internal MOSFET and regulator. The input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
3	EN	**Enable pin of Buck**. Pull high to enable Buck. Pull to GND or Float this pin to disable Buck.
4	FM	**Operation mode and frequency selection**. Program FM to select CCM, pulse skip mode, and the operating switching frequency. Connect a resistor between FM pin and GND can configure the frequency.
5	FB	**Feedback input to the convertor of Buck**. Connect a resistor divider to set the output voltage.
6	VCC	**Internal 5V LDO regulator output**. Decouple VCC with a 1μF capacitor. The VCC LDO is shutdown when EN is pulled low.
7	GND	**System ground**. GND is the reference ground of the regulated output voltage. Use wide PCB traces to make the connection.
8	SW	**Switching output of the convertor**. Internally connected to source of the high-side FET and drain of the low-side FET of Buck. Connect to power inductor.
9	EP	**Exposed Pad.** Connect exposed pad to the PCB GND plane to achieve good thermal performance.

Block Diagram



Absolute Maximum Ratings(Note 1)

T_A=25°C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
V_{IN}	VIN to GND	-0.3~31	V
EN	EN to GND	-0.3~31	V
SW	SW to GND	-0.7 (-5V in 10ns)~VIN + 0.7	V
BST	BST to SW	-0.3~6	V
All Other Pins		-0.3~6	V
T_{STG}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	-40 to 150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
BST	BST to SW	4~5	V
V_{IN}	VIN to GND	4.5~30	V
V_{OUT}	VOUT to GND	0.8V~VIN	V
I_{OUT}	Max Continuous Output Current	5	A

Thermal Resistance(Note 2)

Symbol	Definition	Ratings	Unit
$R_{\theta JC}$	Junction to case thermal resistance	6	°C/W
$R_{\theta JA}$	Junction to ambient thermal resistance	30	°C/W

Note 2: Measured on Latticeart DEMO DEM1315-E-00A, 4-Layer PCB, 64mm x 64mm board

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Input UVLO and Quiescent Current						
VCC_{UVR}	VIN UVLO rising threshold			3.3		V
VCC_{UVF}	VIN UVLO falling threshold			2.8		V
I_{QS}	Shutdown supply current	V_{IN}=18V		1	3	μA
I_Q	Quiescent supply current	No load, VFB = 0.7V, no switching		350		μA
EN 】						
V_{EN_R}	Enable rising threshold	Low to high		1.25		V
V_{EN_F}	Enable falling threshold	High to low		1.05		V
R_{EN}	Enable input resistor			2400		KΩ
VCC REGULATOR						
V_{CC}	V_{CC} regulator	VIN>5.2V		5		V
I_{VCC}	VCC Current Limit	High to low	20			mA
Buck Feedback Voltage and Soft Start Time						
V_{FB}	Feedback voltage	T_J = 25°C	788	800	812	mV
I_{LK_FB}	Feedback leakage	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
T_{SS}	Soft-start time(Note 3)	V_{OUT} from 10% to 90%		6		ms
I_{SS}	Soft-start current			10		μA
Buck High Side and Low Side MOSFETs						
R_{ON_HS}	High-side switch on resistance	V_{BST} - V_{SW} = 5V		43		mΩ
R_{ON_LS}	Low-side switch on resistance	V_{IN} = 12V		27		mΩ
LKG_{HS}	High-side leakage	V_{EN} = 0V, V_{SW} = 0V			1	μA
LKG_{LS}	Low-side leakage	V_{EN} = 0V, V_{SW} = 18V			1	μA
Output Discharge Resistor						
$R_{DISCHARGE}$				200		Ω
Buck Current Limit						
I_{LIM_LS}	Low-side Valley Current limit			5.5		A
I_{LIM_HS}	High-side Peak Current limit			7		A

Electrical Characteristics

V_{IN}=12V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{NOC}	Negative Current Limit			4		A
Buck Output OVP and UVP						
$V_{OVP\_rising\_th}$	Output OVP rising threshold			115%		V_{FB}
$V_{OVP\_falling\_th}$	Output OVP falling threshold			105%		V_{FB}
$V_{UVP\_falling\_th}$	UVP threshold falling threshold			75%		V_{FB}
$V_{UVP\_rising\_th}$	UVP threshold rising threshold			85%		V_{FB}
Switching Frequency						
F_{SW}	Oscillator frequency	FM=PGND, PFM		250		KHz
		FM=30K, PFM		300		KHz
		FM=75K, PFM		400		KHz
		FM=150K, CCM		400		KHz
		FM=270K, CCM		300		KHz
		FM Float, CCM		250		KHz
T_{ON_MIN}	Minimum switch on time(Note 3)			70		ns
T_{OFF_MIN}	Minimum switch off time(Note 3)			150		ns
FB_{UV}	FB UV hiccup			75%		V_{FB}
T_{OTP_R}	Thermal shutdown rising threshold(Note 3)			160		°C
T_{OTP_F}	Thermal shutdown falling threshold(Note 3)			130		°C

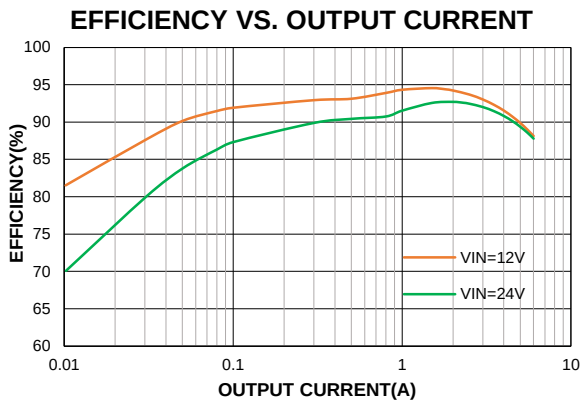
Note 3: Not tested in production and derived from bench characterization.

Typical Performance Characteristic

V_{IN} = 12/24V, V_{OUT} = 5V, F_{SW}=300KHz, Mode=PFM, C_{IN} = 22μF, C_{OUT} = 4*22μF, L1 =10μH, and T_A = +25°C, unless otherwise noted.

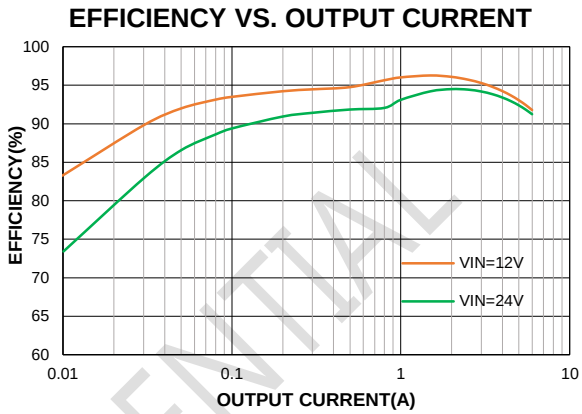
Efficiency

V_{OUT}=3.3V, Lout=6.8μH, DCR=25mohm



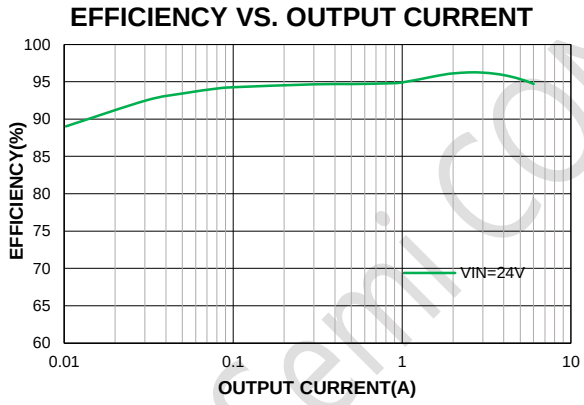
Efficiency

V_{OUT}=5V, Lout=10μH, DCR=30mohm



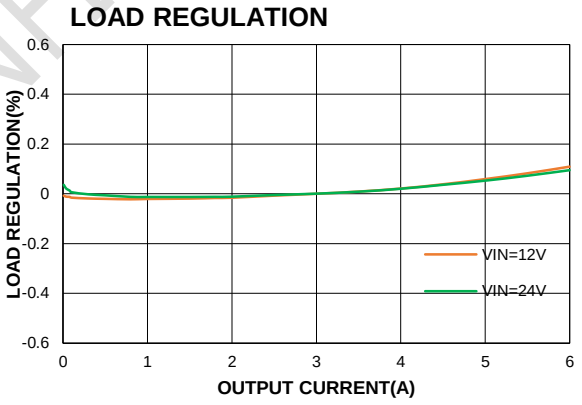
Efficiency

V_{OUT}=12V, Lout=10μH, DCR=30mohm



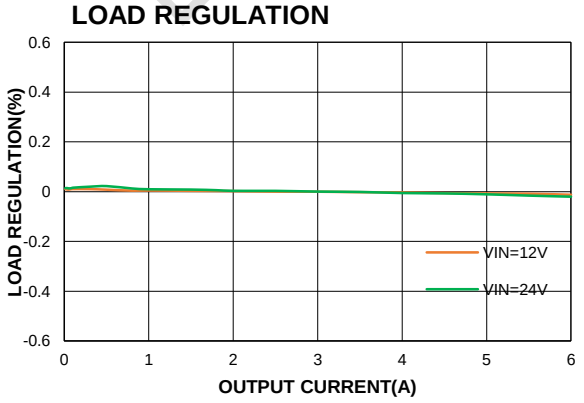
Load Regulation

V_{OUT}=3.3V, Lout=6.8μH



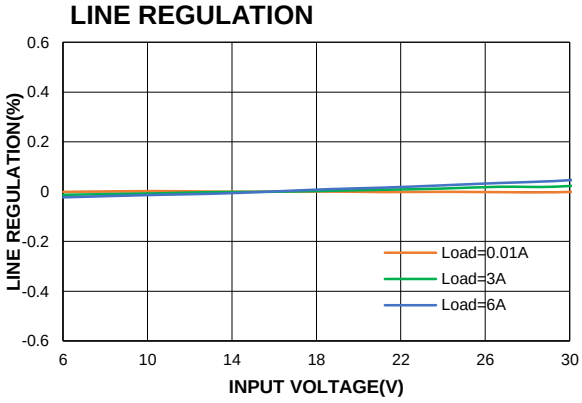
Load Regulation

V_{OUT}=5V, Lout=10μH



Line Regulation

V_{OUT}=3.3V

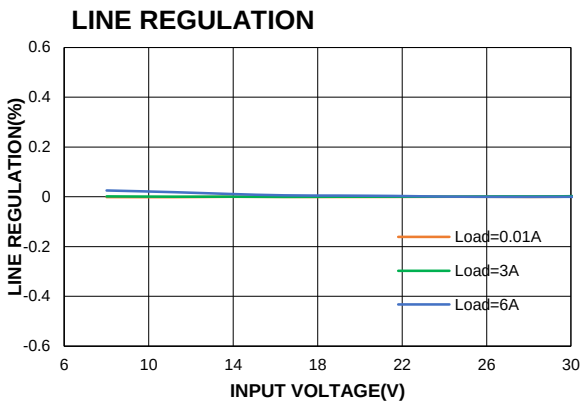


Typical Performance Characteristic

V_{IN} = 12/24V, V_{OUT} = 5V, F_{SW}=300KHz, Mode=PFM, C_{IN} = 22μF, C_{OUT} = 4*22μF, L1 =10μH, and T_A = +25°C, unless otherwise noted.

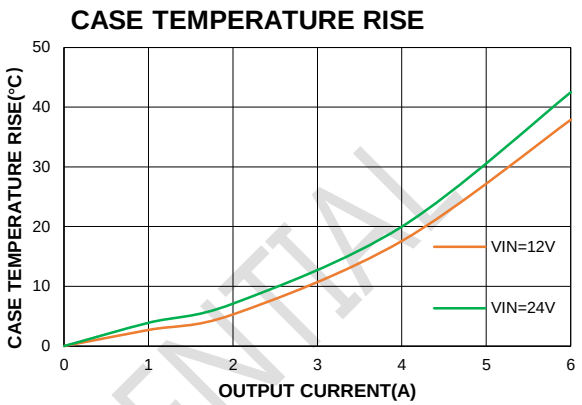
Line Regulation

V_{OUT}=5V



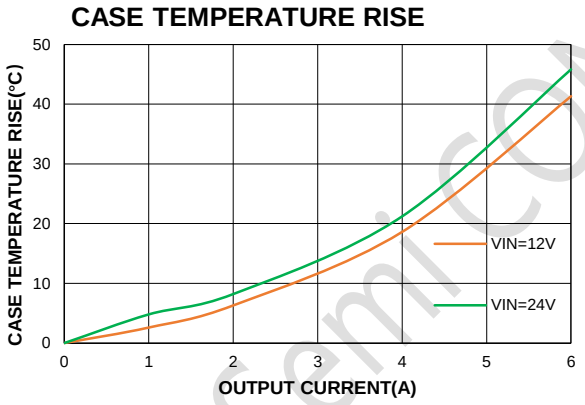
Case Temperasise

V_{OUT}=3.3V, Lout=6.8μH, DCR=25mohm



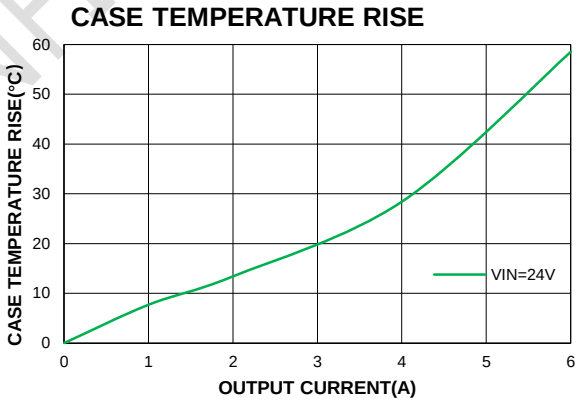
Case Temperasise

V_{OUT}=5V, Lout=10μH, DCR=30mohm



Case Temperasise

V_{OUT}=12V, Lout=10μH, DCR=30mohm



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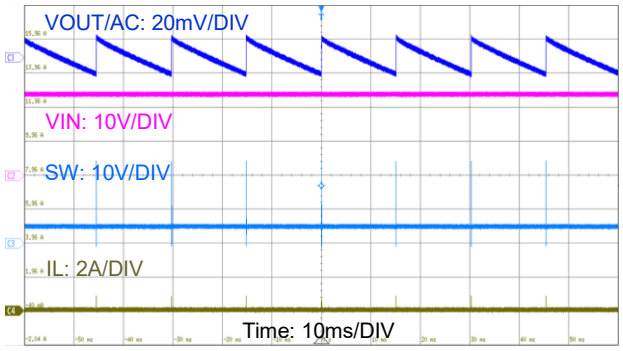
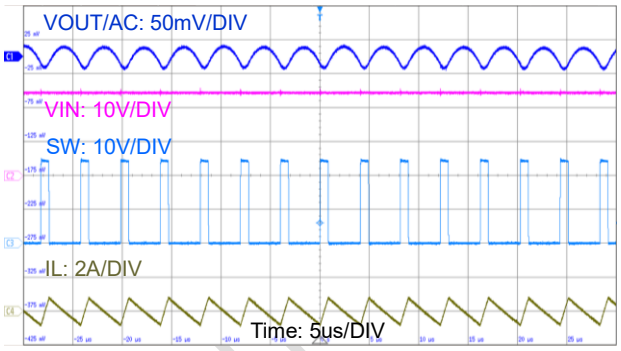
Output Voltage Ripple

IOUT = 0A, PFM



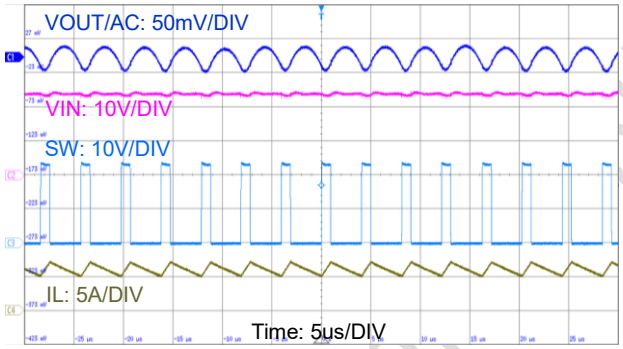
Output Voltage Ripple

IOUT = 0A, FPWM



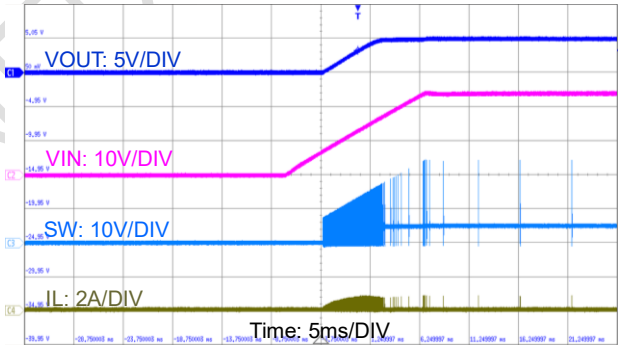
Output Voltage Ripple

IOUT = 5A



Start-Up through VIN

IOUT = 0A, PFM



Start-Up through VIN

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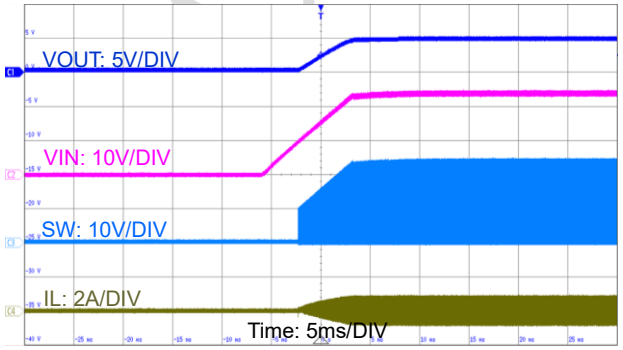
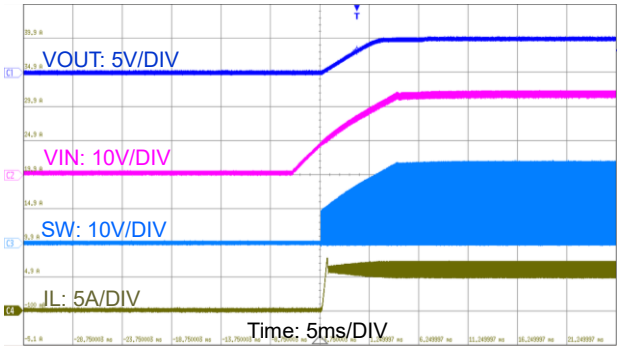


Start-Up through VIN

IOUT = 5A



Typical Performance Characteristic

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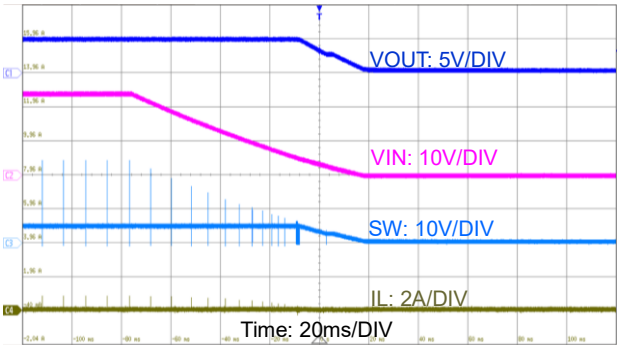
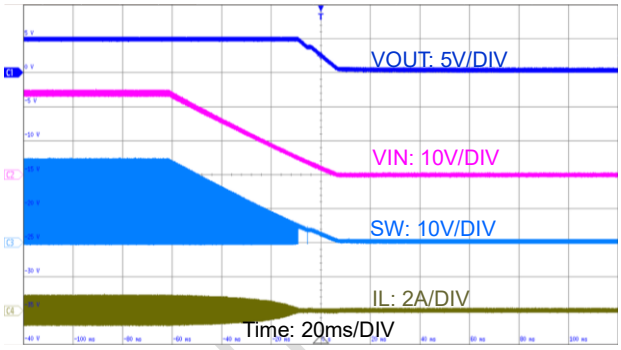
Shutdown through VIN

IOUT = 0A, PFM



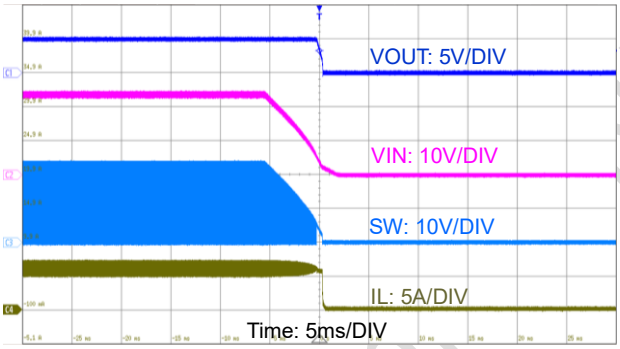
Shutdown through VIN

IOUT = 0A, FPWM



Shutdown through VIN

IOUT = 5A



Start-Up through EN

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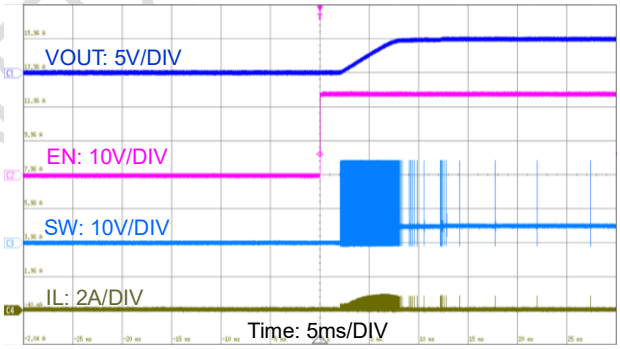

Start-Up through EN

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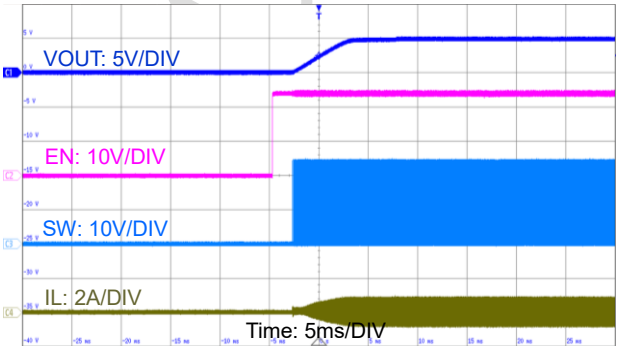
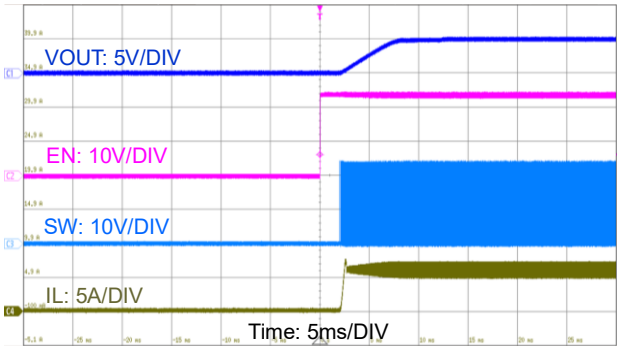


Start-Up through EN

IOUT = 5A



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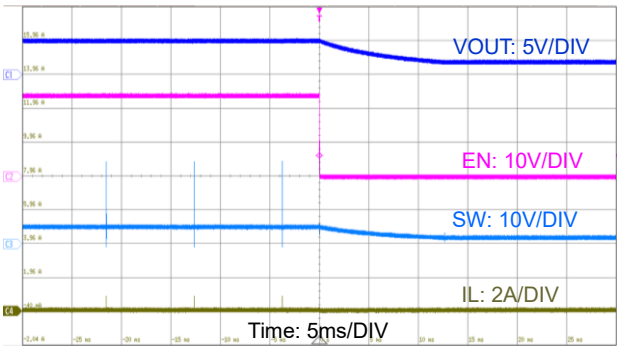
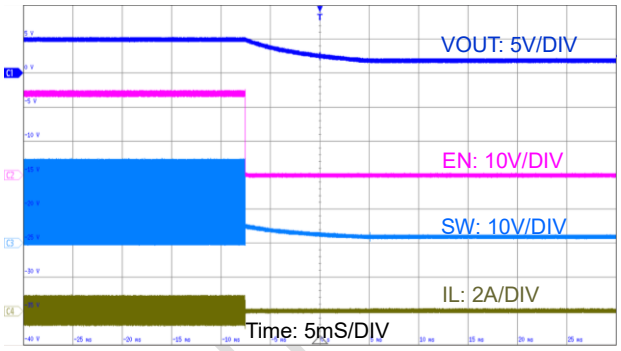
Shutdown through EN

IOUT = 0A, PFM



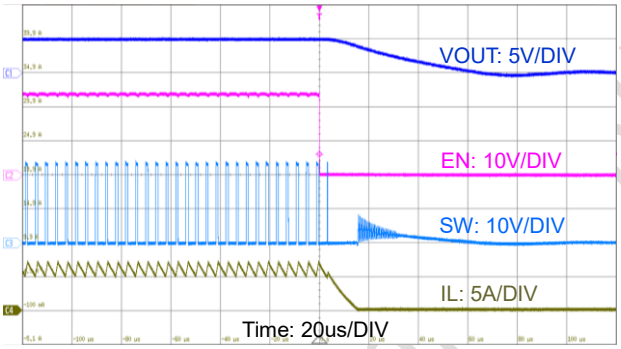
Shutdown through EN

IOUT = 0A, FPWM



Shutdown through EN

IOUT = 5A



Short Entry

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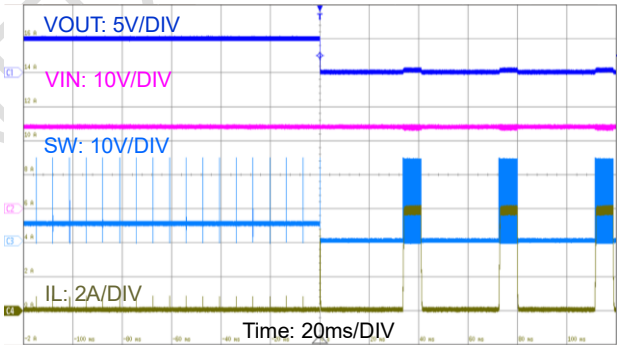

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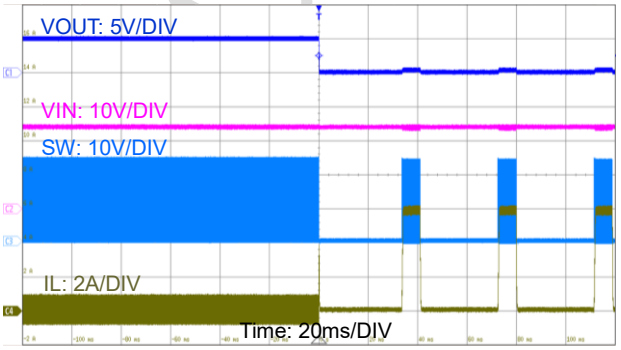
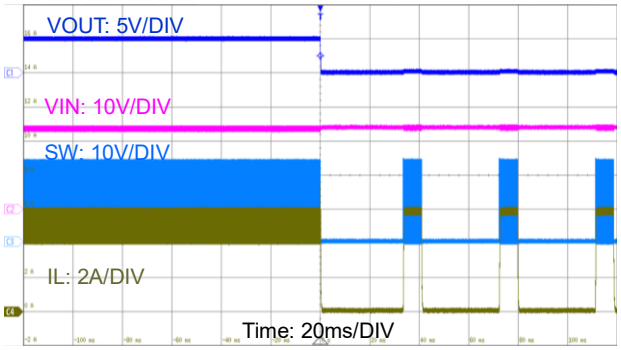


Short Entry

IOUT = 5A



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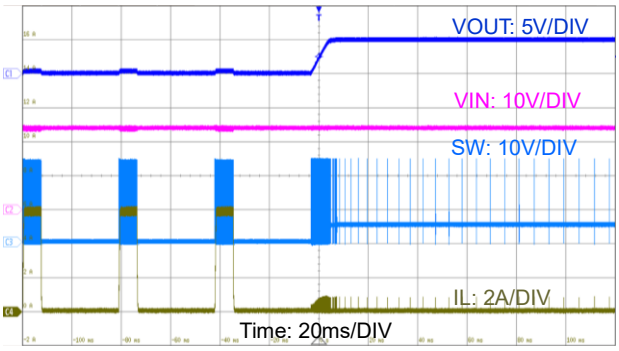
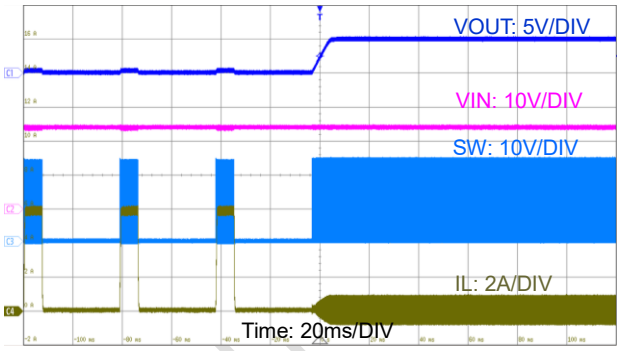
Short Recovery

IOUT = 0A, PFM



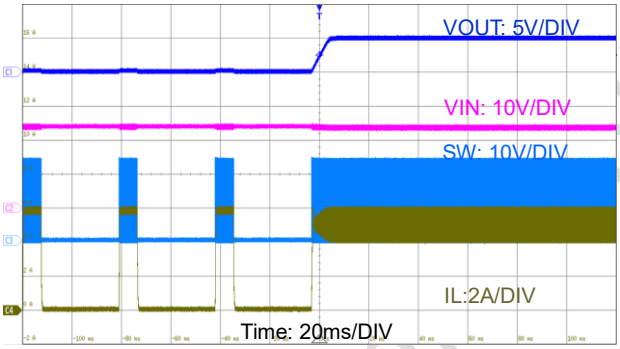
Short Recovery

IOUT = 0A, FPWM



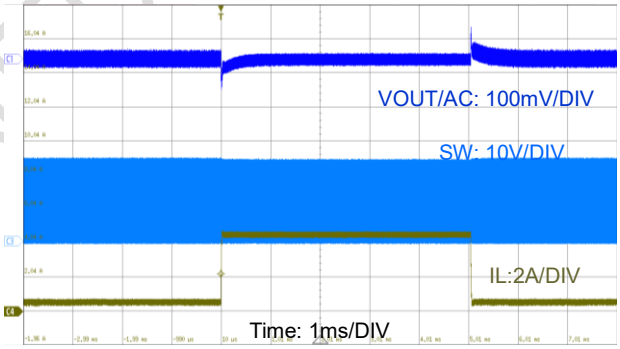
Short Recovery

IOUT = 5A



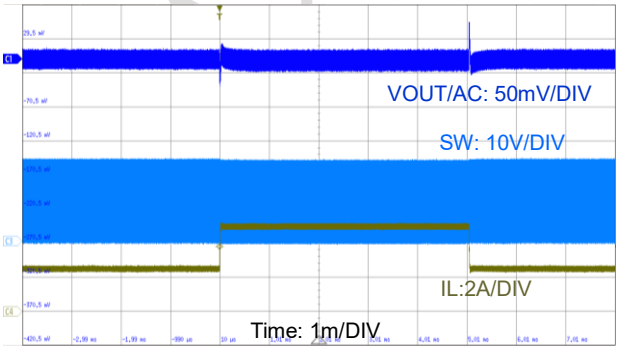
Load Transient

IOUT = 0.5A to 5A



Load Transient

IOUT = 2.5A to 5A



Function Descriptions

Pulse-Width Modulation (PWM) Control

The LA1315E is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS- FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS- FET off and HS-FET on period.

Internal compensation is applied for COT control to provide a more stable operation, even when ceramic capacitors are used as output capacitors. This internal compensation improves jitter performance without affecting the line or load regulation.

Heavy-Load Operation

Continuous conduction mode (CCM) is when the output current is high and the inductor current is always above zero amps (see Figure 1). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-FET is turned on until the next period begins. In CCM operation, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

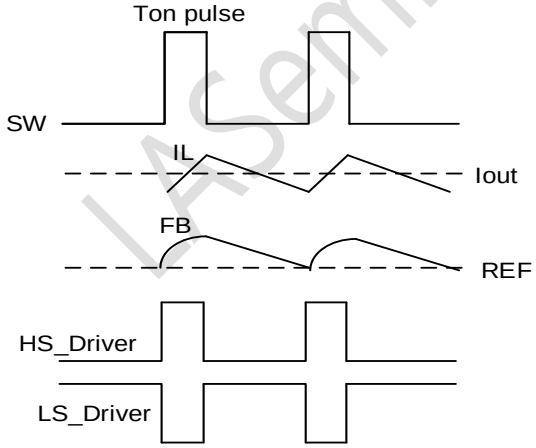


Figure 1. FPWM Operation

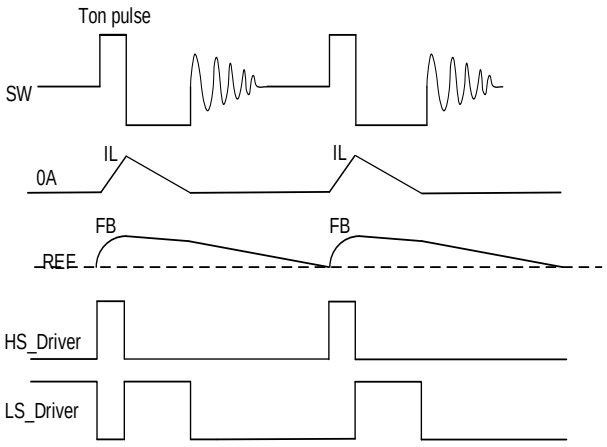


Figure 2. PFM Operation

Light-Load Operation

When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the operation transitions from CCM to discontinuous conduction mode (DCM).

Light-load operation is shown in Figure 2. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on- timer. When the HS-FET is turned off, the LS- FET

is turned on until the inductor current reaches zero. In DCM operation, V_{FB} cannot reach V_{REF} while the inductor current is approaching zero. The LS-FET driver enters tri- state (Hi-Z) whenever the inductor current reaches zero. The output capacitors discharge to GND through the LS- FET slowly. As a result, the efficiency in light- load condition is improved greatly. In light-load condition, the HS-FET is not turned on as frequently as it is in heavy-load condition. This is called skip mode.

At light-load or no-load condition, the output drops very slowly, and the LA1315E reduces the switching frequency naturally. High efficiency is achieved at light load.

As the output current increases from the light- load condition, the current modulator regulation time period becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$\mathbf{I_{OUT\_Critical}} = \frac{(\mathbf{V_{IN}} - \mathbf{V_{OUT}}) \times \mathbf{V_{OUT}}}{\mathbf{2} \times \mathbf{L_{OUT}} \times \mathbf{F_{SW}} \times \mathbf{V_{IN}}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Under-Voltage Lockout (UVLO) Protection

The LA1315E has under-voltage lockout (UVLO) protection: the part starts up only when VIN/VCC UVLO threshold (3.3V typically). The part shuts down when the VIN/VCC voltage is lower than the UVLO falling threshold voltage (typically 2.8V), the UVLO protection is non-latch off.

EN Control

EN is used to enable or disable the entire chip. Pull EN high(1.25V typically) to turn on the regulator. Pull EN low(<1.05V typically) to turn off the regulator. For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. To determine the automatic start-up voltage, calculate the values of the pull-up resistor (R_{UP} from VIN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) with Equation (2):

$$\mathbf{VIN\_start} = \frac{\mathbf{1.3V} * (\mathbf{R_{UP}} + \mathbf{R_{DOWN}})}{\mathbf{R_{DOWN}}} \quad (2)$$

If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see Figure 3).

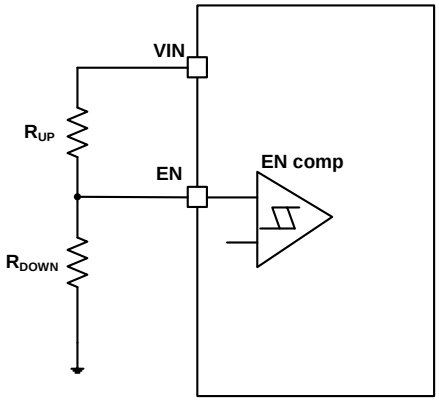


Figure 3: Adjustable UVLO Application Circuits

Soft Start (SS)

The LA1315E employs a soft-start mechanism to ensure a smooth output during power-up. When the chip starts (both EN>1.25V and VIN/VCC is above UVLO), the internal circuitry generates a soft-start voltage (VSS) that ramps up linearly. When SS is below REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS exceeds REF, the error amplifier uses REF as the reference. Soft-start time is fixed 6mS (typically 10% Vout to 90% Vout).

Pre-bias Start-up

If the output is pre-biased to a certain voltage during start-up, the LA1315EE disables the switching of both the high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

Over-Current Limit (OCL)

The LA1315E has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the RDS(ON) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle, even if FB is lower than REF (see Figure 6).

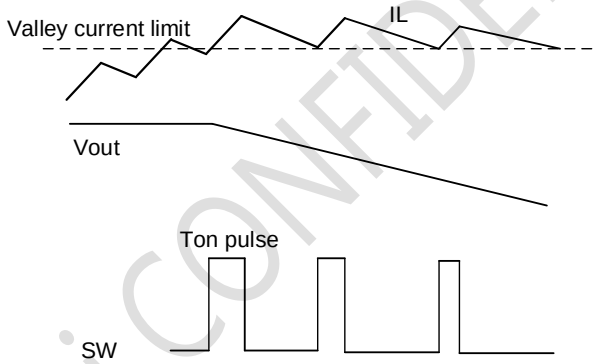


Figure 4: Valley Current-Limit Control

Since the comparison is done during the LSFET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (IOC) can be calculated with Equation (4):

$$\mathbf{I_{OC}} = \mathbf{I_{LIMIT}} + \frac{\Delta \mathbf{I_{inductor}}}{\mathbf{2}} \quad (3)$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, causing the output voltage to fall off. Eventually, the current crosses the under-voltage protection (UVP) threshold and enters the hiccup protection.

OVP/UVP

The LA1315E monitors a resistor-divided VFB to detect over- and under-voltage. When VFB becomes higher than 115% of the target voltage, the over-voltage protection (OVP) comparator output goes high, and the circuit will turn on the low side MOSFET to discharge the output. LSFET will turned off until the negative current limit is triggered then LSFET will remain off for 5us to turn on again. IC will repeat this behavior until the output OVP condition is removed.

When VFB drops below 75% of VREF, the UVP comparator output goes high, and the LA1315E enters the hiccup protection.

FM Select Frequency/Mode Programmable

The LA1315E can setup the operation mode and PWM frequency by connecting FM pin to GND with a resistor. Below table shows the configuration

Table 1. Frequency and Mode configuration

R_{FM}(kΩ)	Work Mode	Frequency(KHz)
0	PFM	250
30	PFM	300
75	PFM	400
150	FPWM	400
270	FPWM	300
Float	FPWM	250

Large Duty Cycle Operation

When LA1315E will automatically extend the frequency to support the application when VIN is close to VOUT. The frequency extend circuit will be triggered when Toff min time is reached. The LA1315E can support up to 100% duty cycle. Large duty cycle operation is disabled when OC is triggered.

Thermal Shutdown

Thermal shutdown is employed in the LA1315E. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off. This is a non-latched protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start is initiated.

Output Discharge

During the EN off period, the output is discharged via a 200Ω resistor on the SW. This discharge FET is turned off when VOUT is fully discharged or the 10ms timer is finished.

Application Information

Setting the Output Voltage

The LA1315BD output voltage can be set by the external resistor dividers. The reference voltage is fixed at 0.8V. The feedback network is shown below Figure 6.

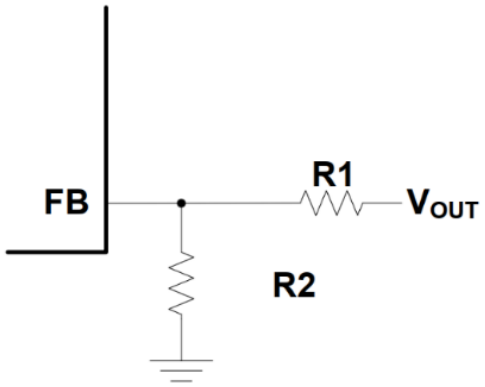


Figure 5: Feedback Network

Choose R_1 and R_2 using Equation (4):

$$V_{OUT} = V_{FB} \times \frac{(R_1 + R_2)}{R_2} \quad (4)$$

Table 2 lists the recommended feedback resistor values for common output voltages.

Table 2: Resistor Selection for Common Output Voltages (Note 4) (Note 5)

VIN(V)	V_{OUT} (V) Note 5	R1 (kΩ)	R2 (kΩ)	C3(pF)	Lout(μH)	C_{OUT} (μF)
12	3.3	40.7	13	100	4.7	47x2
	5	68	13	100	6.8	47x2
	9	133	13	100	6.8	47x2
24	3.3	40.7	13	100	6.8	47x2
	5	68	13	100	10	47x2
	9	133	13	100	10	47x2
	12	182	13	100	10	47x2
	15	232	13	100	10	47x2
	20	312	13	100	10	47x2

Note 4: For a detailed design circuit, please refer to the Typical Application Circuits.

Note5: The table recommends parameters based on Fsw=300KHz

Selecting the Inductor

For most applications, use a 4.7μH to 15μH inductor with a DC current rating at least 25% higher than the maximum load current. For the highest efficiency, use an inductor with a small DC resistance.

For most designs, the inductance value can be derived from Equation (5):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{sw}} \quad (5)$$

Where ΔI_L is the inductor ripple current.

Table 3 lists the recommended values of inductor at different frequency:

Table 3: Power Inductor Selection

V_{IN} (V)	F_{SW} (KHZ)	L1 (μH)
12	250	8.2
	300	6.8
	400	4.7
24	250	15
	300	10
	400	6.8

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage ripple. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (6):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_{sw} \times C_{OUT}}\right) \quad (6)$$

Where L is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor.

The characteristics of the output capacitor also affect the stability of the regulation system. The LA1315E can be optimized for a wide range of capacitance and ESR values.

PCB layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design may cause poor line or load regulation and stable issues. For best results, refer to below figure and follow the guidelines below and take figures as the reference.

- The high current paths (GND, VIN and SW) should be placed very close to the device with short, direct and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the VCC bypass capacitor as close to VCC as possible.
- Keep the switching node (such as SW) far away from the Vout sense network.
- Add a grid of thermal vias under the exposed pad to improve thermal conductivity.

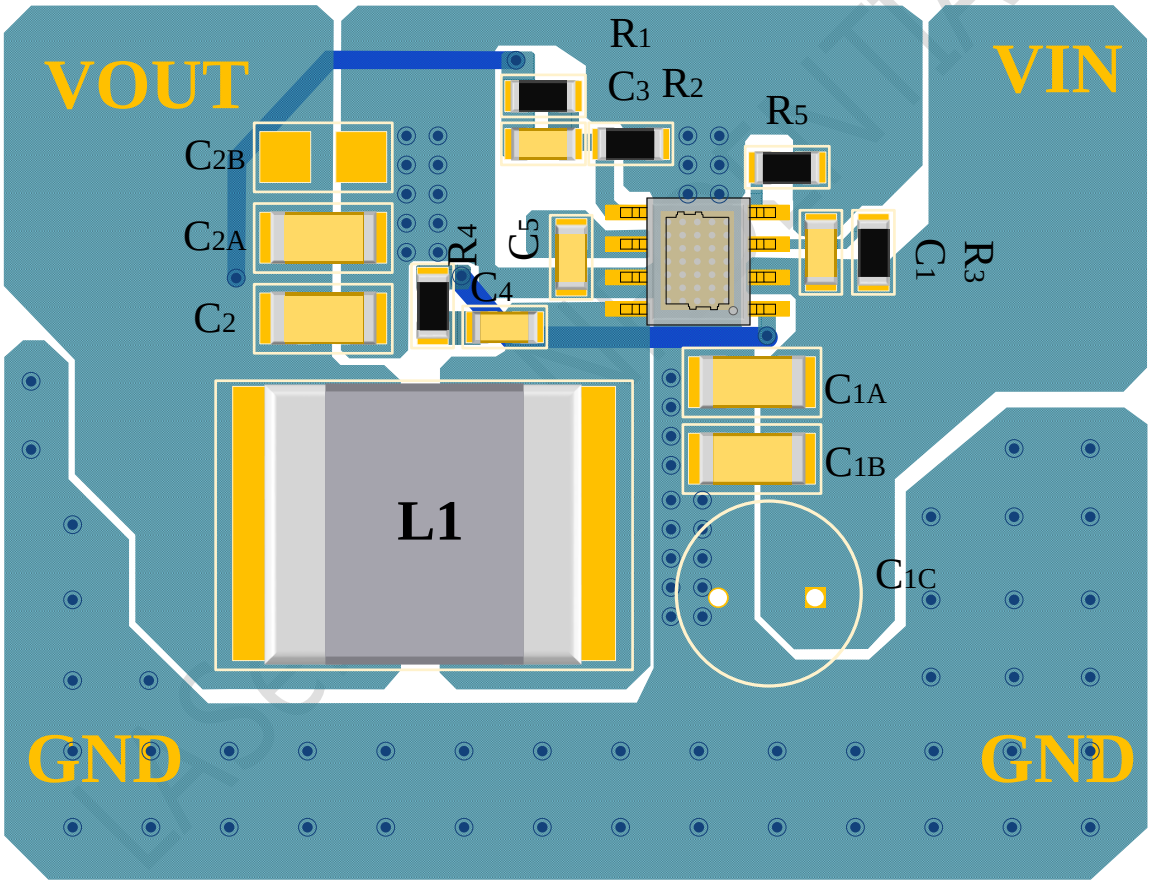
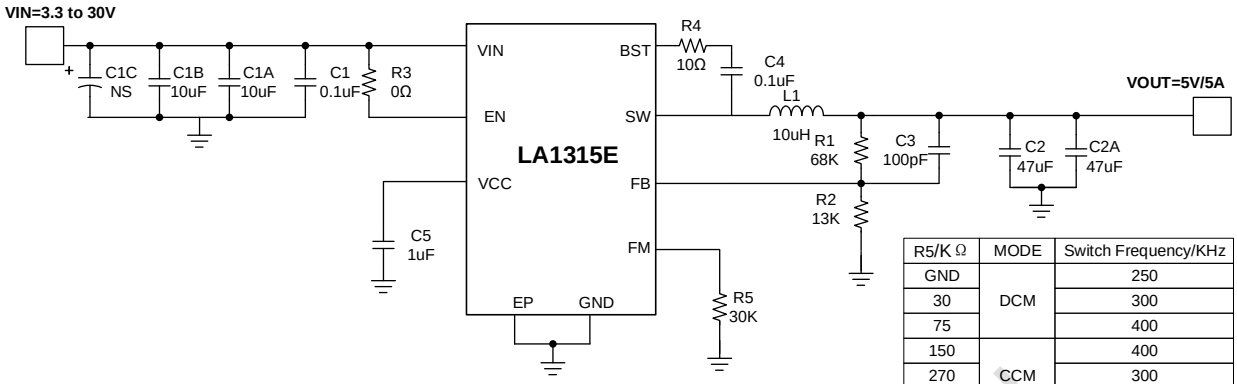


Figure 6. Recommend PCB Layout

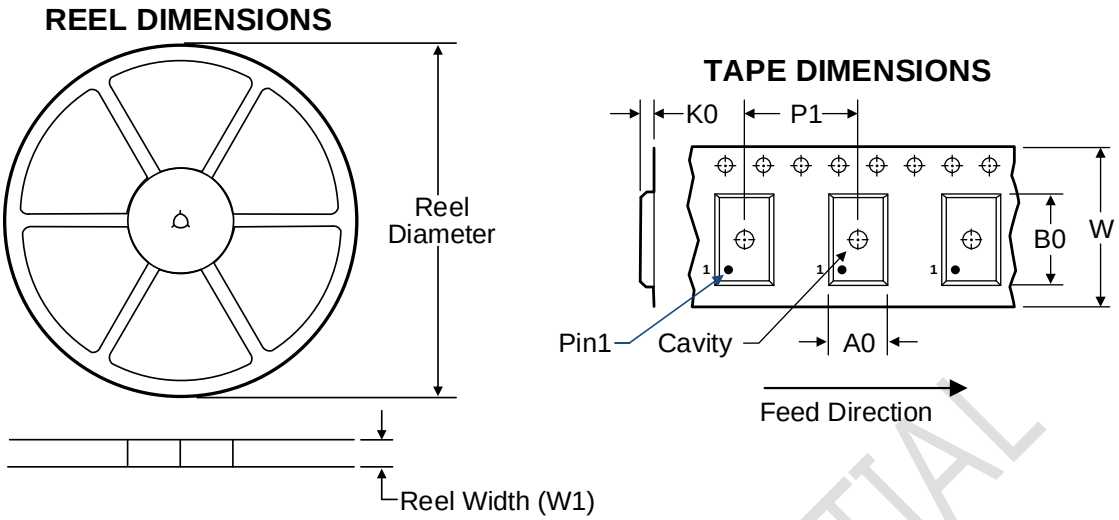
Typical Application Circuits



R5/K Ω	MODE	Switch Frequency/KHz
GND	DCM	250
30		300
75		400
150	CCM	400
270		300
Float		250

Figure 7. Vout=5V Typical Application Circuits

Tape and Reel Information



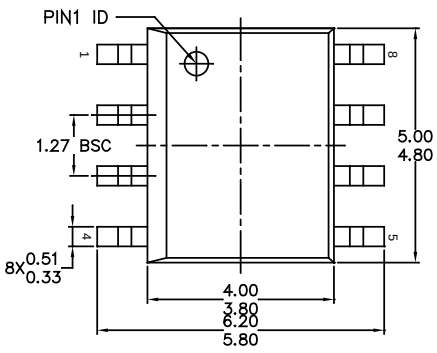
Information (Note 6)

Device	Package Type	Pins	SPQ	Real Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LA1315E	ESOP8	8	2500	330	12.4	6.6	5.3	1.9	8	12

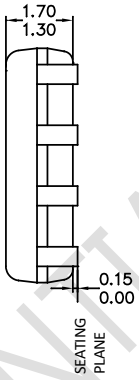
Note 6: Drawing is not to scale.

Detail Package Outline Drawing

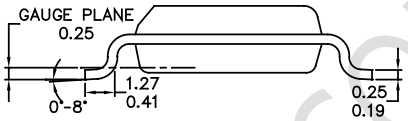
PACKAGE TYPE: ESOP8



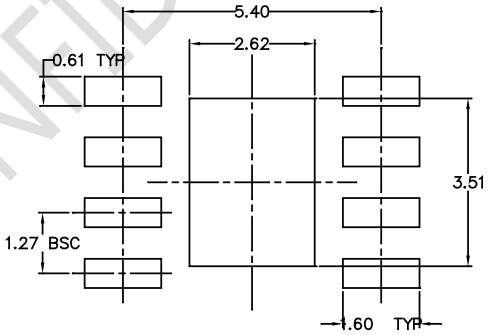
TOP VIEW



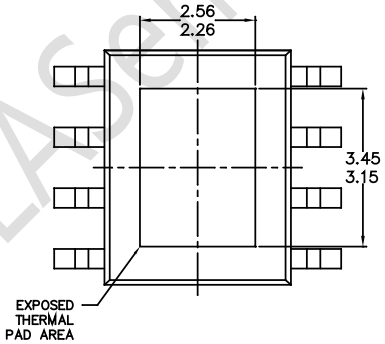
SIDE VIEW



FRONT VIEW



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTE:
1) CONTROL DIMENSION IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) EXPOSED TIE BAR FEATURE IS OPTIONAL. EXPOSED PAD SIZE DOES NOT INCLUDE TIE BAR FEATURE.

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