Low Additive Jitter, Twelve LVDS Outputs Clock Buffer Evaluation Board

This user's guide describes how to use the CDCLVD1212/CDCLVD2106 evaluation module (EVM) and provides users with guidelines to build their own systems. The EVM schematics and bill of materials are included.

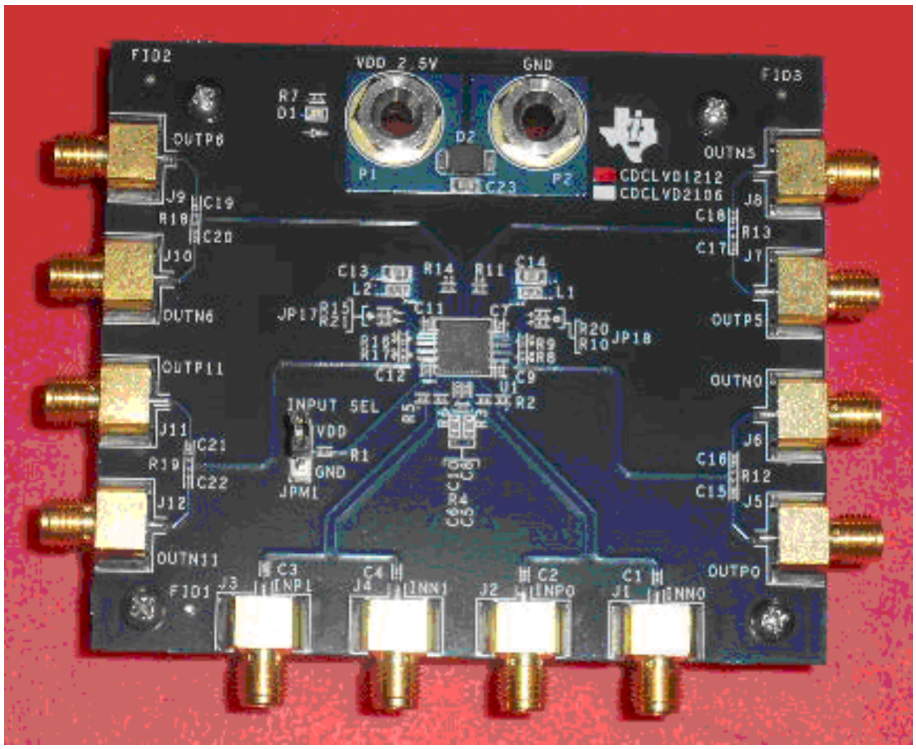

Figure 1. CDCLVD1212/ CDCLVD2106 Evaluation Board

1 Features

- Easy to Use Evaluation Board to Fan-out Low Phase Noise Clocks
- Easy Device Setup
- Fast Configuration
- Control Pins Configurable through Jumpers
- Board and Device Powered at 2.5V
- Single Ended or Differential Input Clocks
- Device Supports 12 LVDS Outputs, EVM Supports 4 LVDS Outputs

2 General Description

The CDCLVD1212 and CDCLVD2106 are high performance low additive phase noise clock buffers. The devices have two universal input buffers, that supports single ended or differential clock inputs, and selectable through a control pin (for CDCLVD1212 only). The devices also feature on-chip bias generators that can provide the LVDS common mode voltage to the device inputs.

The **Ev**aluation **M**odule (EVM) is designed to demonstrate the electrical performance of the CDCLVD1212 or CDCLVD2106. This fully assembled and factory tested evaluation board allows complete validation of device functionalities. For optimum performance, the board is equipped with SMA connectors and well-controlled 50Ω impedance micro strip transmission lines.

3 Signal Path and Control Circuitry

The CDCLVD1212 and CDCLVD2106 support single ended inputs up to 200MHz and differential inputs up to 800MHz. Each device provides up to 12 LVDS outputs operating at the input frequency or frequencies.

For more information, see the CDCLVD1212 or CDCLVD2106 product data sheet for details.

4 Getting Started

The EVM has self-explanatory labeling and offers almost same naming convention as used in the data sheet. All words in bold and italics print in this document is the actual labeling on the EVM. The EVM can be used with single ended or differential inputs.

5 Device Selection

Same EVM is used for both CDCLVD1212 (2:12 single buffer) and CDCLVD2106 (1:6 dual buffer). The assembled product is highlighted with a marker in front of the silkscreen.

6 Power Supply Connection

Connect the power supply source to banana plug labeled ***VDD (P1)*** and connect the ground of the power supply source to the ***GND (P2)***. There are decoupling capacitors and ferrite bead to isolate the EVM power from the device's power pins.

2.375 – 2.625V supply voltage can be used in this EVM.

7 Input Clock Selection

The CDCLVD1212and CDCLVD2106EVM offer options of receiving either differential or single ended clock as clock input. The default option is for the differential signal at both device inputs. The inputs can be applied through the SMAs, ***J1, J2*** and ***J3, J4***. These inputs are ac coupled to the device inputs and the common mode voltage for these inputs after the ac coupling capacitors are provided by 50Ω (***R2, R3*** and ***R5, R6***) to the device on-chip bias generator (V_{AC_REF}) pins.

CDCLVD1212: Either of the 2 input clocks can be selected using the jumper ***JPM1***. When pin 2 of ***JPM1*** jumper is connected to ***GND***, IN0 is selected and connected to ***VDD***, IN1 is selected. The jumper must be used in JPM1, otherwise all ouptuts and inputs will be disabled.

7.1 Configuring Single-Ended Input

For single ended clock applied to IN0, remove the capacitors ***C1*** and ***C2*** and replace them with 0Ω resistors of the same footprint and also remove ***R2 and R3*** the biasing resistors. The single ended signal should be applied to ***INP0 (J2)*** and the DC bias voltage should be applied to ***INN0 (J1)***.

For single ended clock applied to IN1, remove the capacitors ***C3*** and ***C4*** and replace them with 0Ω resistors of the same footprint and also remove ***R5*** and ***R6*** the biasing resistors. The single ended signal should be applied to ***INP1 (J3)*** and the DC bias voltage should be applied to ***INN1 (J4)***.

8 Output Clock

The CDCLVD1212 and CDCLVD2106 generate up to 12 LVDS outputs and 4 outputs are available on the EVM (OUT0, OUT5, OUT6 and OUT11) through the following SMAs: ***J5*** and ***J6*** for OUT0; ***J7*** and ***J8*** for OUT5; ***J9*** and ***J10*** for OUT6; ***J11*** and ***J12*** for OUT11. The LVDS outputs are AC coupled to the respective SMAs. Each output pair has an option of 100Ω termination on the board (***R12, R13, R18*** and ***R19*** – not populated).

All other outputs have test points.

CDCLVD2106: Using the control pin EN (labeled as ***JPM1***), outputs can be disabled or enabled.

Table 1. Output Control for CDCLVD2106

EN (*JMP1*)	CLOCK OUTPUTS
0 (GND)	All outputs disabled (static "0")
OPEN	All outputs enabled
1 (VDD)	OUT0, OUT5 enabled and OUT6, OUT11 disabled (static “0”)

9 EVM Board Schematic and Bill of Materials

9.1 EVM Board Schematic

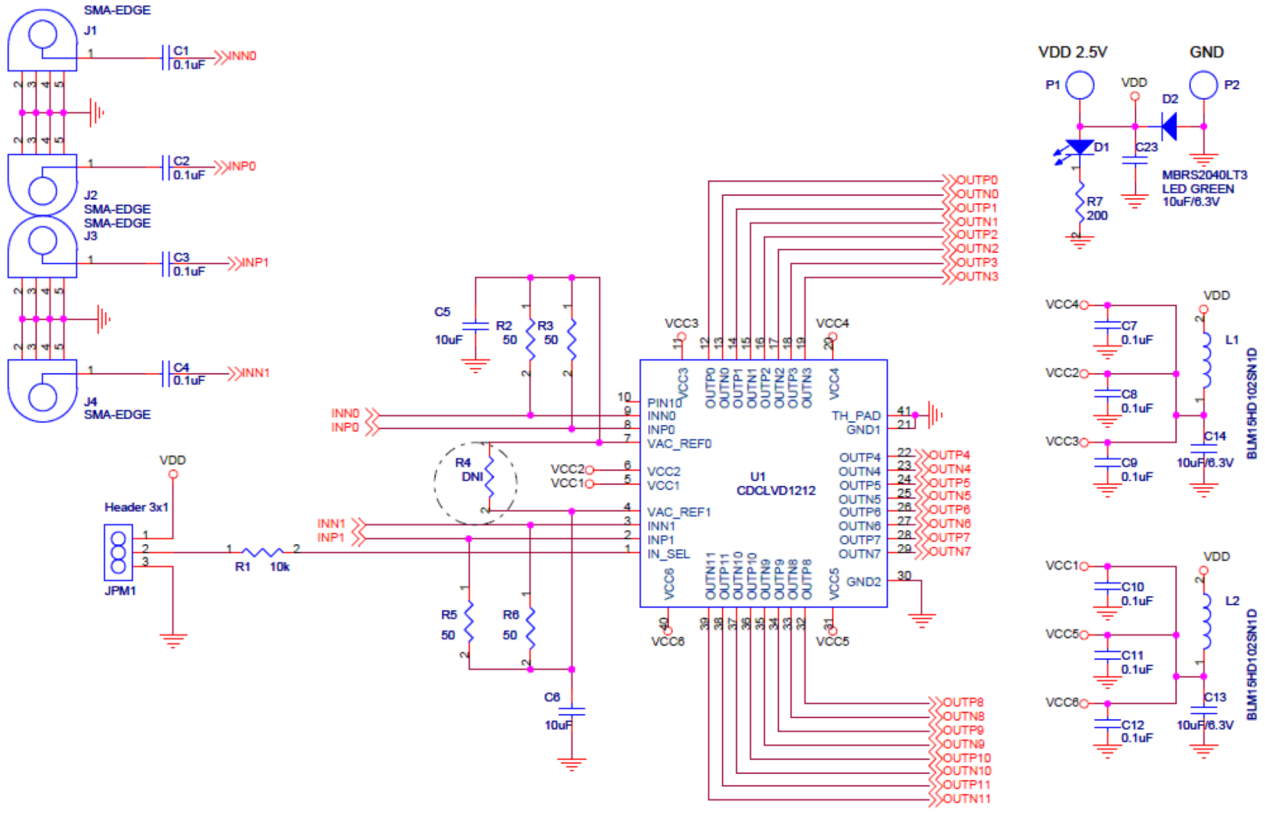

Figure 2. CDCLVD1212/CDCLVD2106EVM – Schematic (Page 1 of 3)

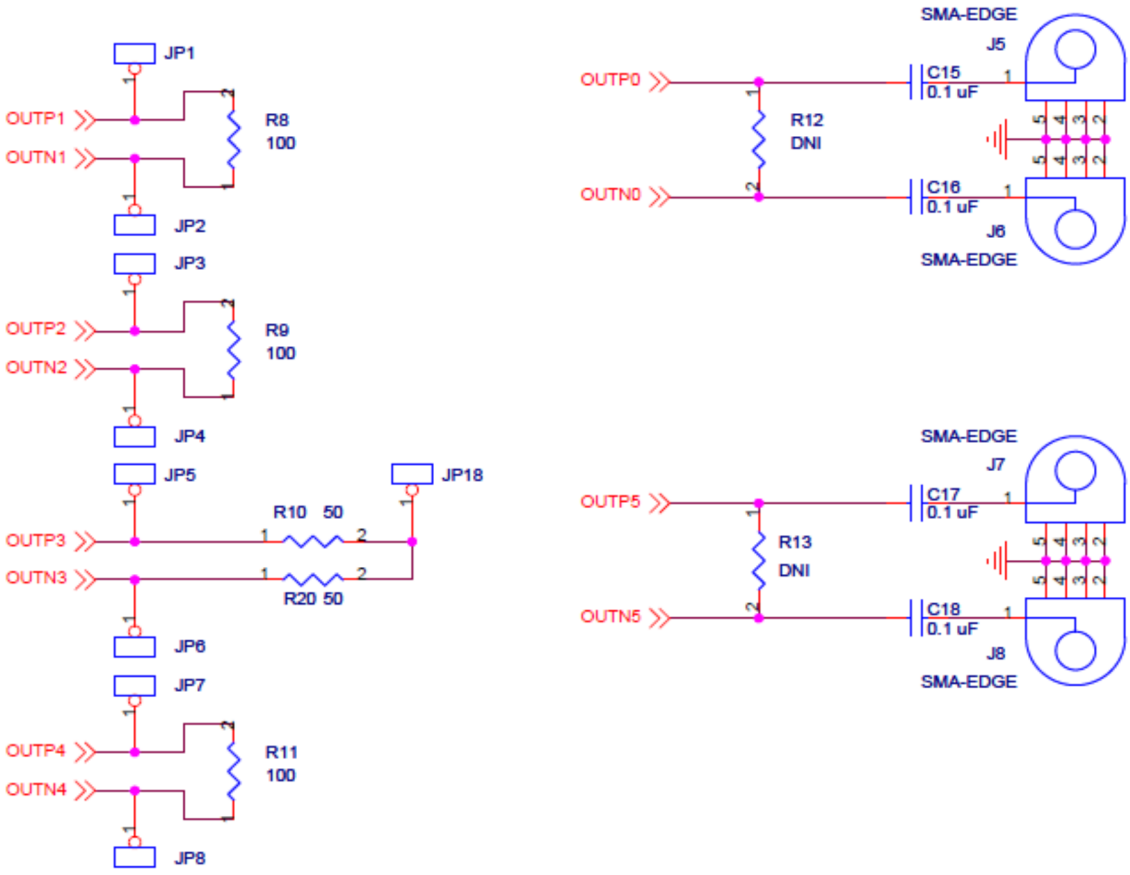

Figure 3. CDCLVD1212/CDCLVD2106EVM – Schematic (Page 2 of 3)

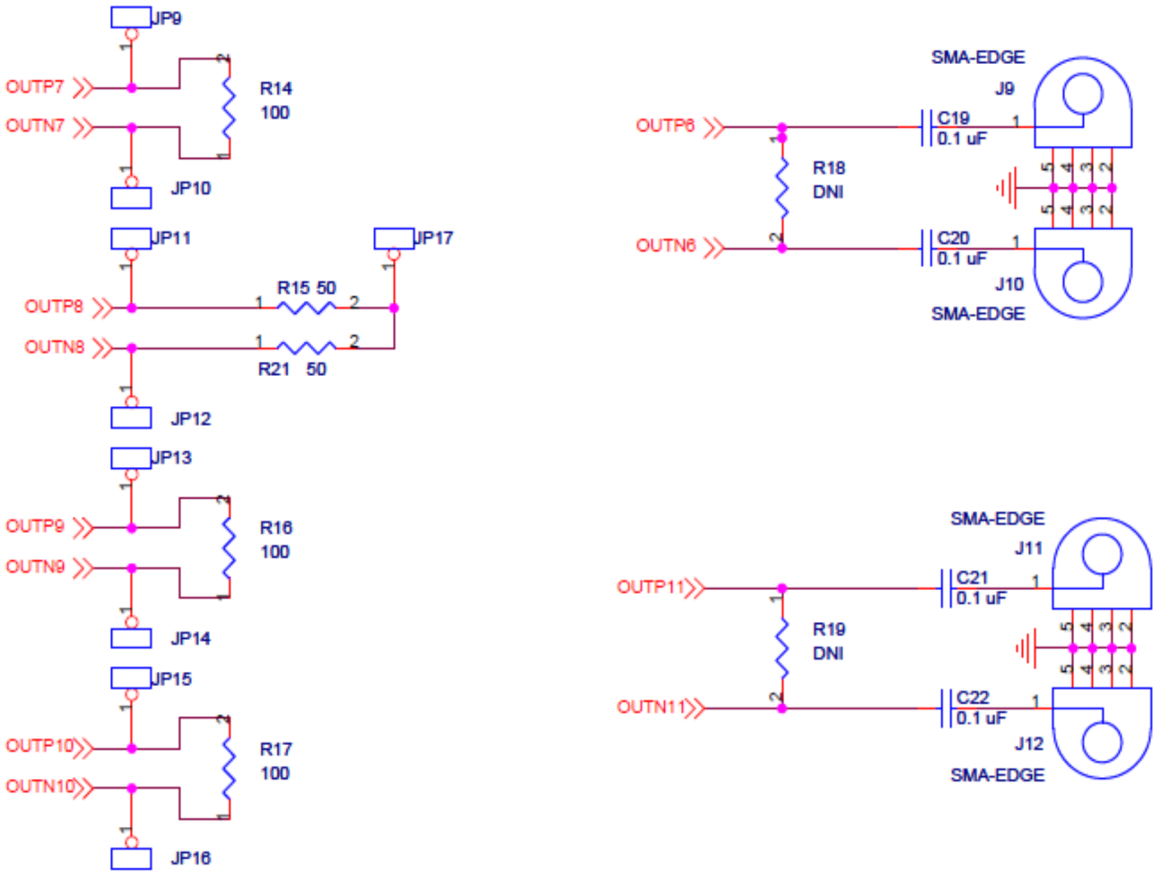

Figure 4. CDCLVD1212/CDCLVD2106EVM – Schematic (Page 3 of 3)

9.2 Bill of Materials

Ref Des	Footprint	Part Category	Manufacturer	Manufacturer Part No
C1–C4,C7–C12	0402	Capacitors	Venkel	C0402X7R160-104KNE
C15–C22	0402	Capacitors	Venkel	C0402X7R160-104KNE
R1	0402	Resistors	Rohm	MCR01MZPF1002
C13, C14, C23	0805	Capacitors	Murata Electronics North America	GRM21BR71A106KE51L
R8, R9, R11, R14, R16, R17	0402	Resistors	Venkel	CR0402-16W-1000FT
R7	0402	Resistors	Venkel	CR0402-16W-2000FT
R2, R3, R5, R6, R10, R15, R20, R21	0402	Resistors	Venkel	CR0402-16W-49R9FT
C5, C6	0603	Capacitors	Panasonic	ECJ-1VB0J106M
L1, L2	0603	Filters	Murata Electronics North America	BLM18HE102SN1D
D2	SMB	Discrete Semiconductor Products	ON Semiconductor	MBRS240LT3G
D1	0603	Optoelectronics	Lite-On	LTST-C190GKT
U1	40-HQFN	Integrated Circuits	Texas Instruments	CDCLVD1212/ CDCLVD2106
P1, P2	4mm	Connectors	Emerson Network Power Connectivity Solutions	108-0740-001
J1–J12	RF SMA Edge mount	Connectors	Emerson Network Power Connectivity Solutions	142-0721-881
JPM1	0.1"	Connectors	Samtec	HTSW-150-07-G-S
Standoffs	Round Threaded	Hardware	Keystone Electronics	2029
Screws	Philips	Hardware	Building Fasteners	PMSSS 440 0025 PH
JP1–JP18				DNI
R12, R13, R18, R19				DNI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of -0.2 V to Vcc +0.2 V and the output voltage range of -0.2 V to Vcc +0.2 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 120°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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