

100V N-Channel Power MOSFET

DESCRIPTION

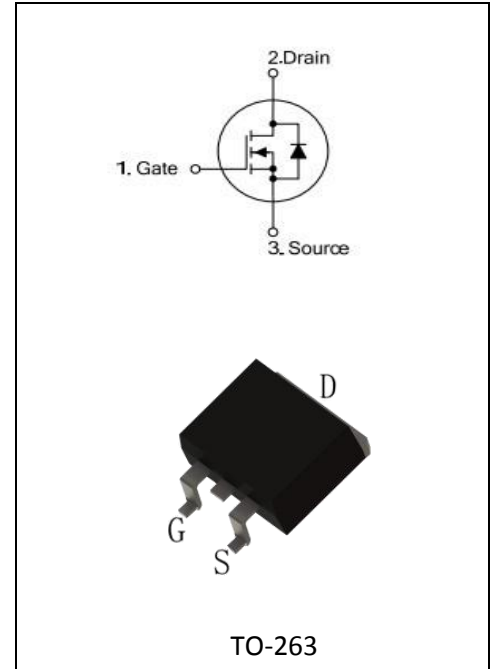
The IRF540NS uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

Application

- ① Power switching application
- ② Hard switched and High frequency circuits
- ③ Uninterruptible power supply

KEY CHARACTERISTICS

- ① $V_{DS} = 100V, I_D = 35A$
 $R_{DS(ON)} < 30m\Omega @ V_{GS} = 10V$
- ② High density cell design for lower R_{dson}
- ③ Fully characterized avalanche voltage and current
- ④ Good stability and uniformity with high EAS
- ⑤ Excellent package for good heat dissipation



Package Marking And Ordering Information:

Ordering Codes	Package	Product Code	Packing
IRF540NS	TO-263	IRF540NS	Reel

Absolute Maximum Ratings (TA=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	35	A
Drain Current-Pulsed ^(Note 1)	I_{DM}	100	A
Maximum Power Dissipation ($T_c = 25^\circ C$)	P_D	70	W
Single pulse avalanche energy ^(Note 2)	EAS	96	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.5	$^\circ C/W$
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Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	B _{VDS}	V _{GS} =0V, I _D =250μA	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	2.3	3	V
Drain-Source On-State Resistance ^(Note 3)	R _{DS(on)}	V _{GS} =10V, I _D =12A	-	25	30	mΩ
Forward Trans conductance	g _{FS}	V _{DS} =5V, I _D =15A	-	11	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	-	2550	-	pF
Output Capacitance	C _{oss}		-	225	-	pF
Reverse Transfer Capacitance	C _{rss}		-	205	-	pF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =20A, V _{GS} =10V, R _{GEN} =10Ω	-	29	-	nS
Turn-on Rise Time	t _r		-	13	-	nS
Turn-Off Delay Time	t _{d(off)}		-	58.2	-	nS
Turn-Off Fall Time	t _f		-	13.4	-	nS
Total Gate Charge	Q _g	V _{DS} =80V, I _D =20A V _{GS} =10V	-	55	-	nC
Gate-Source Charge	Q _{gs}		-	15	-	nC
Gate-Drain Charge	Q _{gd}		-	20	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Reverse Recovery Time	T _{rr}	T _j =25°C, I _F =10A, di/dt=100A/μs ^(note3)	-	58	-	nS
Reverse Recovery Charge	Q _{rr}		-	110	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. EAS condition :T_j=25°C, V_{DD}=50V, V_{GS}=10V, L=0.5mH, R_g=25Ω
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production.

Characteristics Curves

Figure 1 Output Characteristics

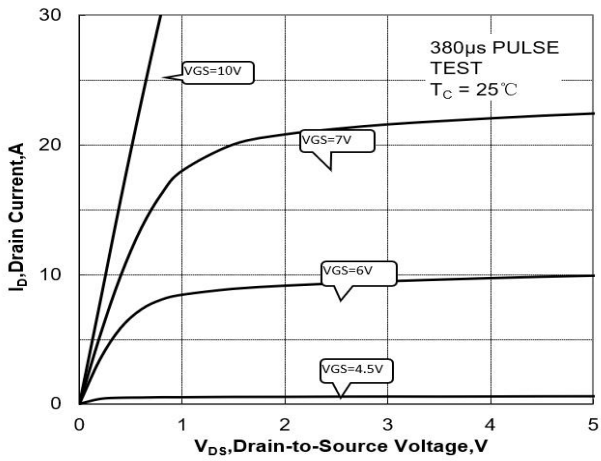


Figure 2 Transfer Characteristics

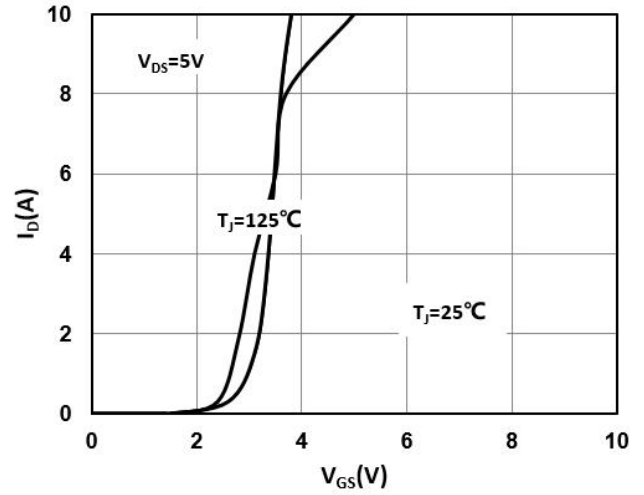


Figure 3 On-Resistance vs. ID and VGS

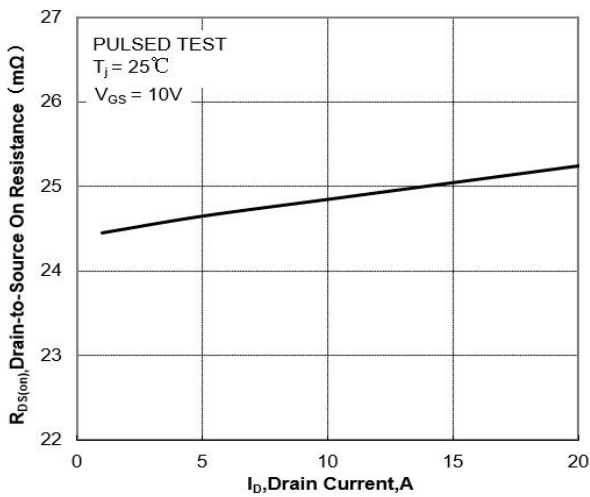


Figure 4 On-Resistance vs. Junction Temperature

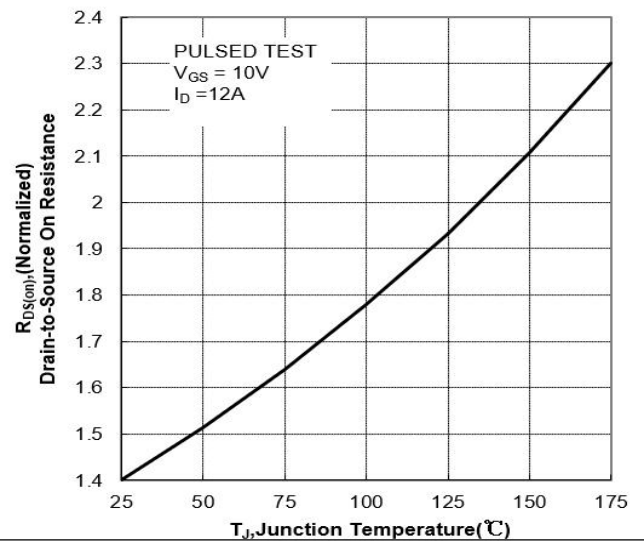


Figure 5 On-Resistance vs. VGS

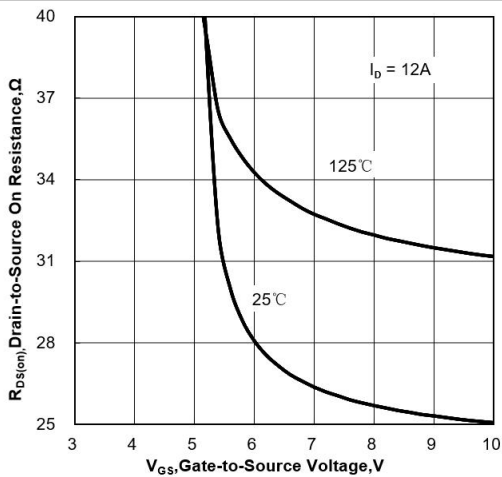


Figure 6 Body Diode Forward Voltage

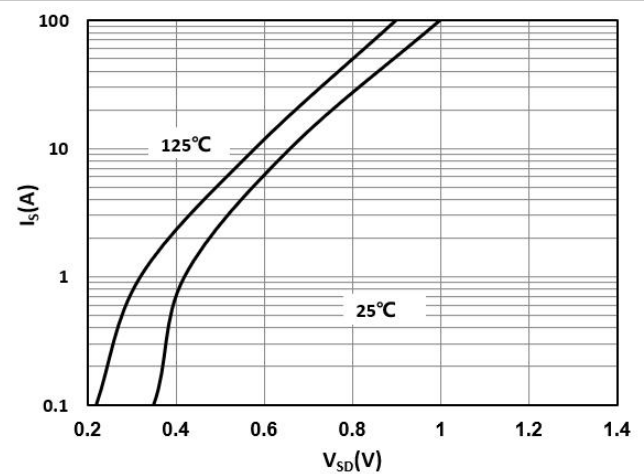


Figure 7 Gate-Charge Characteristics

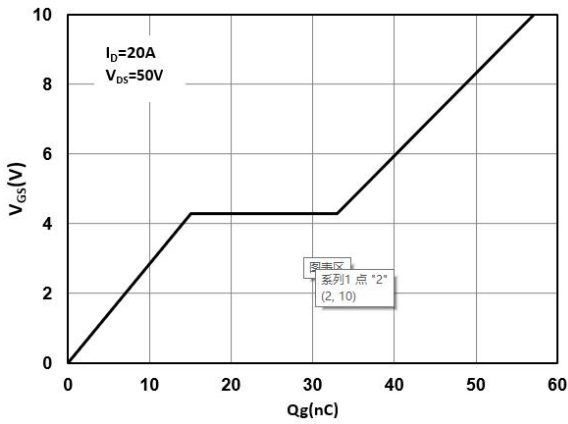


Figure 8 Capacitance Characteristics

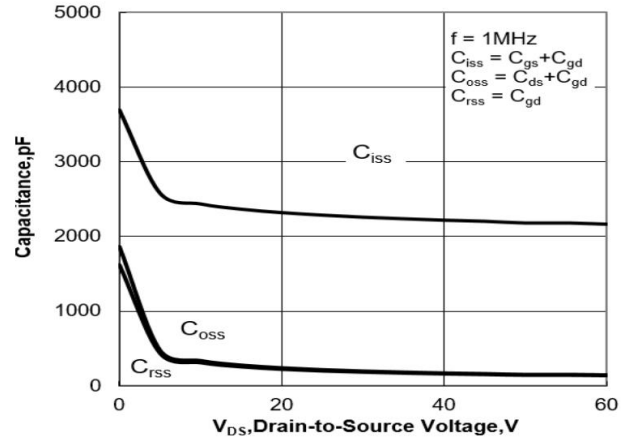


Figure 9 Maximum Forward Biased Safe Operation Area

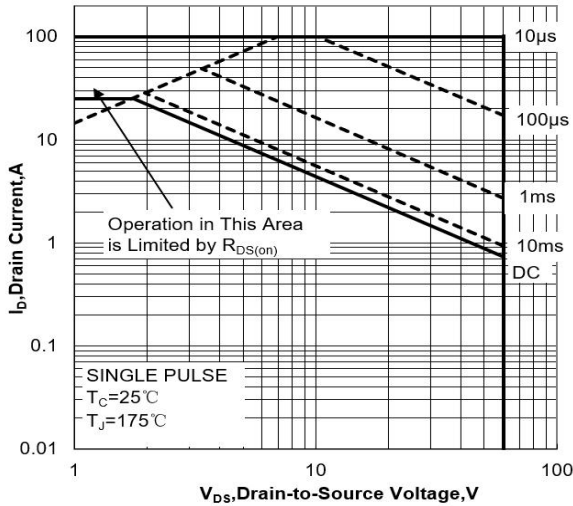


Figure 10 Single Pulse Power Rating Junction-to-Ambient

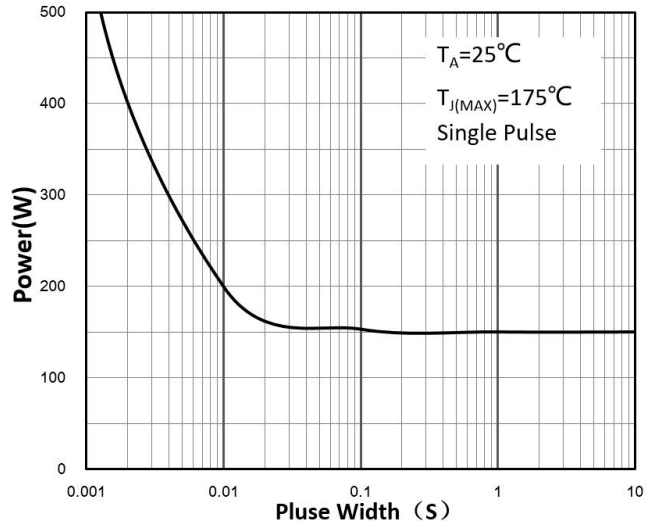
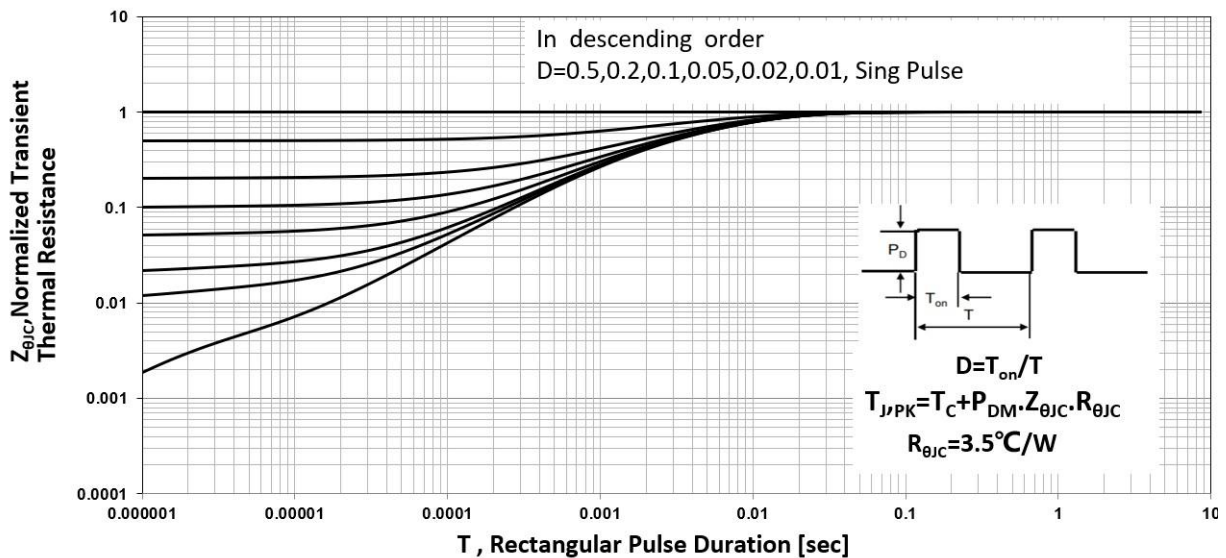
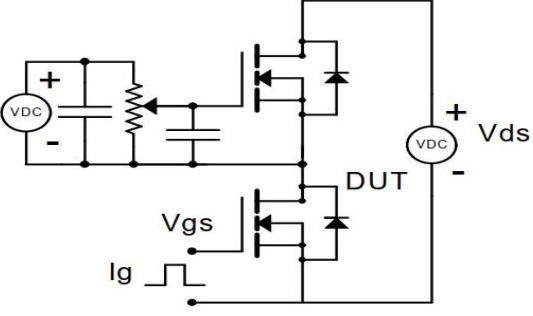
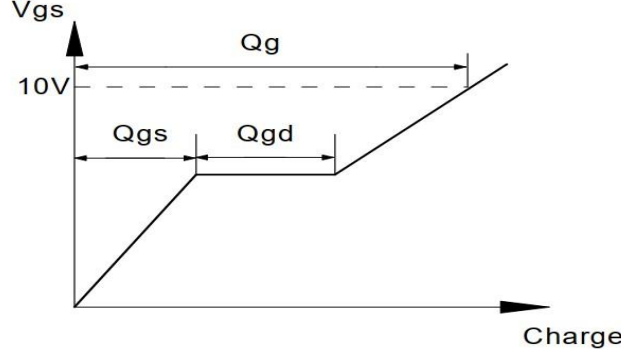
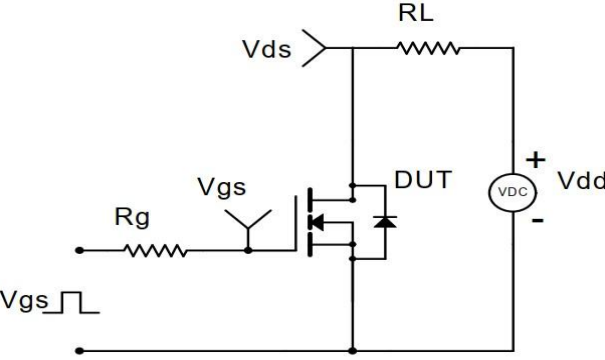
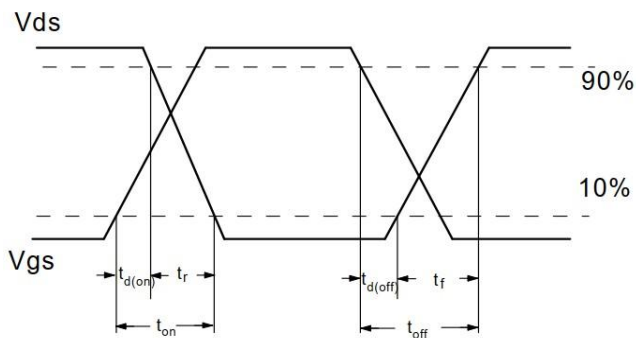
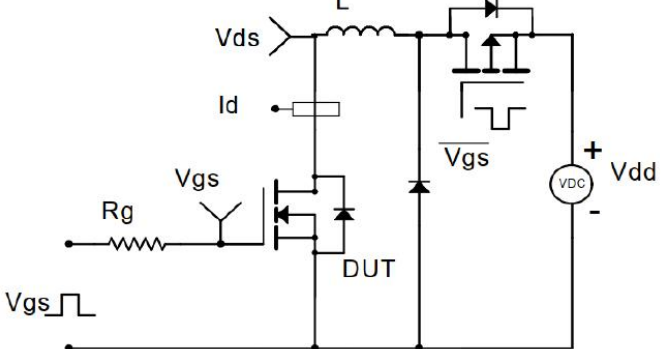
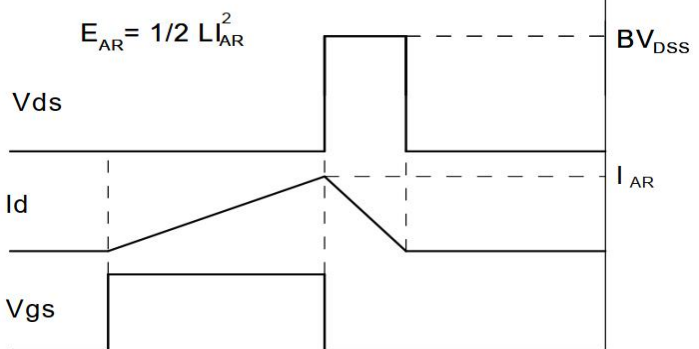
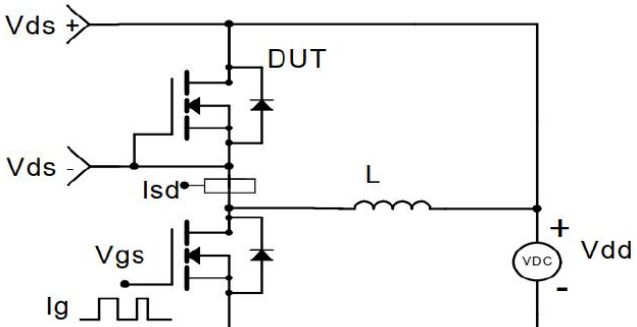
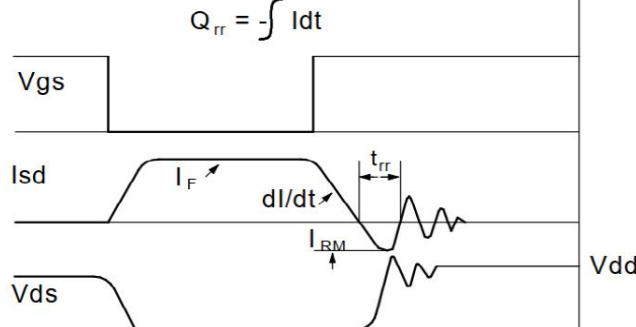


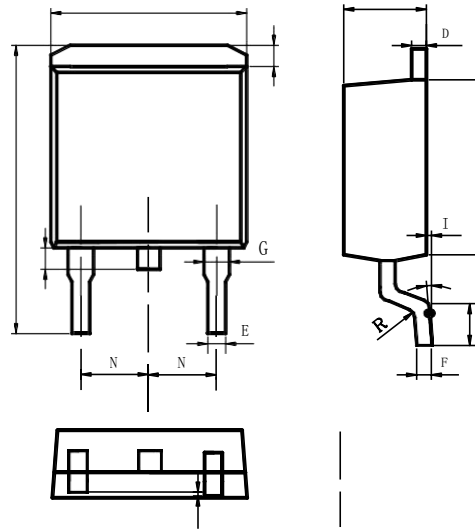
Figure 11 Normalized Maximum Transient Thermal Impedance



Test Circuit and Waveform

Gate Charge Test Circuit	Gate Charge Test Waveform
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a gate driver circuit. The gate driver consists of a VDC source, a resistor, and a capacitor. The gate is driven by a pulse source Ig. The drain is connected to a load resistor and a VDC source. The MOSFET is shown in a common-emitter configuration.</p>	 <p>The graph shows the gate voltage Vgs over time. The gate voltage rises from 0V to 10V, stays constant for a duration Qgs, then falls to 0V for a duration Qgd, and finally rises again. The total gate charge is labeled Qg. The x-axis is labeled 'Charge'.</p>
Resistive Switching Test Circuit	Resistive Switching Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a gate driver circuit. The gate driver consists of a VDC source, a resistor Rg, and a switch. The drain is connected to a load resistor RL and a VDC source Vdd. The MOSFET is shown in a common-emitter configuration.</p>	 <p>The graph shows the drain voltage Vds and gate voltage Vgs over time. Vds is high when the MOSFET is off and low when it is on. Vgs is high when the MOSFET is on and low when it is off. The switching times are labeled: t_{d(on)}, t_r, t_{on}, t_{d(off)}, t_f, and t_{off}. The Vds transitions are marked at 90% and 10% levels.</p>
Unclamped Inductive Switching (UIS) Test Circuit	Unclamped Inductive Switching (UIS) Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a gate driver circuit. The gate driver consists of a VDC source, a resistor Rg, and a switch. The drain is connected to an inductor L and a VDC source Vdd. The MOSFET is shown in a common-emitter configuration.</p>	 <p>The graph shows the drain voltage Vds, drain current Id, and gate voltage Vgs over time. Vds is high when the MOSFET is off and low when it is on. Id is high when the MOSFET is on and low when it is off. Vgs is high when the MOSFET is on and low when it is off. The energy stored in the inductor is given by the equation $E_{AR} = 1/2 L I_{AR}^2$. The Vds peak is labeled BV_{DSS} and the Id peak is labeled I_{AR}.</p>
Diode Recovery Test Circuit	Diode Recovery Test Waveforms
 <p>The diagram shows a MOSFET (DUT) with its gate connected to a gate driver circuit. The gate driver consists of a VDC source, a resistor Rg, and a switch. The drain is connected to an inductor L and a VDC source Vdd. The MOSFET is shown in a common-emitter configuration.</p>	 <p>The graph shows the drain current Isd, gate voltage Vgs, and drain voltage Vds over time. Isd is high when the MOSFET is on and low when it is off. Vgs is high when the MOSFET is on and low when it is off. Vds is high when the MOSFET is off and low when it is on. The reverse recovery time is labeled t_{rr}. The peak reverse current is labeled I_{RM}. The equation $Q_{rr} = \int Idt$ is shown.</p>

Package Description



Items	Values(mm)	
	MIN	MAX
A	9.80	10.40
B	8.90	9.50
B1	0	0.10
C	4.40	4.80
D	1.16	1.37
E	0.70	0.95
F	0.30	0.60
G	1.07	1.47
H	1.30	1.80
K	0.95	1.37
L1	14.50	16.50
L2	1.60	2.30
I	0	0.2
Q	0°	8°
R	0.4	
N	2.39	2.69

TO-263 package



NOTE:

1. Exceeding the maximum ratings of the device in performance may cause damage to the device, even the permanent failure, which may affect the dependability of the machine. Please do not exceed the absolute maximum ratings of the device when circuit designing.
2. When installing the heat sink, please pay attention to the torsional moment and the smoothness of the heat sink.
3. MOSFETs is the device which is sensitive to the static electricity, it is necessary to protect the device from being damaged by the static electricity when using it.
4. Shenzhen Minos reserves the right to make changes in this specification sheet and is subject to change without prior notice.

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