

General Description

The SN74HC/HCT161 is a synchronous presettable binary counter with an internal look-head carry. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock (CP). The outputs (Q0 to Q3) of the counters may be preset HIGH or LOW. A LOW at the parallel enable input (\overline{PE}) disables the counting action and causes the data at the data inputs (D0 to D3) to be loaded into the counter on the positive-going edge of the clock. Preset takes place regardless of the levels at count enable inputs (CEP and CET). A LOW at the master reset input (\overline{MR}) sets Q0 to Q3 LOW regardless of the levels at input pins CP, \overline{PE} , CET and CEP (thus providing an asynchronous clear function). The look-ahead carry simplifies serial cascading of the counters. Both CEP and CET must be HIGH to count. The CET input is fed forward to enable the terminal count output (TC). The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to a HIGH output of Q0. This pulse can be used to enable the next cascaded stage. The maximum clock frequency for the cascaded counters is determined by the CP to TC propagation delay and CEP to CP set-up time, according to the following formula: $f_{max} = 1 / (t_{p(max)}(CP \text{ to } TC) + t_{SU}(CEP \text{ to } CP))$

Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features

- Input levels:
For SN74HC161: CMOS level
For SN74HCT161: TTL level
- Synchronous counting and loading
- 2 count enable inputs for n-bit cascading
- Asynchronous reset
- Positive-edge triggered clock
- Specified from -40°C to +105°C
- Packaging information: DIP16/SOP16/TSSOP16

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing QTY
SN74HC161N	DIP-16	74HC161N	Tube	1000/Box
SN74HC161DTR	SOP-16	74HC161	Tape	2500/Reel
SN74HCT161DTR	SOP-16	74HCT161	Tape	2500/Reel
SN74HCT161TDTR	TSSOP-16	74HCT161	Tape	3000/Reel

Block Diagram And Pin Description

Block Diagram

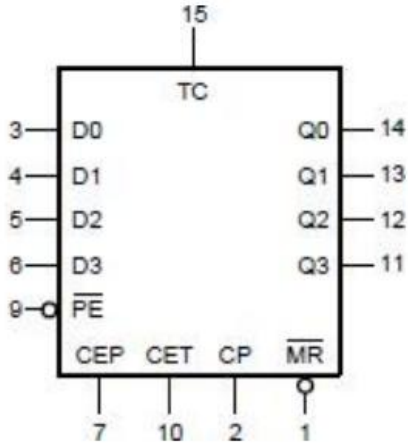


Figure 1. Logic symbol

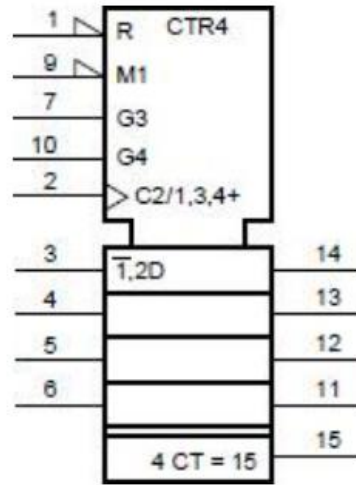


Figure 2. IEC Logic symbol

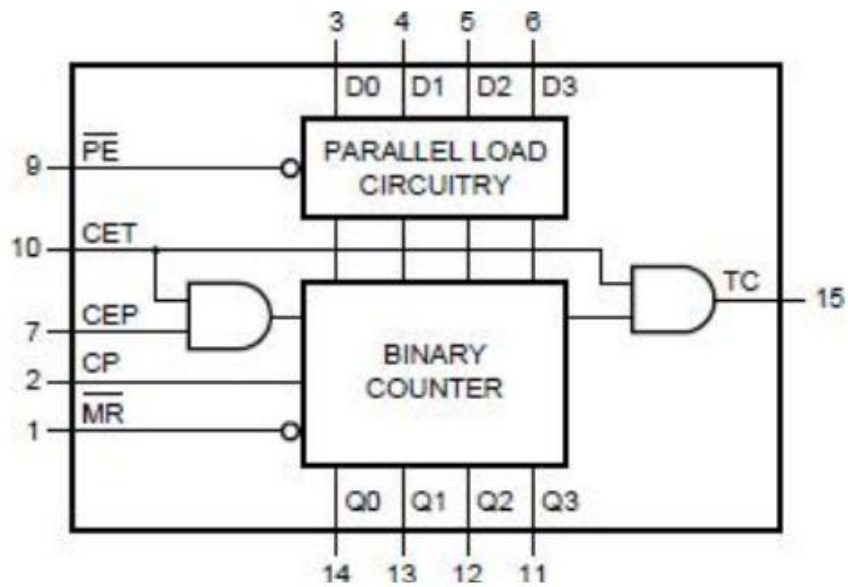


Figure 3. Functional diagram

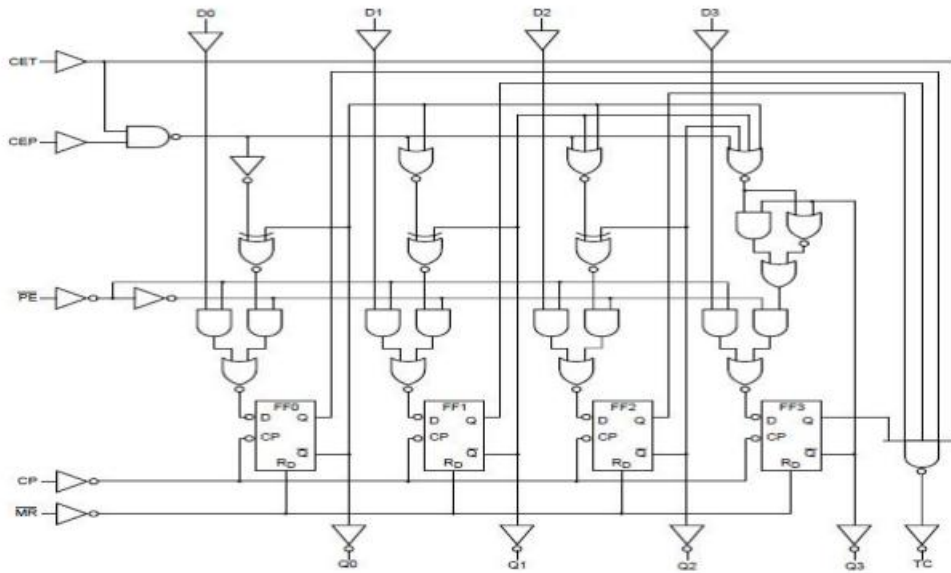


Figure 4. Logic diagram

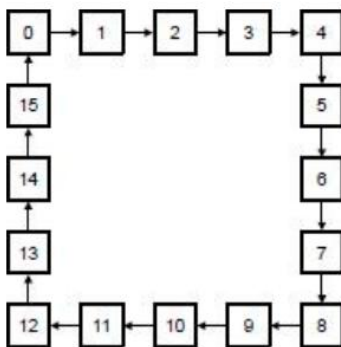


Figure 5. State diagram

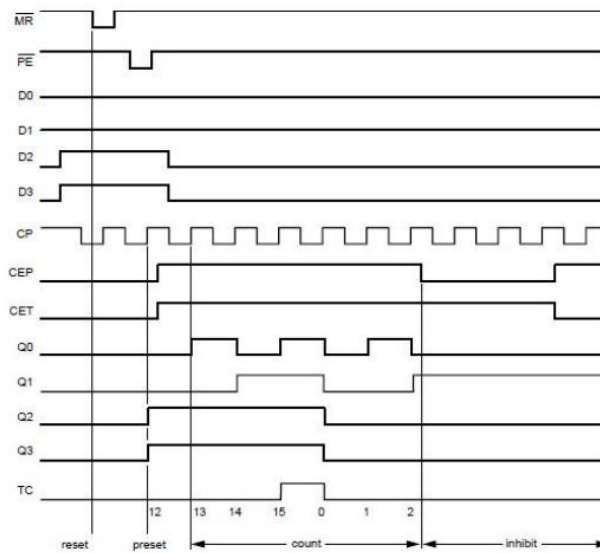
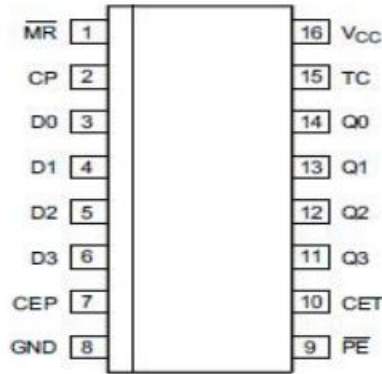


Figure 6. Typical timing sequence

Pin Configurations



Pin Description

Pin No.	Pin Name	Description
1	\overline{MR}	asynchronous master reset(active LOW)
2	CP	clock input(LOW-to-HIGH,edge triggered)
3	D0	data input
4	D1	data input
5	D2	data input
6	D3	data input
7	CEP	count enable input
8	GND	ground(0V)
9	\overline{PE}	parallel enable input(active LOW)
10	CET	count enable carry input
11	Q3	flip-flop output
12	Q2	flip-flop output
13	Q1	flip-flop output
14	Q0	flip-flop output
15	TC	terminal count output
16	V _{CC}	supply voltage

Function Table

Operating mode	Input						Output	
	\overline{MR}	CP	CEP	CET	\overline{PE}	Dn	Qn	TC
reset(clear)	L	X	X	X	X	X	L	L
parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	[2]
count	H	↑	h	h	h	X	count	[2]
hold(do nothing)	H	X	l	X	h	X	q _n	[2]
	H	X	X	l	h	X	q _n	L

Note:

- [1] H=HIGH voltage level; L=LOW voltage level; X=don't care; ↑=LOW-to-HIGH clock transition;
 l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
 h=HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
 q=lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.
- [2] The TC output is HIGH when CET is HIGH and the counter is at terminal count (HLLH).

Electrical Parameter

Absolute Maximum Ratings (Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V _{CC}	-	-0.5	+7.0	V
input clamping current	I _{IK}	V _I < -0.5V or V _I > V _{CC} +0.5V	-	±20	mA
output clamping current	I _{OK}	V _O < -0.5V or V _O > V _{CC} +0.5V	-	±20	mA
output current	I _O	-0.5V < V _O < V _{CC} +0.5V	-	±25	mA
supply current	I _{CC}	-	-	+50	mA
ground current	I _{GND}	-	-50	-	mA
storage temperature	T _{stg}	-	-65	+150	°C
total power dissipation	P _{tot}	-	-	500	mW
soldering temperature	T _L	10s	DIP	245	°C
			SOP	250	

Note:

- [1] For DIP16 packages: above 70°C the value of P_{tot} derates linearly with 12mW/K.
 [2] For SOP16 packages: above 70°C the value of P_{tot} derates linearly with 8mW/K.
 [3] For (T)SSOP16 packages: above 60°C the value of P_{tot} derates linearly with 5.5mW/K.

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC161						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=2.0V$	-	-	625	ns/V
		$V_{CC}=4.5V$	-	1.67	139	ns/V
		$V_{CC}=6.0V$	-	-	83	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	°C
SN74HCT161						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC}=4.5V$	-	1.67	139	ns/V
ambient temperature	T_{amb}	-	-40	-	+105	°C

Electrical Characteristics

DC Characteristics 1 ($T_{amb}=25^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC161							
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$	1.5	1.2	-	V	
		$V_{CC}=4.5V$	3.15	2.4	-	V	
		$V_{CC}=6.0V$	4.2	3.2	-	V	
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$	-	0.8	0.5	V	
		$V_{CC}=4.5V$	-	2.1	1.35	V	
		$V_{CC}=6.0V$	-	2.8	1.8	V	
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	$I_O=-20\mu A; V_{CC}=2.0V$	1.9	2.0	-	V
			$I_O=-20\mu A; V_{CC}=4.5V$	4.4	4.5	-	V
			$I_O=-20\mu A; V_{CC}=6.0V$	5.9	6.0	-	V
			$I_O=-4.0mA; V_{CC}=4.5V$	3.98	4.32	-	V
			$I_O=-5.2mA; V_{CC}=6.0V$	5.48	5.81	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	$I_O=20\mu A; V_{CC}=2.0V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=4.5V$	-	0	0.1	V
			$I_O=20\mu A; V_{CC}=6.0V$	-	0	0.1	V
			$I_O=4.0mA; V_{CC}=4.5V$	-	0.15	0.26	V
			$I_O=5.2mA; V_{CC}=6.0V$	-	0.16	0.26	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$	-	-	± 0.1	μA	
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_O=0A; V_{CC}=6.0V$	-	-	8.0	μA	

input apacitance	C_I	-		-	3.5	-	pF
SN74HCT161							
HIGH-level input voltage	V_{IH}	$V_{CC}=4.5V$ to $5.5V$		2.0	1.6	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=4.5V$ to $5.5V$		-	1.2	0.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL} $V_{CC}=4.5V$	$I_O=-20\mu A$	4.4	4.5	-	V
			$I_O=-4.0\mu A$	3.98	4.32	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL} $V_{CC}=4.5V$	$I_O=20\mu A$	-	0	0.1	V
			$I_O=4.0\mu A$	-	0.15	0.26	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=5.5V$		-	-	± 0.1	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_O=0A$; $V_{CC}=5.5V$		-	-	8.0	μA
Additional Supply currend	ΔI_{CC}	per input pin; $V_I=V_{CC}-2.1V$; other inputs at V_{CC} or GND; $I_O=0V$; $V_{CC}=4.5V$ to $5.5V$	pin $M\bar{R}$	-	95	342	μA
			pin CP	-	110	396	μA
			pin CEP and Dn	-	25	90	μA
			pin CET	-	75	270	μA
			pin $P\bar{E}$	-	30	108	μA
input apacitance	C_I	-		-	3.5	-	pF

DC Characteristics 2

($T_{amb}=-40^{\circ}C$ to $+85^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC161							
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$	1.5	-	-	V	
		$V_{CC}=4.5V$	3.15	-	-	V	
		$V_{CC}=6.0V$	4.2	-	-	V	
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$	-	-	0.5	V	
		$V_{CC}=4.5V$	-	-	1.35	V	
		$V_{CC}=6.0V$	-	-	1.8	V	
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL}	$I_O=-20\mu A$; $V_{CC}=2.0V$	1.9	-	-	V
			$I_O=-20\mu A$; $V_{CC}=4.5V$	4.4	-	-	V
			$I_O=-20\mu A$; $V_{CC}=6.0V$	5.9	-	-	V
			$I_O=-4.0mA$; $V_{CC}=4.5V$	3.84	-	-	V
			$I_O=-5.2mA$; $V_{CC}=6.0V$	5.34	-	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL}	$I_O=20\mu A$; $V_{CC}=2.0V$	-	-	0.1	V
			$I_O=20\mu A$; $V_{CC}=4.5V$	-	-	0.1	V
			$I_O=20\mu A$; $V_{CC}=6.0V$	-	-	0.1	V
			$I_O=4.0mA$; $V_{CC}=4.5V$	-	-	0.33	V
			$I_O=5.2mA$; $V_{CC}=6.0V$	-	-	0.33	V

input leakage current	I_I	$V_i = V_{CC}$ or GND; $V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_i=V_{CC}$ or GND; $I_o=0A$; $V_{CC}=6.0V$		-	-	80	μA
SN74HCT161							
HIGH-level input voltage	V_{IH}	$V_{CC}=4.5V$ to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=4.5V$ to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	$V_i=V_{IH}$ or V_{IL} $V_{CC}=4.5V$	$I_o=-20\mu A$	4.4	-	-	V
			$I_o=-4.0mA$	3.84	-	-	V
LOW-level output voltage	V_{OL}	$V_i=V_{IH}$ or V_{IL} $V_{CC}=4.5V$	$I_o=20\mu A$	-	-	0.1	V
			$I_o=4.0mA$	-	-	0.33	V
input leakage current	I_I	$V_i = V_{CC}$ or GND; $V_{CC}=5.5V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_i=V_{CC}$ or GND; $I_o=0A$; $V_{CC}=5.5V$		-	-	80	μA
additional supply current	ΔI_{CC}	per input pin; $V_i=V_{CC}-2.1V$; other inputs at V_{CC} or GND; $I_o=0V$; $V_{CC}=4.5V$ to 5.5V	pin $M\bar{R}$	-	-	427.5	μA
			pin CP	-	-	495	μA
			pin CEP and Dn	-	-	112.5	μA
			pin CET	-	-	337.5	μA
			pin $P\bar{E}$	-	-	135	μA

DC Characteristics 3

($T_{amb}=-40^{\circ}C$ to $+105^{\circ}C$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC161							
HIGH-level input voltage	V_{IH}	$V_{CC}=2.0V$	1.5	-	-	V	
		$V_{CC}=4.5V$	3.15	-	-	V	
		$V_{CC}=6.0V$	4.2	-	-	V	
LOW-level input voltage	V_{IL}	$V_{CC}=2.0V$	-	-	0.5	V	
		$V_{CC}=4.5V$	-	-	1.35	V	
		$V_{CC}=6.0V$	-	-	1.8	V	
HIGH-level output voltage	V_{OH}	$V_i=V_{IH}$ or V_{IL}	$I_o=-20\mu A$; $V_{CC}=2.0V$	1.9	-	-	V
			$I_o=-20\mu A$; $V_{CC}=4.5V$	4.4	-	-	V
			$I_o=-20\mu A$; $V_{CC}=6.0V$	5.9	-	-	V
			$I_o=-4.0mA$; $V_{CC}=4.5V$	3.7	-	-	V
			$I_o=-5.2mA$; $V_{CC}=6.0V$	5.2	-	-	V
LOW-level output voltage	V_{OL}	$V_i=V_{IH}$ or V_{IL}	$I_o=20\mu A$; $V_{CC}=2.0V$	-	-	0.1	V
			$I_o=20\mu A$; $V_{CC}=4.5V$	-	-	0.1	V
			$I_o=20\mu A$; $V_{CC}=6.0V$	-	-	0.1	V
			$I_o=4.0mA$; $V_{CC}=4.5V$	-	-	0.4	V



			$I_o=5.2mA; V_{CC}=6.0V$	-	-	0.4	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=6.0V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_o=0A; V_{CC}=6.0V$		-	-	160	μA
SN74HCT161							
HIGH-level input voltage	V_{IH}	$V_{CC}=4.5V$ to 5.5V		2.0	-	-	V
LOW-level input voltage	V_{IL}	$V_{CC}=4.5V$ to 5.5V		-	-	0.8	V
HIGH-level output voltage	V_{OH}	$V_I=V_{IH}$ or V_{IL} $V_{CC}=4.5V$	$I_o=-20\mu A$	4.4	-	-	V
			$I_o=4.0mA$	3.7	-	-	V
LOW-level output voltage	V_{OL}	$V_I=V_{IH}$ or V_{IL} $V_{CC}=4.5V$	$I_o=20\mu A$	-	-	0.1	V
			$I_o=4.0mA$	-	-	0.4	V
input leakage current	I_I	$V_I=V_{CC}$ or GND; $V_{CC}=5.5V$		-	-	± 1.0	μA
supply current	I_{CC}	$V_I=V_{CC}$ or GND; $I_o=0A; V_{CC}=5.5V$		-	-	160	μA
additional supply current	ΔI_{CC}	$V_I=V_{CC}-2.1V$; other inputs at V_{CC} or GND; $I_o=0V$; $V_{CC}=4.5V$ to 5.5V	pin $M\bar{R}$	-	-	465.5	μA
			pin CP	-	-	539	μA
			pin CEP and Dn	-	-	122.5	μA
			pin CET	-	-	367.5	μA
			pin $P\bar{E}$	-	-	147	μA

AC Characteristics 1 (Tamb=25°C, GND=0V; $t_r=t_f=6ns$; $C_L=50pF$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC161							
Propagation delay	t_{pd}	CP to Qn; see Figure8	$V_{CC}=2.0V$	-	61	190	ns
			$V_{CC}=4.5V$	-	22	38	ns
			$V_{CC}=5.0V; C_L=15pF$	-	19	-	ns
			$V_{CC}=6.0V$	-	18	32	ns
		CP to TC; see Figure8	$V_{CC}=2.0V$	-	69	215	ns
			$V_{CC}=4.5V$	-	25	43	ns
			$V_{CC}=5.0V; C_L=15pF$	-	21	-	ns
			$V_{CC}=6.0V$	-	20	37	ns
		CET to TC; see Figure9	$V_{CC}=2.0V$	-	33	150	ns
			$V_{CC}=4.5V$	-	12	30	ns
			$V_{CC}=5.0V; C_L=15pF$	-	10	-	ns
			$V_{CC}=6.0V$	-	10	26	ns
High to LOW Propagation delay	t_{PHL}	M \bar{R} to Qn; see Figure10	$V_{CC}=2.0V$	-	63	210	ns
			$V_{CC}=4.5V$	-	23	42	ns
			$V_{CC}=5.0V; C_L=15pF$	-	20	-	ns
			$V_{CC}=6.0V$	-	18	36	ns

		M \bar{R} to TC; see Figure10	V _{CC} =2.0V	-	63	220	ns
			V _{CC} =4.5V	-	23	44	ns
			V _{CC} =5.0V;CL=15pF	-	20	-	ns
			V _{CC} =6.0V	-	18	37	ns
transition time	t _t	see Figure8 and see Figure9	V _{CC} =2.0V	-	19	75	ns
			V _{CC} =4.5V	-	7	15	ns
			V _{CC} =6.0V	-	6	13	ns
pulse width	t _w	CP HIGH or LOW;see Figure8	V _{CC} =2.0V	80	22	-	ns
			V _{CC} =4.5V	16	8	-	ns
			V _{CC} =6.0V	14	6	-	ns
		M \bar{R} LOW; see Figure10	V _{CC} =2.0V	80	19	-	ns
			V _{CC} =4.5V	16	7	-	ns
			V _{CC} =6.0V	14	6	-	ns
Recovery time	t _{rec}	M \bar{R} to CP; see Figure10	V _{CC} =2.0V	100	19	-	ns
			V _{CC} =4.5V	20	7	-	ns
			V _{CC} =6.0V	17	6	-	ns
Set-up time	t _{su}	Dn to CP; see Figure11	V _{CC} =2.0V	80	25	-	ns
			V _{CC} =4.5V	16	9	-	ns
			V _{CC} =6.0V	14	7	-	ns
		P \bar{E} to CP; see Figure11	V _{CC} =2.0V	100	30	-	ns
			V _{CC} =4.5V	20	11	-	ns
			V _{CC} =6.0V	17	9	-	ns
		CEP,CET to CP; see Figure12	V _{CC} =2.0V	170	47	-	ns
			V _{CC} =4.5V	34	17	-	ns
			V _{CC} =6.0V	29	14	-	ns
Hold time	t _h	Dn, P \bar{E} ,CEP,CETto CP; see Figure11,12	V _{CC} =2.0V	0	-14	-	ns
			V _{CC} =4.5V	0	-5	-	ns
			V _{CC} =6.0V	0	-4	-	ns
Maximum frequency	f _{MAX}	CP;see Figure8	V _{CC} =2.0V	4.6	13	-	MHz
			V _{CC} =4.5V	23	40	-	MHz
			V _{CC} =5.0V;CL=15pF	-	44	-	MHz
			V _{CC} =6.0V	27	48	-	MHz
power dissipation capacitance	C _{PD}	f _i =1MHz; V _i =GND to V _{CC}	-	33	-	pF	
SN74HCT161							
Propagation delay	t _{pd}	CP to Qn; see Figure8 ^[1]	V _{CC} =4.5V	-	25	43	ns
			V _{CC} =5.0V;C _L =15pF	-	20	-	ns
		CP to TC; see Figure8	V _{CC} =4.5V	-	28	48	ns
			V _{CC} =5.0V;C _L =15pF	-	24	-	ns
		CET to TC;	V _{CC} =4.5V	-	17	35	ns

		see Figure9	$V_{CC}=5.0V; C_L=15pF$	-	14	-	ns
HIGH to LOW propagation delay	t_{PHL}	\overline{MR} to Qn; see Figure10	$V_{CC}=4.5V$	-	29	46	ns
			$V_{CC}=5.0V; C_L=15pF$	-	25	-	ns
		\overline{MR} to TC; see Figure10	$V_{CC}=4.5V$	-	30	51	ns
			$V_{CC}=5.0V; C_L=15pF$	-	26	-	ns
transition time	t_t	$V_{CC}=4.5V$; see Figure8,9		-	7	15	ns
pulse width	t_w	CP HIGH or LOW; $V_{CC}=4.5V$; see Figure8		16	7	-	ns
		\overline{MR} LOW; $V_{CC}=4.5V$; see Figure10		20	10	-	ns
Recovery time	t_{rec}	\overline{MR} CP; $V_{CC}=4.5V$; see Figure10		20	6	-	ns
Set-up time	t_{su}	Dn to CP; $V_{CC}=4.5V$; see Figure11		18	8	-	ns
		\overline{PE} to CP; $V_{CC}=4.5V$; see Figure11		30	17	-	ns
		CEP, CET to CP; $V_{CC}=4.5V$; see Figure12		40	17	-	ns
Hold time	t_h	Dn, \overline{PE} , CEP, CET to CP; $V_{CC}=4.5V$; see Figure11		0	-7	-	ns
Maximum frequency	f_{MAX}	CP; see Figure8	$V_{CC}=4.5V$	23	41	-	MHz
			$V_{CC}=5.0V; C_L=15pF$	-	45	-	MHz
power dissipation capacitance	C_{PD}	$f_i=1MHz$; $V_i=GND$ to $V_{CC}-1.5V$		-	35	-	pF

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in uW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i =input frequency in MHz;

f_o =output frequency in MHz;

C_L =output load capacitance in pF;

V_{CC} =supply voltage in V;

N=number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f)$ =sum of outputs.

AC Characteristics 2 ($T_{amb}=-40^\circ C$ to $+85^\circ C$, $GND=0V$; $t_r=t_f=6ns$; $C_L=50pF$, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC161							
Propagation delay	t_{pd}	CP to Qn; see Figure8	$V_{CC}=2.0V$	-	-	240	ns
			$V_{CC}=4.5V$	-	-	48	ns
			$V_{CC}=6.0V$	-	-	41	ns
		CP to TC; see Figure8	$V_{CC}=2.0V$	-	-	270	ns
			$V_{CC}=4.5V$	-	-	54	ns
			$V_{CC}=6.0V$	-	-	46	ns



		CET to TC; see Figure9	V _{CC} =2.0V	-	-	190	ns
			V _{CC} =4.5V	-	-	38	ns
			V _{CC} =6.0V	-	-	33	ns
High to LOW Propagation delay	t _{PHL}	M \bar{R} to Qn; see Figure10	V _{CC} =2.0V	-	-	265	ns
			V _{CC} =4.5V	-	-	53	ns
			V _{CC} =6.0V	-	-	45	ns
		M \bar{R} to TC; see Figure10	V _{CC} =2.0V	-	-	275	ns
			V _{CC} =4.5V	-	-	55	ns
			V _{CC} =6.0V	-	-	47	ns
transition time	t _t	see Figure8 and see Figure9	V _{CC} =2.0V	-	-	95	ns
			V _{CC} =4.5V	-	-	19	ns
			V _{CC} =6.0V	-	-	16	ns
pulse width	t _w	CP HIGH or LOW;see Figure8	V _{CC} =2.0V	100	-	-	ns
			V _{CC} =4.5V	20	-	-	ns
			V _{CC} =6.0V	17	-	-	ns
		M \bar{R} LOW; see Figure10	V _{CC} =2.0V	100	-	-	ns
			V _{CC} =4.5V	20	-	-	ns
			V _{CC} =6.0V	17	-	-	ns
Recovery time	t _{rec}	M \bar{R} to CP; see Figure10	V _{CC} =2.0V	125	-	-	ns
			V _{CC} =4.5V	25	-	-	ns
			V _{CC} =6.0V	21	-	-	ns
Set-up time	t _{su}	Dn to CP; see Figure11	V _{CC} =2.0V	100	-	-	ns
			V _{CC} =4.5V	20	-	-	ns
			V _{CC} =6.0V	17	-	-	ns
		P \bar{E} to CP; see Figure11	V _{CC} =2.0V	125	-	-	ns
			V _{CC} =4.5V	25	-	-	ns
			V _{CC} =6.0V	21	-	-	ns
		CEP,CET to CP; see Figure12	V _{CC} =2.0V	215	-	-	ns
			V _{CC} =4.5V	43	-	-	ns
			V _{CC} =6.0V	37	-	-	ns
Hold time	t _h	Dn, P \bar{E} CEP,CET, to CP; see Figure11,12	V _{CC} =2.0V	0	-	-	ns
			V _{CC} =4.5V	0	-	-	ns
			V _{CC} =6.0V	0	-	-	ns
Maximum frequency	f _{MAX}	CP;see Figure8	V _{CC} =2.0V	3.6	-	-	MHz
			V _{CC} =4.5V	18	-	-	MHz
			V _{CC} =6.0V	21	-	-	MHz
SN74HCT161							
Propagation delay	t _{pd}	CP to Qn; see Figure8	V _{CC} =4.5V	-	-	54	ns
		CP to TC; see Figure8	V _{CC} =4.5V	-	-	60	ns

		CET to TC; see Figure9	V _{CC} =4.5V	-	-	44	ns
High to LOW propagation delay	t _{PHL}	M \bar{R} to Qn; see Figure10	V _{CC} =4.5V	-	-	58	ns
		M \bar{R} to TC; see Figure10	V _{CC} =4.5V	-	-	63	ns
transition time	t _t	V _{CC} =4.5V;see Figure8,9 ^[2]		-	-	19	ns
pulse width	t _w	CP HIGH or LOW;V _{CC} =4.5V;see Figure8		20	-	-	ns
		M \bar{R} LOW;V _{CC} =4.5V;see Figure10		25	-	-	ns
Recovery time	t _{rec}	M \bar{R} to CP;V _{CC} =4.5V;see Figure10		25	-	-	ns
Set-up time	t _{su}	Dn to CP;V _{CC} =4.5V;see Figure11		23	-	-	ns
		P \bar{E} to CP;V _{CC} =4.5V;see Figure11		38	-	-	ns
		CEP,CET to CP;V _{CC} =4.5V;see Figure12		50	-	-	ns
Hold time	t _h	Dn, P \bar{E} , CEP, CET to CP; V _{CC} =4.5V;see Figure11		0	-	-	ns
Maximum frequency	f _{MAX}	CP;see Figure8	V _{CC} =4.5V	18	-	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

AC Characteristics 3 (T_{amb}=-40°C to +105°C, GND=0V; t_r=t_f=6ns; C_L=50pF, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
SN74HC161							
Propagation delay	t _{pd}	CP to Qn; see Figure8	V _{CC} =2.0V	-	-	248	ns
			V _{CC} =4.5V	-	-	57	ns
			V _{CC} =6.0V	-	-	48	ns
		CP to TC; see Figure8	V _{CC} =2.0V	-	-	325	ns
			V _{CC} =4.5V	-	-	65	ns
			V _{CC} =6.0V	-	-	55	ns
		CET to TC; see Figure9	V _{CC} =2.0V	-	-	225	ns
			V _{CC} =4.5V	-	-	45	ns
			V _{CC} =6.0V	-	-	38	ns
High to LOW Propagation delay	t _{PHL}	M \bar{R} to Qn; see Figure10	V _{CC} =2.0V	-	-	315	ns
			V _{CC} =4.5V	-	-	63	ns
			V _{CC} =6.0V	-	-	54	ns
		M \bar{R} to TC; see Figure10	V _{CC} =2.0V	-	-	330	ns
			V _{CC} =4.5V	-	-	66	ns

			$V_{CC}=6.0V$	-	-	56	ns
transition time	t_t	see Figure8 and see Figure9	$V_{CC}=2.0V$	-	-	110	ns
			$V_{CC}=4.5V$	-	-	22	ns
			$V_{CC}=6.0V$	-	-	19	ns
pulse width	t_w	CP HIGH or LOW; see Figure8	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	20	-	-	ns
		\overline{MR} LOW; see Figure10	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	20	-	-	ns
Recovery time	t_{rec}	\overline{MR} to CP; see Figure10	$V_{CC}=2.0V$	150	-	-	ns
			$V_{CC}=4.5V$	30	-	-	ns
			$V_{CC}=6.0V$	26	-	-	ns
Set-up time	t_{su}	Dn to CP; see Figure11	$V_{CC}=2.0V$	120	-	-	ns
			$V_{CC}=4.5V$	24	-	-	ns
			$V_{CC}=6.0V$	20	-	-	ns
		\overline{PE} to CP; see Figure11	$V_{CC}=2.0V$	150	-	-	ns
			$V_{CC}=4.5V$	30	-	-	ns
			$V_{CC}=6.0V$	26	-	-	ns
		CEP, CET to CP; see Figure12	$V_{CC}=2.0V$	255	-	-	ns
			$V_{CC}=4.5V$	51	-	-	ns
			$V_{CC}=6.0V$	43	-	-	ns
Hold time	t_h	Dn, \overline{PE} CEP, CET, to CP; see Figure11,12	$V_{CC}=2.0V$	0	-	-	ns
			$V_{CC}=4.5V$	0	-	-	ns
			$V_{CC}=6.0V$	0	-	-	ns
Maximum frequency	f_{MAX}	CP; see Figure8	$V_{CC}=2.0V$	3.0	-	-	MHz
			$V_{CC}=4.5V$	15	-	-	MHz
			$V_{CC}=6.0V$	18	-	-	MHz
SN74HCT161							
Propagation delay	t_{pd}	CP to Qn; see Figure8 ^[1]	$V_{CC}=4.5V$	-	-	65	ns
		CP to TC; see Figure8	$V_{CC}=4.5V$	-	-	72	ns
		CET to TC; see Figure9	$V_{CC}=4.5V$	-	-	53	ns
High to LOW propagation delay	t_{PHL}	\overline{MR} to Qn; see Figure10	$V_{CC}=4.5V$	-	-	69	ns
		\overline{MR} to TC; see Figure10	$V_{CC}=4.5V$	-	-	77	ns
transition time	t_t	$V_{CC}=4.5V$; see Figure8,9 ^[2]		-	-	22	ns
pulse width	t_w	CP HIGH or LOW; $V_{CC}=4.5V$; see Figure8		24	-	-	ns
		\overline{MR} LOW; $V_{CC}=4.5V$; see Figure10		30	-	-	ns

Recovery time	t_{rec}	$M\bar{R}$ to CP; $V_{CC}=4.5V$; see Figure10	30	-	-	ns
Set-up time	t_{su}	Dn to CP; $V_{CC}=4.5V$; see Figure11	27	-	-	ns
		$P\bar{E}$ to CP; $V_{CC}=4.5V$; see Figure11	45	-	-	ns
		CEP, CET to CP; $V_{CC}=4.5V$; see Figure12	60	-	-	ns
Hold time	t_h	Dn, $P\bar{E}$, CEP, CET to CP; $V_{CC}=4.5V$; see Figure11	0	-	-	ns
Maximum frequency	f_{MAX}	CP; see Figure8	$V_{CC}=4.5V$	15	-	MHz

Note:

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] t_t is the same as t_{THL} and t_{TLH} .

Testing Circuit

AC Testing Circuit

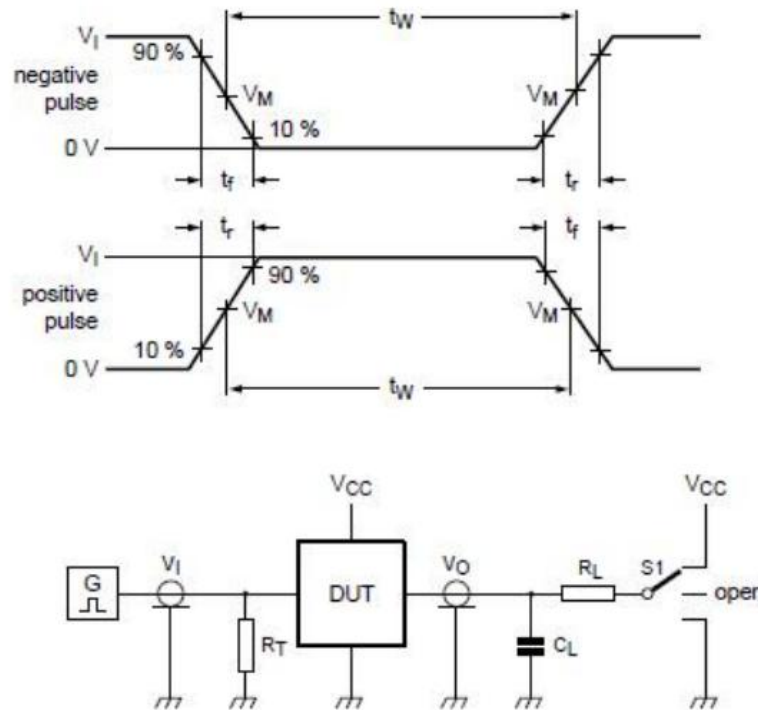


Figure 7. Test circuit for measuring switching times

Definitions for test circuit:

C_L =Load capacitance including jig and probe capacitance.

R_T =Termination resistance should be equal to the output impedance Z_o of the pulse generator.

R_L =Load resistance

S1=Test selection switch

AC Testing Waveforms

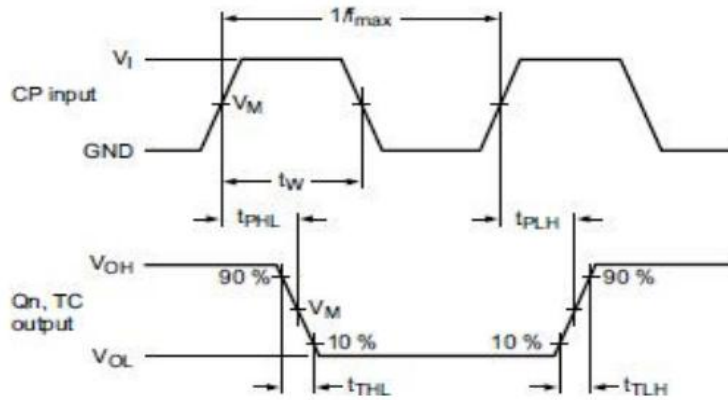


Figure 8. The clock (CP) to outputs (Qn, TC) propagation delays, pulse width, output transition times and maximum frequency

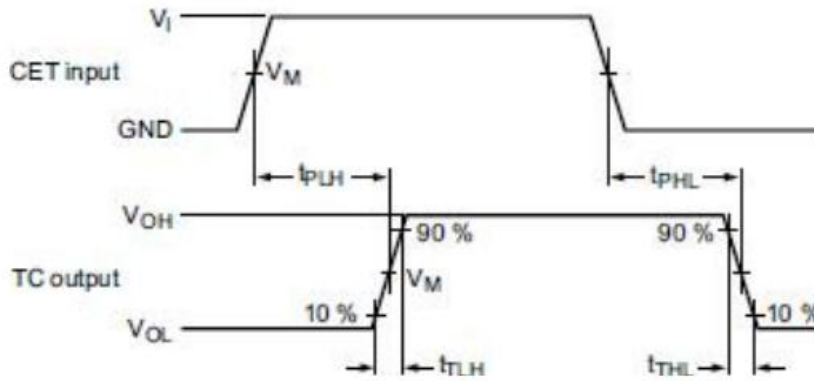


Figure 9. The count enable carry input (CET) to terminal count output (TC) propagation delays and output transition times

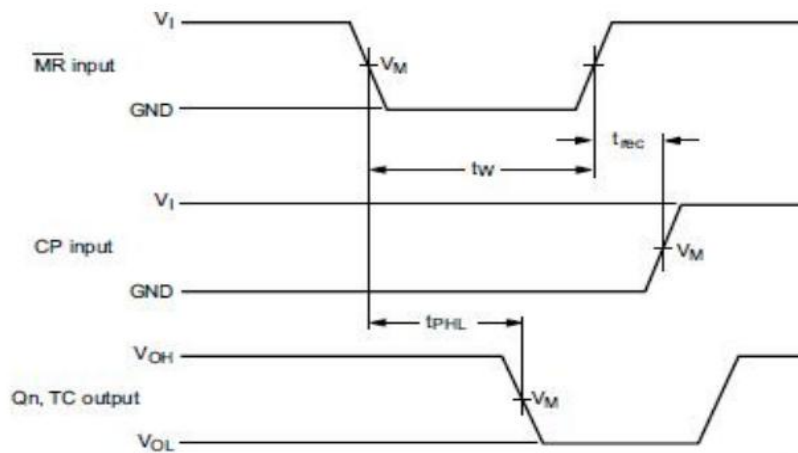


Figure 10. The master reset (\overline{MR}) pulse width, master reset to output (Qn, TC) propagation delays, and the master reset to clock (CP) recovery times

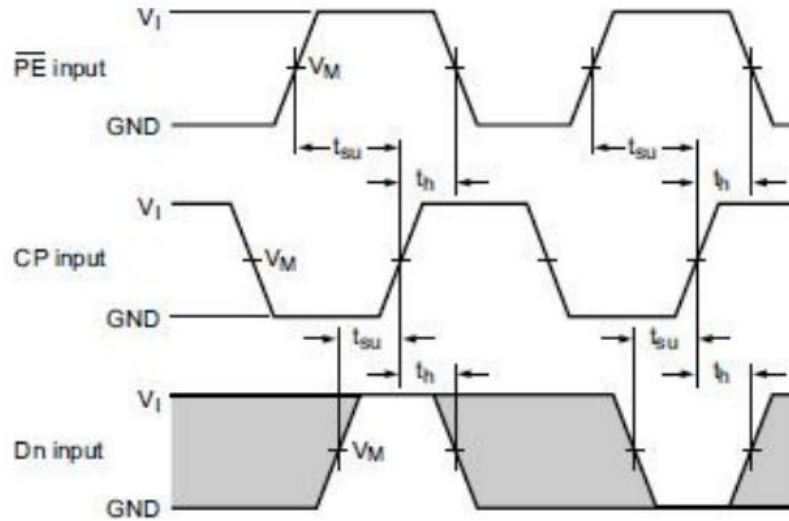


Figure 11. The data input (Dn) and parallel enable input (\overline{PE}) set-up and hold times

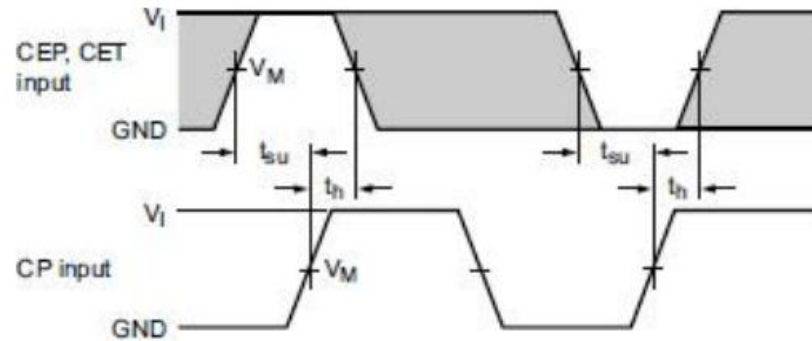


Figure 12. The count enable input (CEP) and count enable carry input (CET) set-up and hold times

Measurement Points

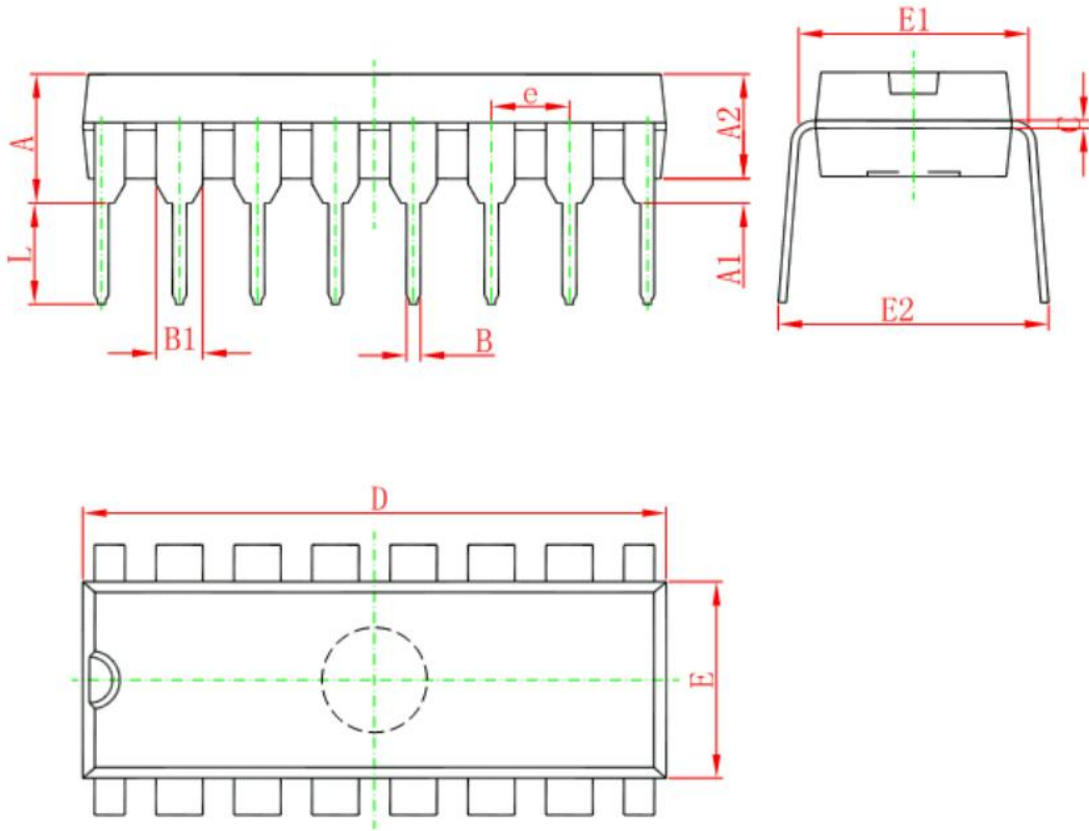
Type	Input		Output
	V_I	V_M	V_M
SN74HC161	GND to V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
SN74HCT161	GND to 3V	1.3V	1.3V

Test Data

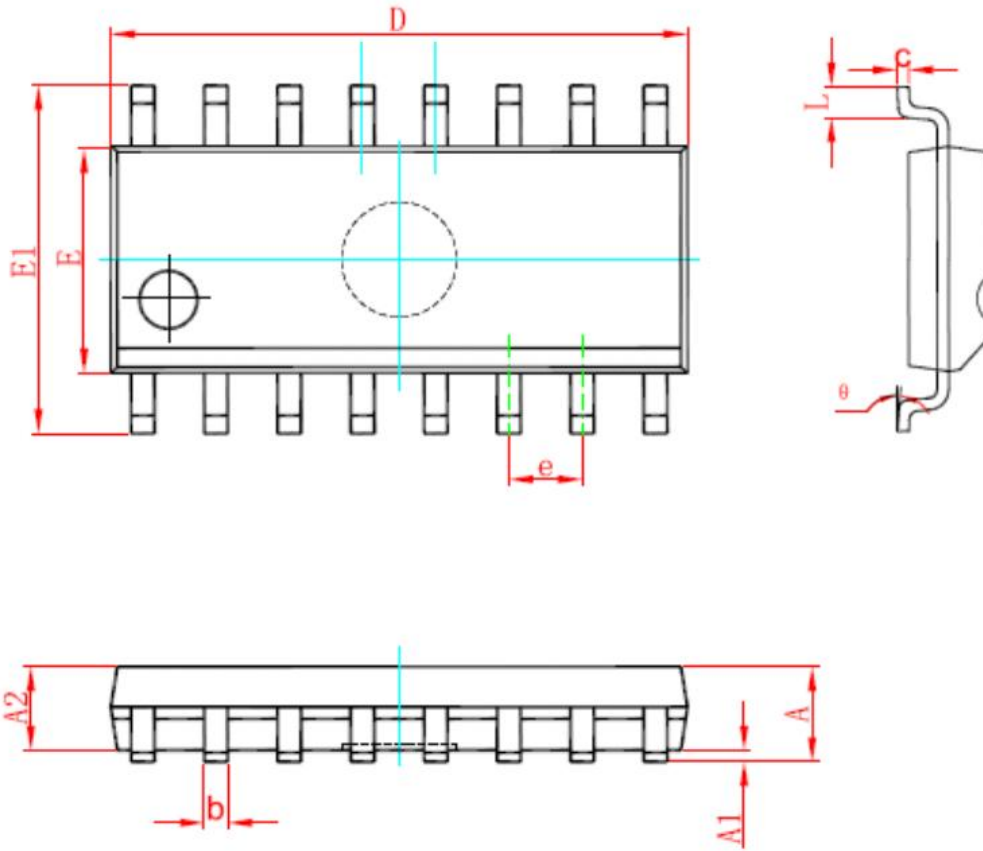
Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
SN74HC161	V_{CC}	6.0ns	15pF, 50pF	1K Ω	open
SN74HCT161	3.0V	6.0ns	15pF, 50pF	1K Ω	open

Package Information

DIP16

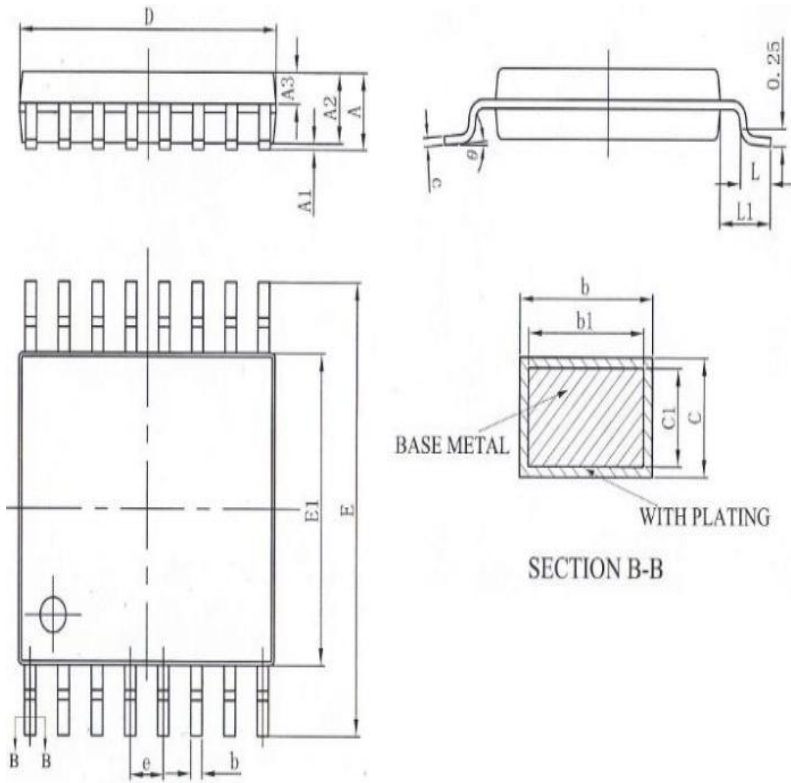


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	18.800	19.200	0.740	0.756
E	6.200	6.600	0.244	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TSSOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	-	0.28
b1	0.19	0.22	0.25
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	-	8°

Statements And Notes

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butyl benzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○: Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×: Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements									

Statement:

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