AUP045N12, AUB045N12

MOSFET Silicon N-Channel MOS

1. Applications

Synchronous rectification in SMPS,
Hard switching and High speed circuit
DC/DC in telecoms and industrial

2. Features

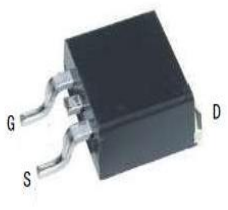
Low drain-source on-resistance: RDS(on) = 4.1mΩ (typ.)
High speed power switching
Enhanced body diode dv/dt capability
Enhanced avalanche ruggedness

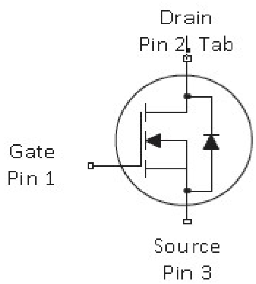
Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	120	V
$R_{DS(on),max}$	4.5	mΩ
$Q_{g,typ}$	178.1	nC
$I_{D,pulse}$	490	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
AUP045N12	TO220	AUP045N12
AUB045N12	TO263	AUB045N12

TO263	TO220
	



1 Maximum ratings

At T_j= 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current at silicon[1]	I_D		-	169	A	T_C=25°C
Continuous drain current at package[1]	I_D		-	152	A	T_C=25°C
Continuous drain current at silicon[1]	I_D			119	A	T_C=100°C
Pulsed drain current[2]	$I_{D,pulse}$	-		490	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	635	mJ	Tc=25℃,VDD=50V,Vgs=10V, L=0.5mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	50.4	A	Tc=25℃, VDD=50V, L=0.5mH, RG=25Ω
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Power dissipation	P_{tot}	-	-	310	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	175	°C	
Operating junction temperature	T_j	-55	-	175	°C	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			300	°C	

[1] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2] Pulse width t_p limited by $T_{j,max}$
[3] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.48	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

atT_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	2.5		4.5	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=120V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	4.1	4.5	mΩ	V_{GS}=10V, I_D=20A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	2.0	-	Ω	f=1MHz, open drain
Transconductance	Gfs		115.8		S	V_{DS}=5V, I_D=50A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	11701	-	pF	V_{GS}=0V, V_{DS}=60V, f=1MHz
Output capacitance	C_{oss}	-	654	-	pF	V_{GS}=0V, V_{DS}=60V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	47	-	pF	V_{GS}=0V, V_{DS}=60V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	V_{DD}=60V,V_{GS}=10V,I_D=50A, R_G=2.5Ω
Rise time	t_r	-	101	-	ns	V_{DD}=60V,V_{GS}=10V,I_D=50A, R_G=2.5Ω
Turn-off delay time	$t_{d(off)}$	-	96	-	ns	V_{DD}=60V,V_{GS}=10V,I_D=50A, R_G=2.5Ω
Fall time	t_f	-	67	-	ns	V_{DD}=60V,V_{GS}=10V,I_D=50A, R_G=2.5Ω

Table 6 Gate charge characteristics

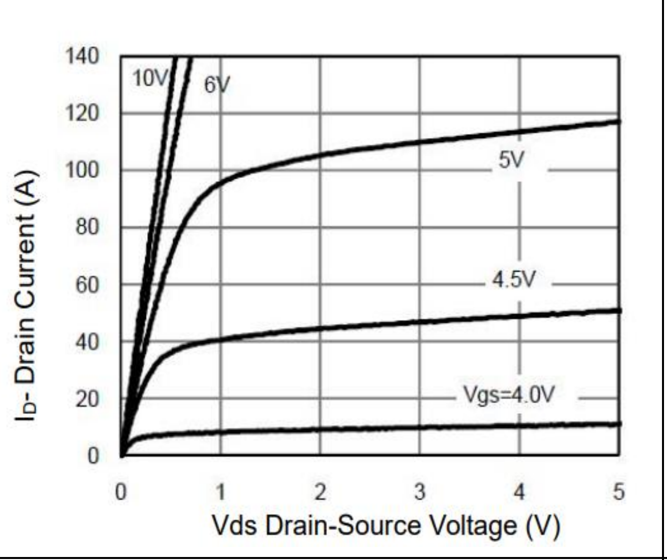
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	45.5	-	nC	V_{DD}=60V, I_D=20A, V_{GS}=10V
Gate to drain charge	Q_{gd}	-	50.0	-	nC	V_{DD}=60V, I_D=20A, V_{GS}=10V
Gate charge total	Q_g	-	178.1	-	nC	V_{DD}=60V, I_D=20A, V_{GS}=10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous Source Current at silicon	I_{SD}	-	-	169	A	*Maximum Ratings*
Diode forward voltage	V_{SD}	-	-	1.2	V	V_{GS}=0V, I_s=1A, T_j=25°C
Reverse recovery time	t_{rr}	-	117.7	-	ns	*Vgs=0V*, I_F=50A, di_F/dt=100A/µs
Reverse recovery charge	Q_{rr}	-	433.8	-	nC	*Vgs=0V*, I_F=50A, di_F/dt=100A/µs
Peak Reverse Recovery Current	I_{rrm}	-	5.48	-	A	*Vgs=0V*, I_F=50A, di_F/dt=100A/µs

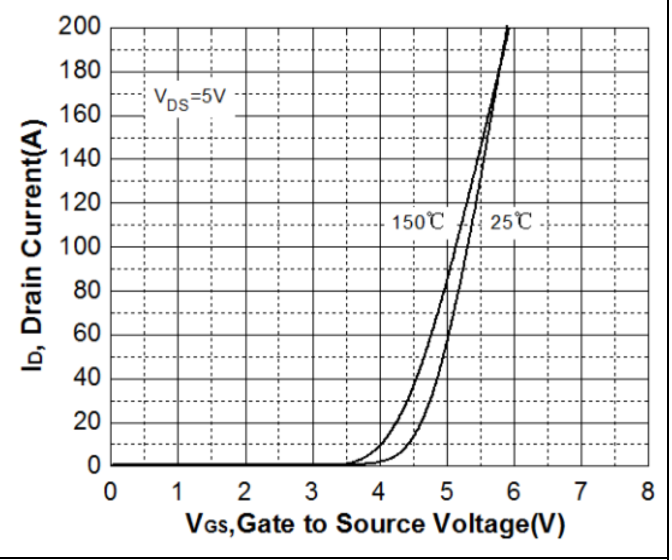
4 Electrical characteristics diagram

Diagram 1: Typ. Output characteristics



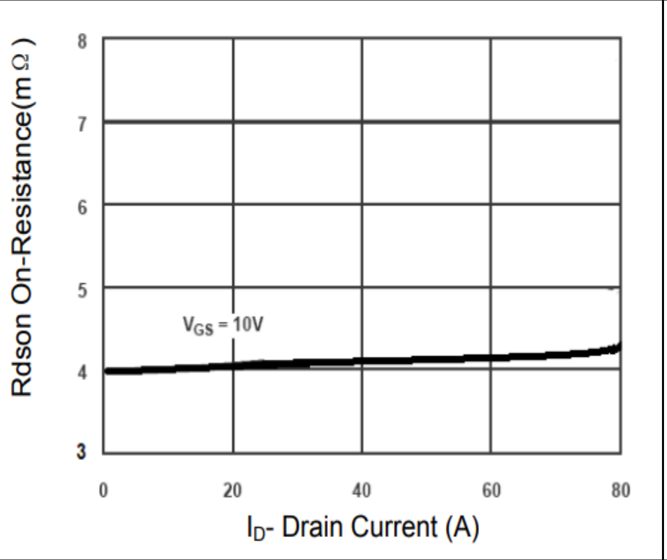
I_D=f(V_{DS});T_j=25 °C; parameter: V_{GS}

Diagram 2: Typ. Transfer characteristics



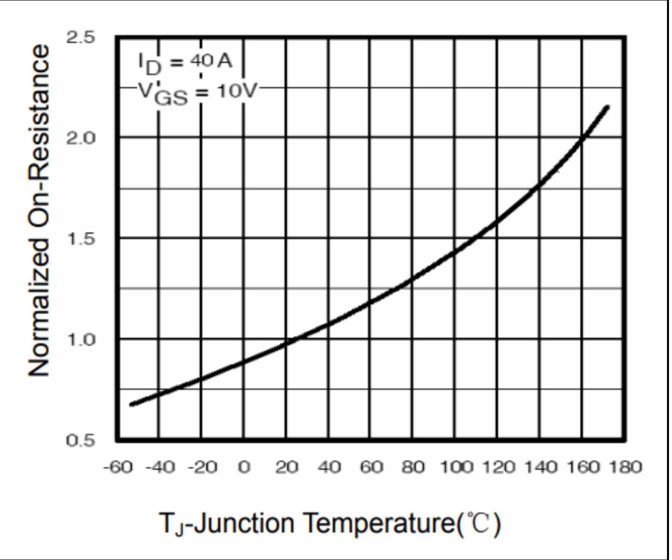
I_D=f(V_{GS});parameter: T_j

Diagram 3: Typ. Rdson vs. Drain Current



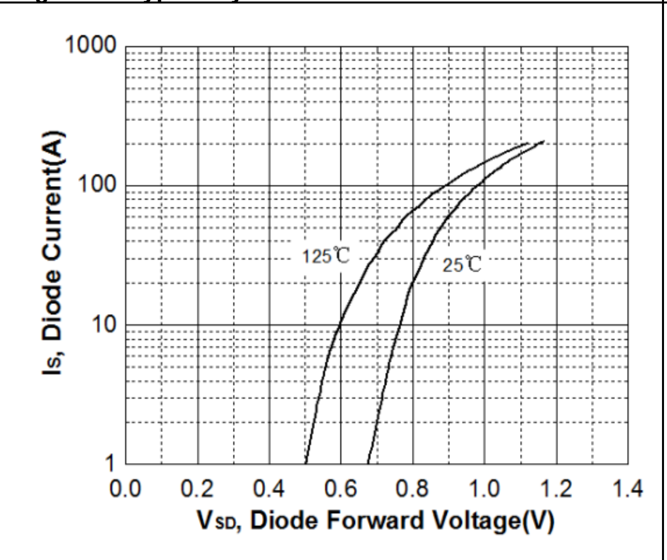
$R_{ds(on)}$=f(Id);Vgs=10V

Diagram 4: Typ. Rdson – Junction Temperature



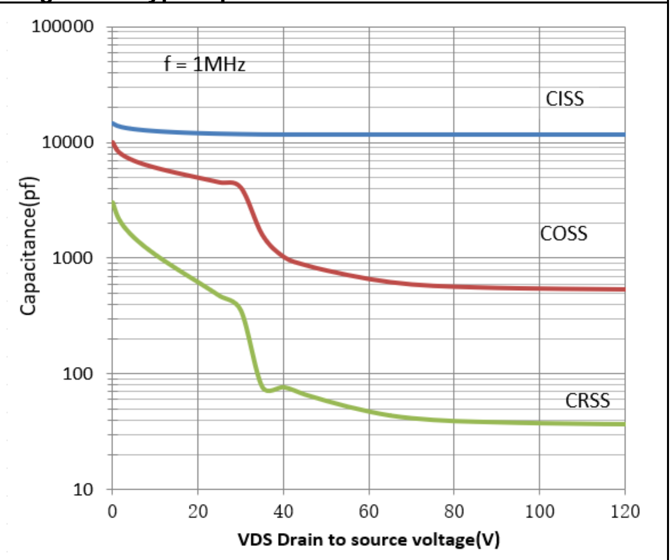
$R_{ds(on)}$=f(T_j);Vgs=10V/I_D=40A

Diagram 5: Typ. Body-Diode Characteristics



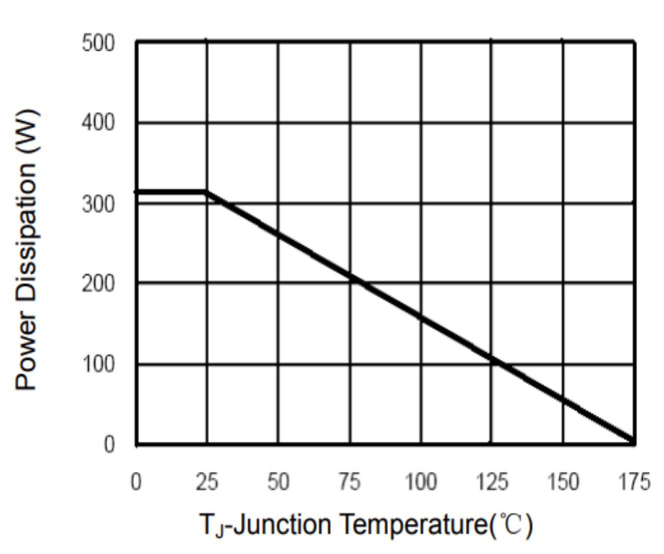
I_F=f(V_{DS});parameter: Tj

Diagram 6: Typ. Capacitance vs. Vds



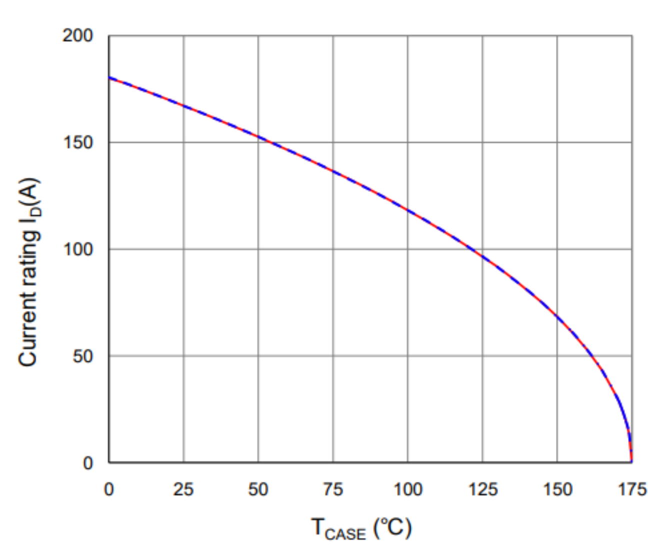
C=f(V_{DS});V_{GS}=0V; f=1MHz

Diagram 7: Typ. Power Dissipation



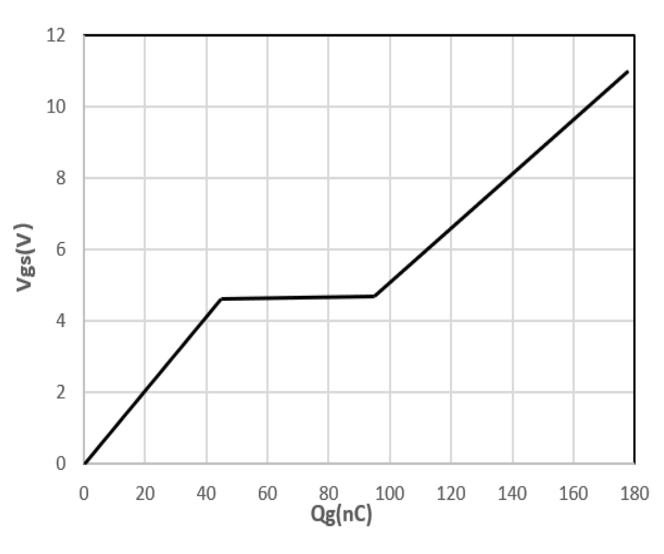
P_{tot}=f(T_C);

Diagram 8: Typ. Drain Current De-rating



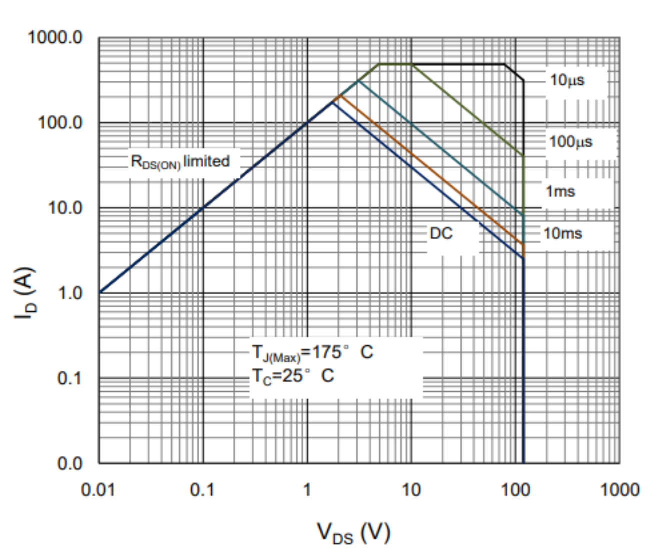
Id=f(T_C);

Diagram 9: Typ. Gate charge



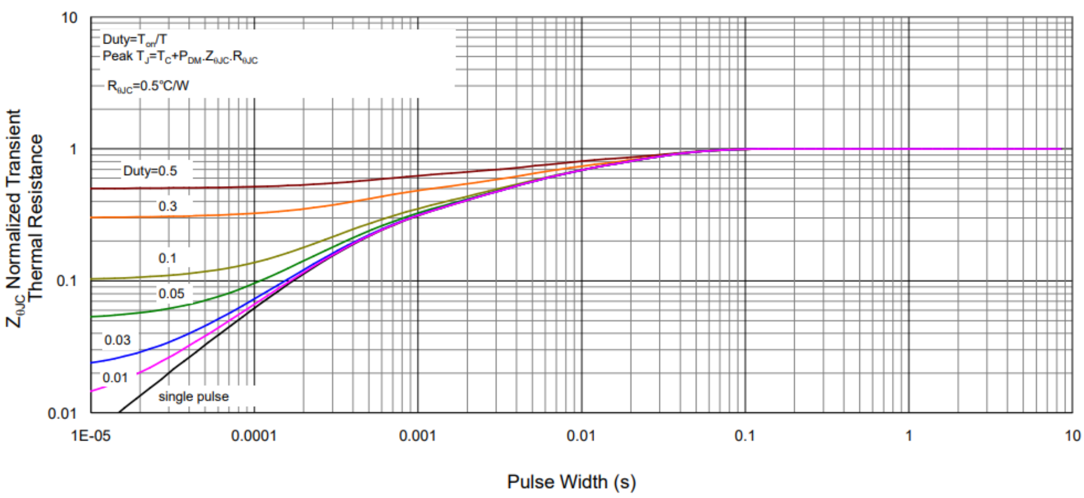
V_{GS}=f(Q_{gate});I_D=20A pulsed; parameter: V_{DD}

Diagram 10: Typ. Maximum Safe Operating Area



I_D=f(V_{DS}); T_C=25 °C; V_{GS}> 7V; D=0; parameter tp

Figure 11 Normalized Maximum Transient Thermal Impedance



5. Test Circuits

Table 8 Diode characteristics

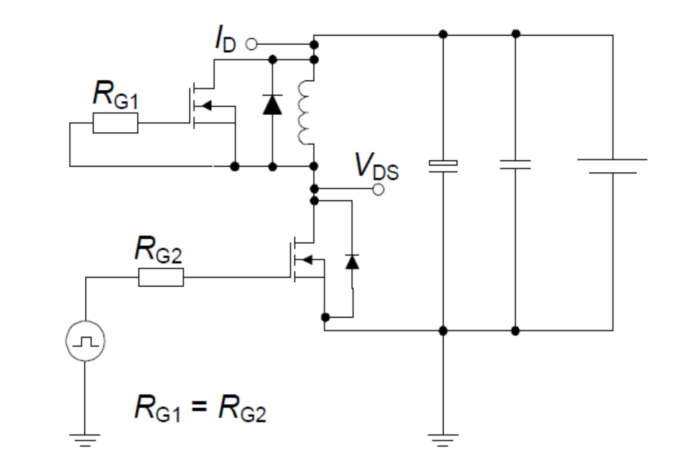
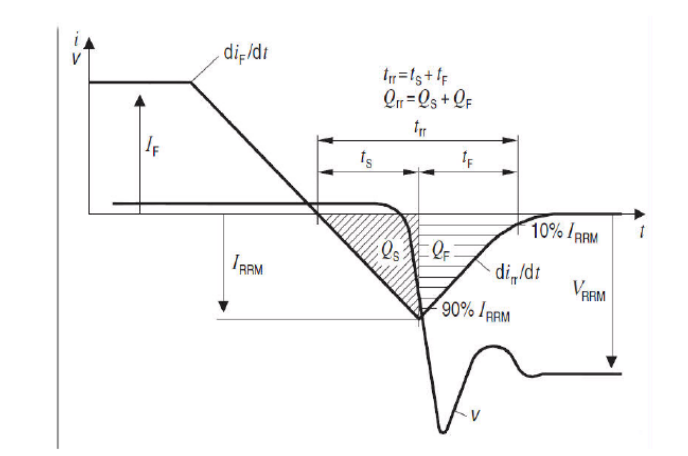
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

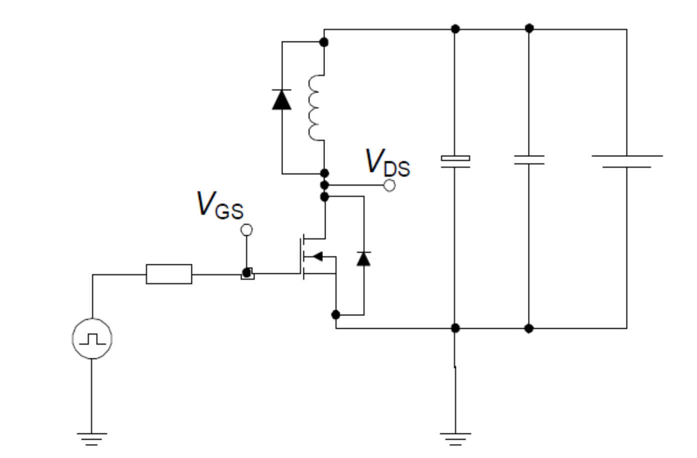
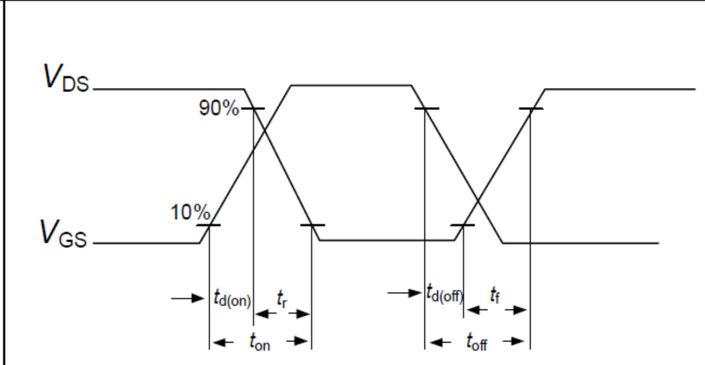
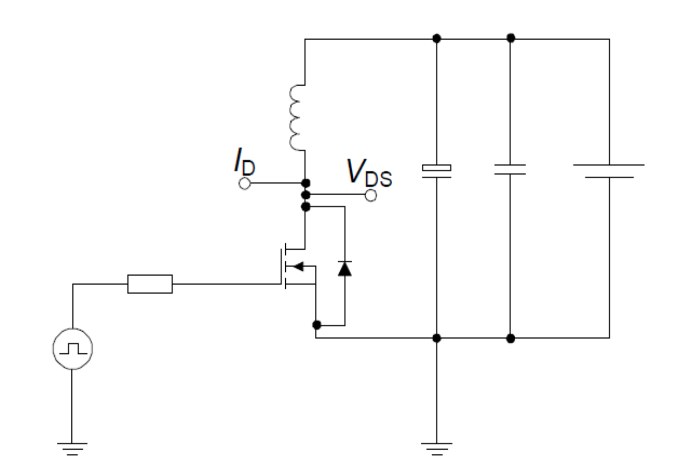
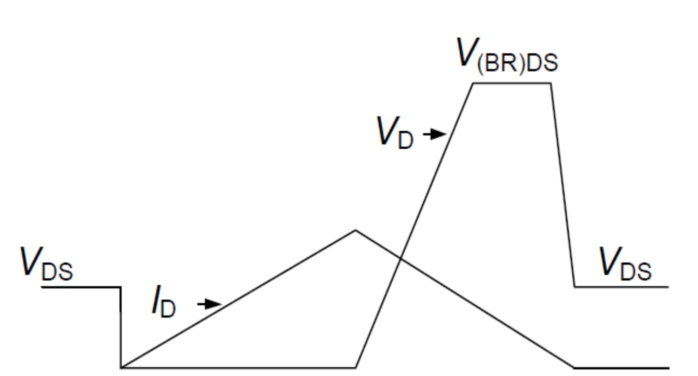
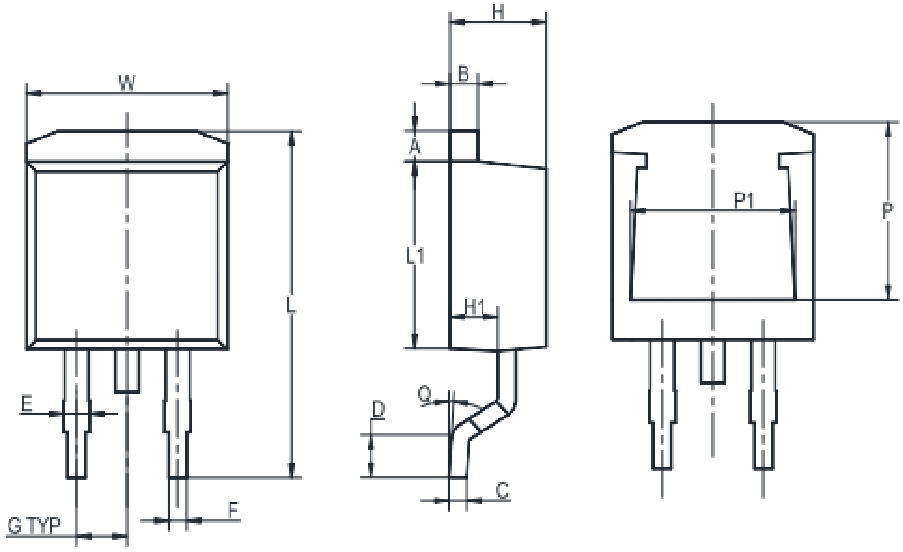
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6. Package Outlines



UNIT	A	B	C	D	E	F	G	W	H	H1	L	L1	Q	P	P1
mm	1.5	1.5	0.5	2.60	1.6	0.94	2.54	10.5	4.8	2.9	16.5	8.7	8°	7.6	8.2
	1.1	1.1	0.3	2.15	1.1	0.68	TYP	9.6	4.4	2.5	14.5	8.2	MAX	7.1	7.4

Figure1：Outline PG-TO263(HC)

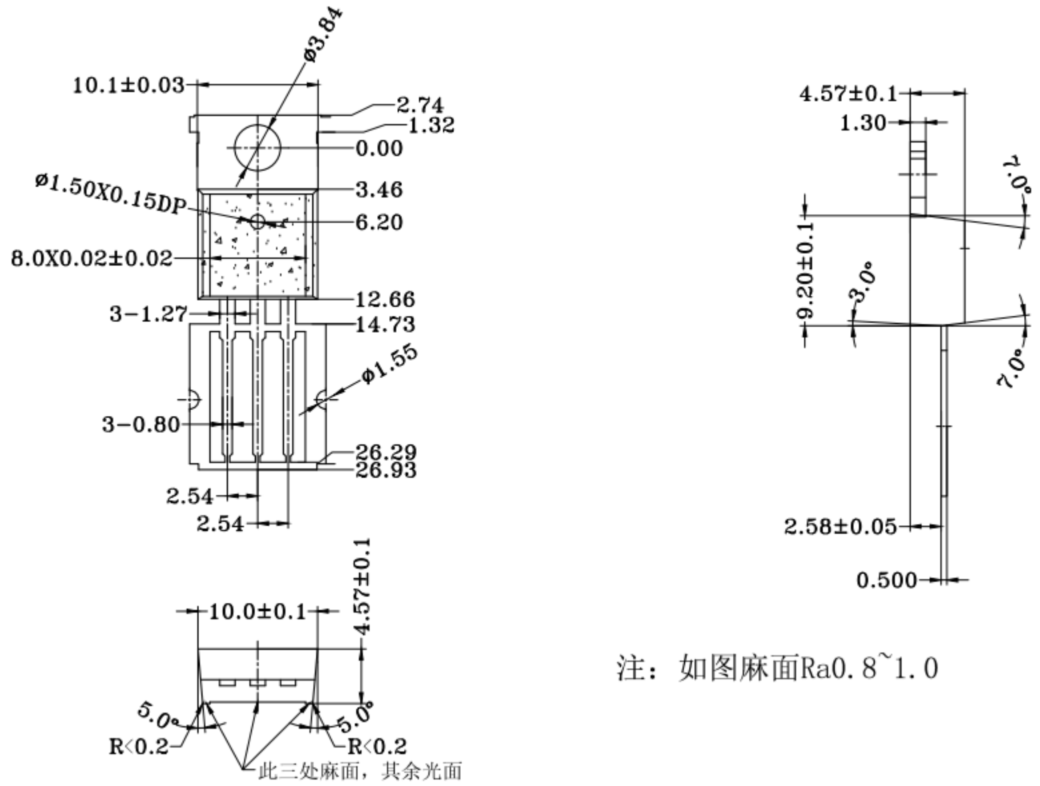


Figure2：Outline PG-TO220(HT)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2023-06-15	Preliminary version
1.1	2023-07-06	Added test circuits