

#### 1MHz, General Purpose, RRIO CMOS Amplifiers

## **General Description**

The HTC321A (single), HTC358A (dual) and HTC324A (quad) are general purpose, low offset, high frequency response and micro power operational amplifiers. With an excellent bandwidth of 1MHz, a slew rate of 0.8V/µs, and a quiescent current of 80µA per amplifier at 5V, the HTC321A/358A/324A family can be designed into a wide range of applications.

The HTC321A/358A/324A op-amps are designed to provide optimal performance in low voltage and low power systems. The input common-mode voltage range includes ground, and the maximum input offset voltage are 4.5mV. These parts provide rail-to-rail output swing into heavy loads. The HTC321A/358A/324A family is specified for single or dual power supplies of +1.8V to +5.5V. All models are specified over the extended industrial temperature range of -40 °C to +125 °C.

The HTC321A is available in 5-lead SOT-23 and SC70-5 package. The HTC358A is available in 8-lead SOP package. The HTC324A is available in 14-lead SOP package.

### Features

- General Purpose 1MHz Amplifiers, Low Cost
- High Slew Rate: 0.8V/µs
- Low Offset Voltage: 4.5 mV Maximum
- Low Power: 80µA per Amplifier Supply Current
- Settling Time to 0.1% with 2V Step: 4.2 μs
- Unit Gain Stable
- Rail-to-Rail Input and Output
  - Input Voltage Range: -0.1V to +5.1V at 5V Supply

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### **Applications**

- Smoke/Gas/Environment Sensors
- Audio Outputs
- Battery and Power Supply Control
- Portable Equipment and Mobile Devices
- Active Filters
- Sensor Interfaces





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### Applications









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## **Ordering Information**

Type Number	Package	Number of package	Description
HTC321AXC5/R6	SC70-5	3000 PCS	C21YW
HTC321AXT5/R6	SOT23-5	3000 PCS	C21AYW
HTC358AXS8/R8	SOP-8	4000 PCS	C358A XXXXX
HTC324AXS14/R5	SOP-14	2500 PCS	C324A XXXXX
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## Absolute Maximum Ratings (T<sub>A</sub>= 25°C)

Symbol	Description	Value	Units
$V_{S^+\!,}V_{S^-}$	Supply Voltage, $V_{S^+}$ to $V_{S^-}$	7.0	KE V
V <sub>CM</sub>	Common-Mode Input Voltage	$V_{S-} - 0.3$ to $V_{S+} + 0.3$	v
ECD		HBM ±4000	V
ESD	Electrostatic Discharge Voltage	CDM ±2000	V
TJ	Junction Temperature	160	°C
Tstg	Storage Temperature Range	-65 to +150	°C(TJ)
Тл	Lead Temperature Range (Soldering 10 sec)	260	°C

#### Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods and affect device reliability.
Provided device does not exceed maximum junction temperature (T<sub>J</sub>) at any time. may affect device reliability.





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### **Electrical Characteristics**

		$5/2$ , and $R_{\rm L}$ = 10kS2 connected to $4$	<i>5,2</i> , unicss		fieu.	70 I	
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit	
INPUT CHA	ARACTERISTICS		N K				
Vos	Input offset voltage	ALL ALL	-4.5	±1.0	+4.5	mV	
	Over temperature	ALCONT T	-4.8		+4.8		
$V_{\text{OS}}\text{TC}$	Offset voltage drift	Over Temperature		2.3		µV/°C	
IB	Input bias current			1		pА	
1D	Over temperature			500			
Ios	Input offset current			1		pА	
V <sub>CM</sub>	Common-mode voltage range		V <sub>S-</sub> -0.1		V <sub>S+</sub> +0.1	v	
	Common-mode rejection ratio	N 0.05N/+ 2.5N		90 P	110	dB	
CMRR	Over temperature	VCM - 0.03 V to 5.5 V	. Ć	85			
CIVIKK		$V_{CM} = V_{S-} - 0.1$ to $V_{S+} + 0.1$ V	x 2 x	80			
	Over temperature		-	75			
$\mathbf{A}_{\mathrm{VOL}}$	Open-loop voltage gain	$V_0 = 0.05 \text{ to } 3.5 \text{ V}$		110		dB	
	Over temperature	v0-x.05 t0 5.5 v		100			
$R_{\rm IN}$	Input resistance		100			GΩ	
C <sub>IN</sub>	Input capacitance	Differential		2.0		υF	
	PET	Common mode		3.5	.0	P-	
OUTPUT CH	HARACTERISTICS			2	100	1	
V <sub>OH</sub>	High output voltage swing			V <sub>S+</sub> -8	1/-	mV	
Vol	Low output voltage swing		S X	8		mV	
Z <sub>OUT</sub>	Closed-loop output impedance	f = 200  kHz, G = +1	332	0.4		Ω	
	Open-loop output impedance	$f = 1 MHz, I_0 = 0$		2.6			
I <sub>SC</sub>	Short circuit current	Source current through $10\Omega$		40		m۸	
	Short-encunt current	Sink current through $10\Omega$		40		111/3	
DYNAMIC	PERFORMANCE						
GBW	Gain bandwidth product			1.0		MHz	
$\Phi_{\rm M}$	Phase margin	$C_L = 100 pF$		62		o	
		$G = +1$ $C_{\rm T} = 100 {\rm pF}$					





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Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
ts	Settling time	To 0.1%, G = +1, 2V step	. >	4.2		
		To 0.01%, G = +1, 2V step	0 3 ×	5.2		μs
t <sub>OR</sub>	Overload recovery time	$V_{IN} * Gain > V_S$		2		μs
THD+N	Total harmonic distortion+Noise	$f = 1 \text{kHz}, G = +1, V_{O} = 3 V_{PP}$		0.003		%
NOISE PEF	RFORMANCE	A EX				
$V_n$	Input voltage noise	f = 0.1 to 10 Hz		13		μV <sub>P-P</sub>
en	Input voltage noise density	f=1kHz		35		nV/√H
In	Input current noise density	f=10kHz		6	7.	fA/√H
OWER SU	JPPLY	·		0	RIF	t.
Vs	Operating supply voltage		1.8	CT V	5.5	v
DCDD	Power supply rejection ratio	$V_{S} = 2.7V$ to 5.5V, $V_{CM} < V_{S+} - 2V$	0 **	98		ID
PSKK	Over temperature		ΞX	85		dB
IQ	Quiescent current (per amplifier)	- MIC PA		80	120	A
	Over temperature	J.S.F.		85	130	μΑ
HERMAL	CHARACTERISTICS	No series and the series of th				
T <sub>A</sub>	Operating temperature range		-40		+125	°C
	PPE 1	SOT23-5		190		C/W
$\theta_{JA}$	Package thermal resistance	SO-8		125	215	
		SO-14		115	R	
ecification	ns subject to changes without r	SENICAL				





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### **Typical Performance Characteristics**



Time (4 µs/div)

Figure 7 Small-Signal Step Response at 2.7V



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Figure 6 Large-Signal Step Response at 2.7V

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### **Typical Performance Characteristics**







### **Application Notes**

#### **1. LOW INPUT BIAS CURRENT**

The HTC321A/358A/324A family is a CMOS op-amp family and features very low input bias current in pA range. The low input bias current allows the amplifiers to be used in applications with high resistance sources. Care must be taken to minimize PCB Surface Leakage. See below section on "PCB Surface Leakage" for more details.

#### **2. PCB SURFACE LEAKAGE**

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5pA of current to flow, which is greater than the HTC321A/358A/324A's input bias current at +25°C (±1pA, typical). It is recommended to use multi-layer PCB layout and route the op-amp's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 10 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

a) Connect the non-inverting pin (+IN) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (-IN). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (+IN). This biases the guard ring to the same reference voltage as the op-amp (e.g.,  $V_s/2$  or ground).

b) Connect the inverting pin (-IN) to the input with a wire that does not touch the PCB surface.



Figure 10 Use a guard ring around sensitive pins







### **Application Notes**

#### **3. GROUND SENSING AND RAIL TO RAIL**

The input common-mode voltage range of the HTC321A/358A/324A series extends 100mV beyond the supply rails. This is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair. For normal operation, inputs should be limited to this range. The absolute maximum input voltage is 300mV beyond the supplies. Inputs greater than the input common-mode range but less than the maximum input voltage, while not valid, will not cause any damage to the op-amp. Unlike some other op-amps, if input current is limited, the inputs may go beyond the supplies without phase inversion, as shown in Figure 11. Since the input common-mode range extends from (V<sub>S-</sub> – 0.1V) to (V<sub>S+</sub> + 0.1V), the HTC321A/358A/324A op-amps can easily perform 'true ground' sensing.



Figure 11 No Phase Inversion with Inputs Greater Than the Power-Supply Voltage

A topology of class AB output stage with common-source transistors is used to achieve rail-to-rail output. For light resistive loads (e.g.  $100k\Omega$ ), the output voltage can typically swing to within 5mV from the supply rails. With moderate resistive loads (e.g.  $10k\Omega$ ), the output can typically swing to within 10mV from the supply rails and maintain high open-loop gain.

The maximum output current is a function of total supply voltage. As the supply voltage to the amplifier increases, the output current capability also increases. Attention must be paid to keep the junction temperature of the IC below 150°C when the output is in continuous short-circuit. The output of the amplifier has reverse-biased ESD diodes connected to each supply. The output should not be forced more than 0.5V beyond either supply, otherwise current will flow through these diodes.

### 4. CAPACITIVE LOAD AND STABILITY

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The HTC321A/358A/324A can directly drive 1nF in unity-gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even



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### **Application Notes**

oscillation. Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 12. The isolation resistor  $R_{ISO}$  and the load capacitor  $C_L$  form a zero to increase stability. The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. Note that this method results in a loss of gain accuracy because  $R_{ISO}$  forms a voltage divider with the  $R_L$ .



An improvement circuit is shown in Figure 13. It provides DC accuracy as well as AC stability. The  $R_F$  provides the DC accuracy by connecting the inverting signal with the output. The  $C_F$  and  $R_{ISO}$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.



Figure 13 Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain, or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

## 5. POWER SUPPLY LAYOUT AND BYPASS

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The HTC321A/358A/324A family operates from either a single +1.8V to +5.5V supply or dual  $\pm 0.9V$  to  $\pm 2.75V$  supplies. For single-supply operation, bypass the power supply Vs



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with a ceramic capacitor (i.e.  $0.01\mu$ F to  $0.1\mu$ F) which should be placed close (within 2mm for good high frequency performance) to the V<sub>s</sub> pin. For dual-supply operation, both the V<sub>s+</sub> and the V<sub>s-</sub> supplies should be bypassed to ground with separate  $0.1\mu$ F ceramic capacitors. A bulk capacitor (i.e.  $2.2\mu$ F or larger tantalum capacitor) within 100mm to provide large, slow currents and better performance. This bulk capacitor can be shared with other analog parts.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op-amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible. For the op-amp, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

#### **6. GROUNDING**

A ground plane layer is important for the HTC321A/358A/324A circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

#### 7. INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

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## **Typical Application Circuits**



Figure 15 Instrumentation Amplifier

The HTC321A/358A/324A family is well suited for conditioning sensor signals in battery-powered applications. Figure 15 shows a two op-amp instrumentation amplifier, using the HTC358A op-amps. The circuit works well for applications requiring rejection of common-mode noise at higher gains. The reference voltage ( $V_{REF}$ ) is supplied by a low-impedance source. In single voltage supply applications, the  $V_{REF}$  is typically  $V_S/2$ .

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### **Typical Application Circuits**



The HTC321A/358A/324A family has input bias current in the pA range. This is ideal in buffering high impedance chemical sensors, such as pH probes. As an example, the circuit in Figure 16 eliminates expansive low-leakage cables that is required to connect a pH probe (general purpose combination pH probes, e.g Corning 476540) to metering ICs such as ADC, AFE and/or MCU. An HTC321A/358A/324A op-amp and a lithium battery are housed in the probe assembly. A conventional low-cost coaxial cable can be used to carry the op-amp's output signal to subsequent ICs for pH reading.

#### 4. SHUNT-BASED CURRENT SENSING AMPLIFIER

The current sensing amplification shown in Figure 8 has a slew rate of  $2\pi f V_{PP}$  for the output of sine wave signal, and has a slew rate of  $2fV_{PP}$  for the output of triangular wave signal. In most of motor control systems, the PWM frequency is at 10kHz to 20kHz, and one cycle time is 100µs for a 10kHz of PWM frequency. In current shunt monitoring for a motor phase, the phase current is converted to a phase voltage signal for ADC sampling. This sampling voltage signal must be settled before entering the ADC. As the Figure 19 shown, the total settling time of a current shunt monitor circuit includes: the rising edge delay time (t<sub>SR</sub>) due to the op-amp's slew rate, and the measurement settling time (t<sub>SET</sub>). For a 3-shunt solution in motor phase current sensing, if the smaller duty cycle of the PWM is defined at 45% (In fact, the phase with minimum PWM duty cycle, such as 5%, is not detected current directly, and it can be calculated from the other two phase currents), and the t<sub>SR</sub> is required at 20% of a total time window for a phase current monitoring, in case of a 3.3V motor control system(3.3V MCU with 12-bit ADC), the op-amp's slew rate should be more than:





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### **Typical Application Circuits**



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### **Package Information**





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### **Package Information**



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