MOSFET Silicon N-Channel MOS

1. Applications

Synchronous rectification in SMPS,
Hard switching and High speed circuit
DC/DC in telecoms and industrial

2. Features

Low drain-source on-resistance:
TOLL-8L RDS(on) = 1.2mΩ (typ.)
High speed power switching
Enhanced body diode dv/dt capability
Enhanced avalanche ruggedness

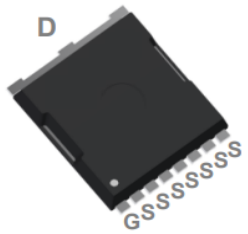
Table 1 Key Performance Parameters

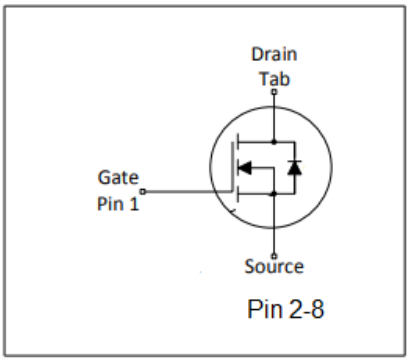
Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	100	V
$R_{DS(on),max}$	1.4	mΩ
$Q_{g,typ}$	231	nC
$I_{D,pulse}$	987	A

3. Packaging and Internal Circuit

Part Name	Package	Marking
AUR014N10	TOLL	AUR014N10

TOLL





1 Maximum ratings

At T_j= 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current at sikicon[1)]	I_D		-	395	A	T_C=25°C
Continuous drain current at package[1)]	I_D		-	316	A	T_C=25°C
Continuous drain current at silicon[1)]	I_D			250	A	T_C=100°C
Pulsed drain current[2)]	$I_{D,pulse}$	-		987	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	1250	mJ	Tc=25°C,VDD=50V,Vgs=10V, L=1mH, RG=25Ω
Avalanche current, single pulse	I_{AR}	-	-	50	A	Tc=25°C, VDD=50V, L=1mH, RG=25Ω
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Power dissipation	P_{tot}	-	-	313	W	T_C=25°C
Storage temperature	T_{stg}	-55	-	150	°C	
Operating junction temperature	T_j	-55	-	150	°C	
Soldering Temperature Distance of 1.6mm from case for 10s	T_L			260	°C	

[1)] Limited by $T_{j,max}$. Maximum Duty Cycle D = 0.50
[2)] Pulse width t_p limited by $T_{j,max}$
[3)] Identical low side and high side switch with identical R_G

2 Thermal characteristics

Table Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.4	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	40	°C/W	device on PCB, minimal footprint

3 Electrical characteristics

At T_j=25°C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{(GS)th}$	2		4	V	V_{DS}=V_{GS}, I_D=250uA
Zero gate voltage drain current	I_{DSS}	-	-	1	uA	V_{DS}=80V, V_{GS}=0V, T_j=25°C
Gate-source leakage current	I_{GSS}	-	-	+/-100	nA	V_{GS}=+/-20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	-	1.4	mΩ	V_{GS}=10V, I_D=30A, T_j=25°C
Gate resistance (Intrinsic)	R_G	-	0.7	-	Ω	f=1MHz, open drain
Transconductance	Gfs		108		S	V_{DS}=$5V$, I_D=50A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	13000	-	PF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Output capacitance	C_{oss}	-	2147	-	PF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Reverse transfer capacitance	C_{rss}	-	398	-	PF	V_{GS}=0V, V_{DS}=50V, f=1MHz
Turn-on delay time	$t_{d(on)}$	-	27.7	-	ns	V_{DD}=50V,V_{GS}=10V,I_D=1A, R_G=1Ω
Rise time	t_r	-	21.5	-	ns	V_{DD}=50V,V_{GS}=10V,I_D=1A, R_G=1Ω
Turn-off delay time	$t_{d(off)}$	-	89.6	-	ns	V_{DD}=50V,V_{GS}=10V,I_D=1A, R_G=1Ω
Fall time	t_f	-	96.8	-	ns	V_{DD}=50V,V_{GS}=10V,I_D=1A, R_G=1Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	70.2	-	nC	V_{DD}=50V, I_D=100A, V_{GS}=10V
Gate to drain charge	Q_{gd}	-	65.7	-	nC	V_{DD}=50V, I_D=100A, V_{GS}=10V
Gate charge total	Q_g	-	231	-	nC	V_{DD}=50V, I_D=100A, V_{GS}=10V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous Source Current at silicon	I_{SD}	-	-	395	A	*Maximum Ratings*
Diode forward voltage	V_{SD}	-	0.75	1.1	V	V_{GS}=0V, I_S=30A, T_j=25°C
Reverse recovery time	t_{rr}	-	120	-	ns	*Vgs=0V*, I_F=30A, di_F/dt=100A/µs
Reverse recovery charge	Q_{rr}	-	400	-	nC	*Vgs=0V*, I_F=30A, di_F/dt=100A/µs

4 Electrical characteristics diagram

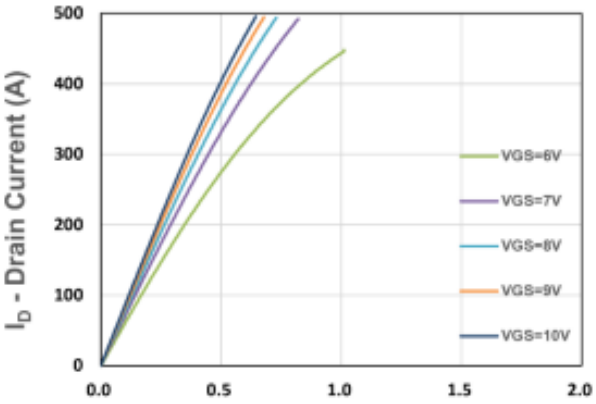


Figure 1. Output Characteristics

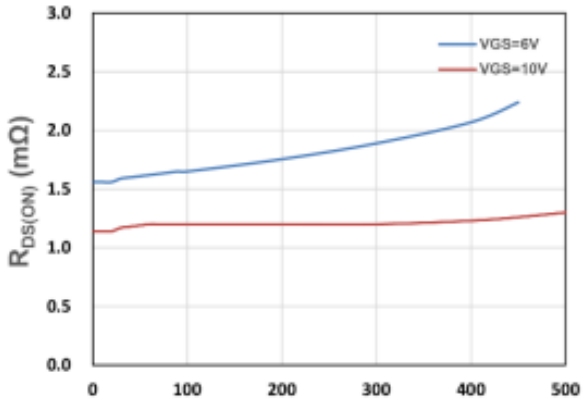


Figure 2. On-Resistance vs. ID

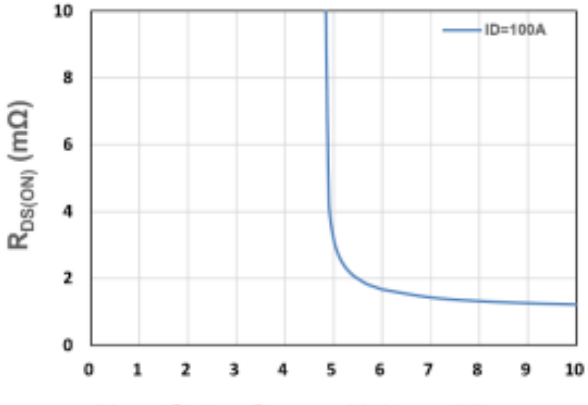


Figure 3. On-Resistance vs. VGS

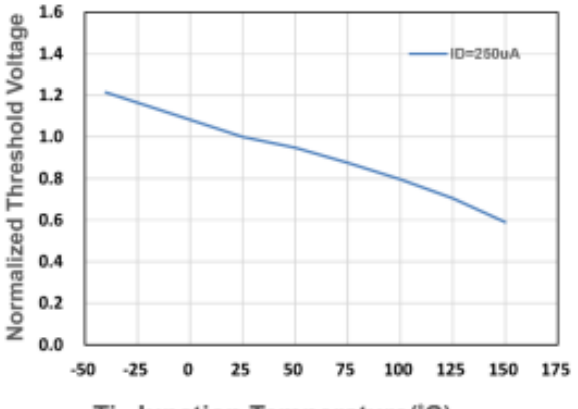


Figure 4. Gate Threshold Voltage

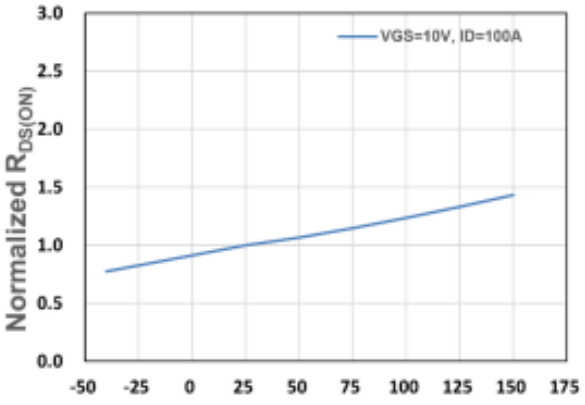


Figure 5. Drain-Source On Resistance

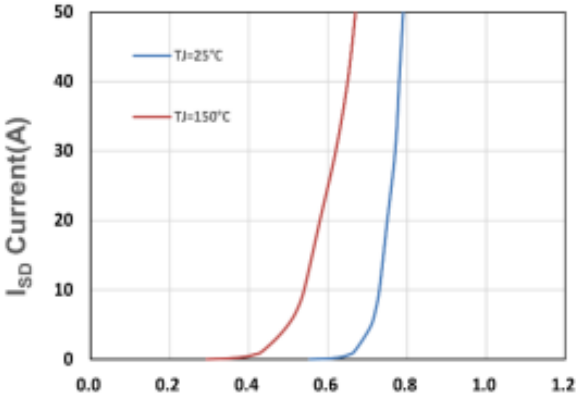


Figure 6. Source-Drain Diode Forward

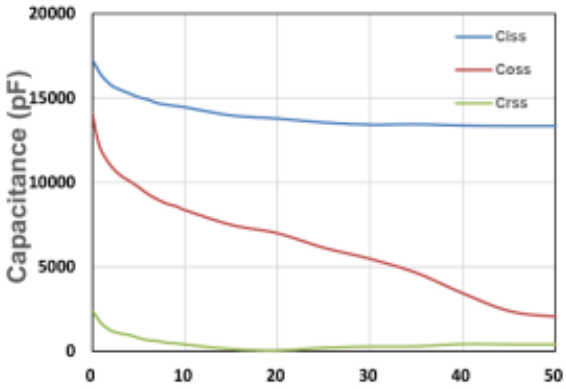


Figure 7. Capacitance

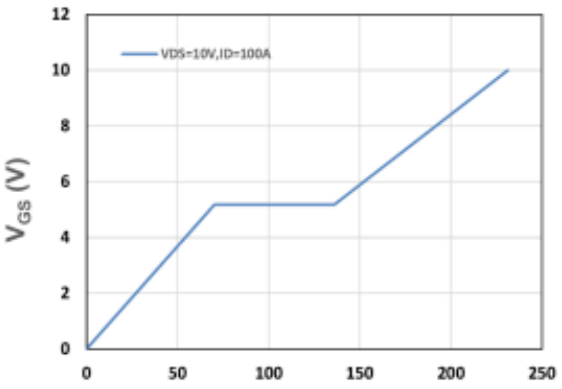


Figure 8. Gate Charge Characteristics

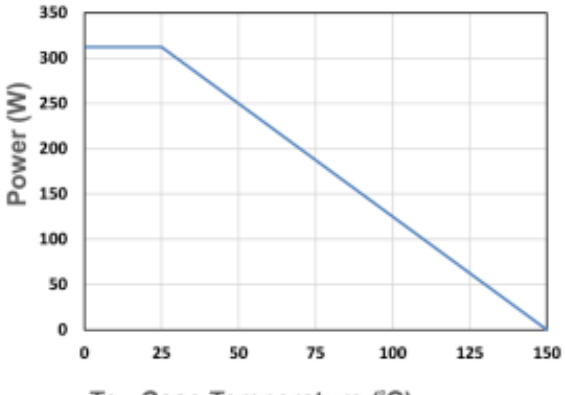


Figure 9. Power Dissipation

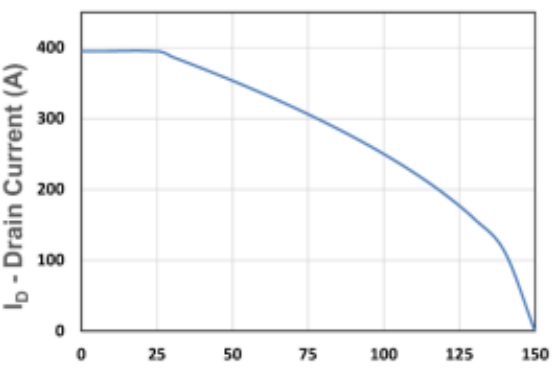


Figure 10. Drain Current

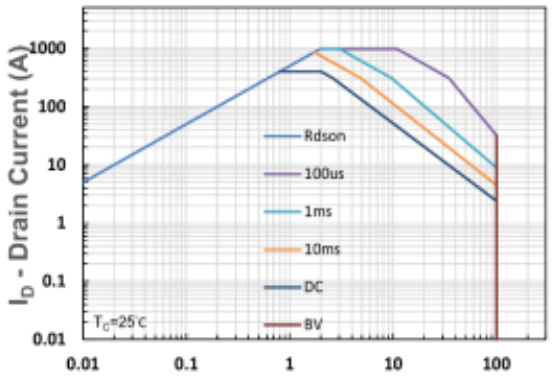


Figure 11. Safe Operating Area

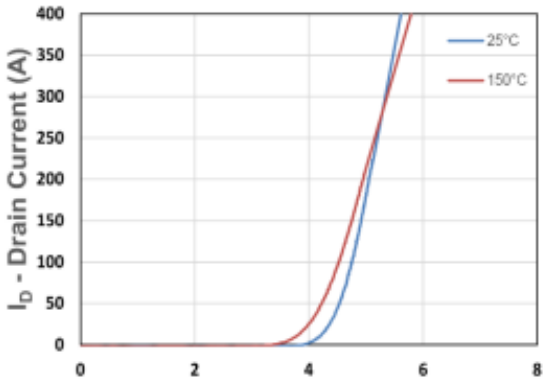


Figure 12. Transfer Characteristics

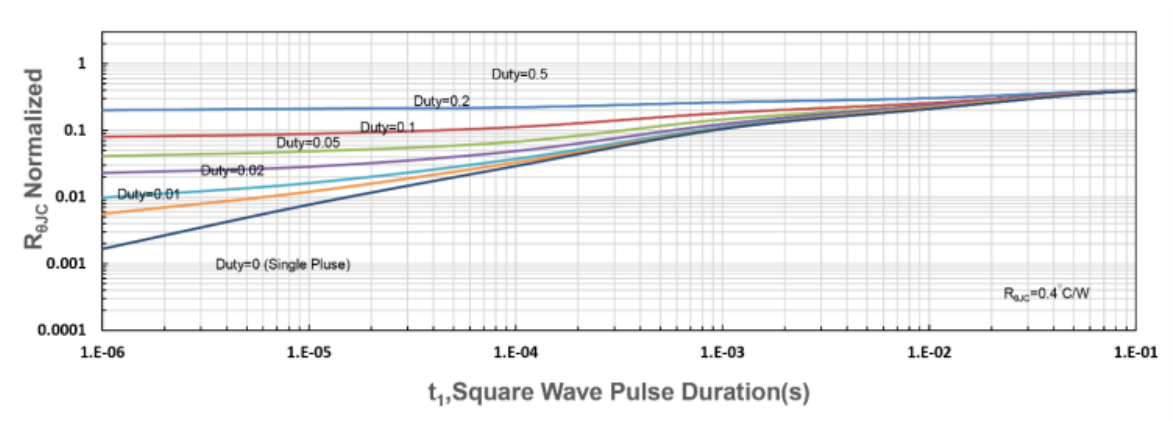
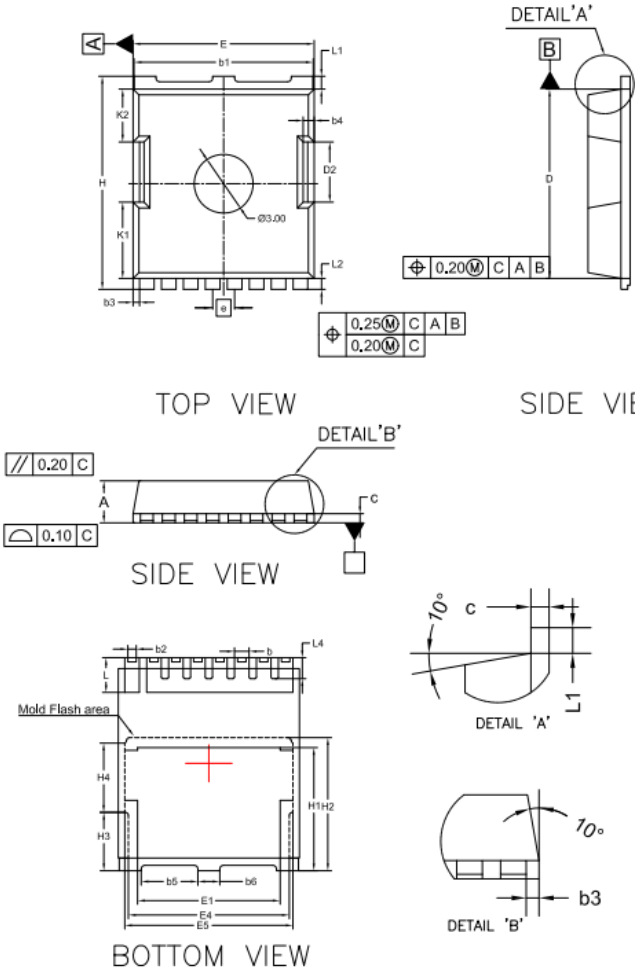


Figure 13. RθJC Transient Thermal Impedance

5. Package Outline



SYMBOLS	DIMENSION IN MM		
	MIN	NOM	MAX
* A	2.200	2.300	2.400
c	0.492	0.500	0.508
* D	10.280	10.380	10.480
* E	9.800	9.900	10.000
e		1.20 BSC	
* H	11.580	11.680	11.780
H1	6.650	6.750	6.850
H2		7.300	
H3		3.200	
H4		3.800	
K1		4.180	
K2		2.900	
* D2		3.300	
b	0.700	0.800	0.900
b1	9.700	9.800	9.900
b2	0.420	0.460	0.500
b3		0.350	
b4		0.600	
b5		3.100	
b6		1.200	
L	1.700	1.900	2.100
L1		0.700	
L2		0.600	
L4	1.050	1.150	1.250
L5	0.500	0.600	0.700
E1		7.800	
E4		8.800	
E5		9.200	

Figure： Outline PG-TOLL(JW)

Revision History

Revision	Date	Subjects (major changes since last revision)
1.0	2023-05-26	Preliminary version