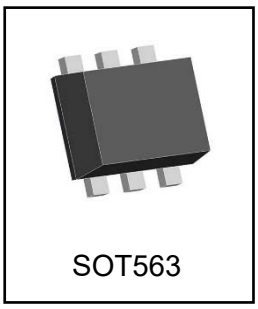
5.5V, 3A, 1.1MHz, Synchronous

Step-Down Converter with 25μA Low Quiescent Current

LA1163S

Overview


SOT563

The LA1163S is a high frequency (1.1MHz) step-down switching regulator with integrated internal power MOSFETs. It achieves 3A of continuous output current from a 2.5V to 5.5V input voltage range with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

The constant-on-time (COT) control scheme in forced continuous conduction mode (CCM) provides a fast transient response, a low output voltage ripple, and eases loop stabilization. Fault protections include cycle-by-cycle current limiting and thermal shutdown. The LA1163S is available in an ultra-small SOT563 package and requires a minimal number of readily available, standard, external components.

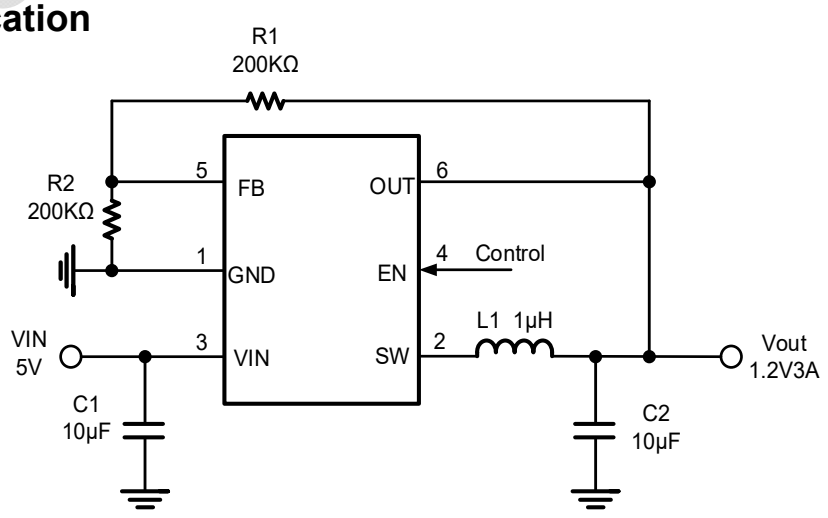
Features

- 2.5V to 5.5V Input Voltage Range Supporting
- 25μA Low Quiescent Current
- Up to 3A Output Current
- Output Adjustable from 0.6V
- 65mΩ and 35mΩ Internal Power MOSFETs
- 100% Maximum Duty Cycle
- 1.1MHz fixed Switching Frequency
- Output Discharge
- Stable Short-Circuit Protection (SCP) with Hiccup
- Stable with Low ESR Output Ceramic Capacitors
- Available in a SOT563 Package
- ±1% Tolerance Voltage Reference at 25°C

Applications

- Wireless/Networking Cards
- Portable and Mobile Device
- Battery-Powered Device
- Low-Voltage I/O System Power
- Solid-State Drives (SSDs)

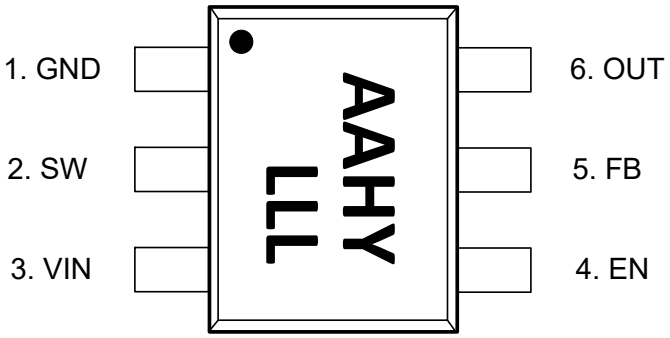
Typical Application



Package Mark and Order Information

Device	Package	Temperature range	Packaging Type	Purchase Contact
LA1163S	SOT563	-40 to 125 °C	T/R 5000pcs/roll	sales@latticeart.com

Pin Diagram

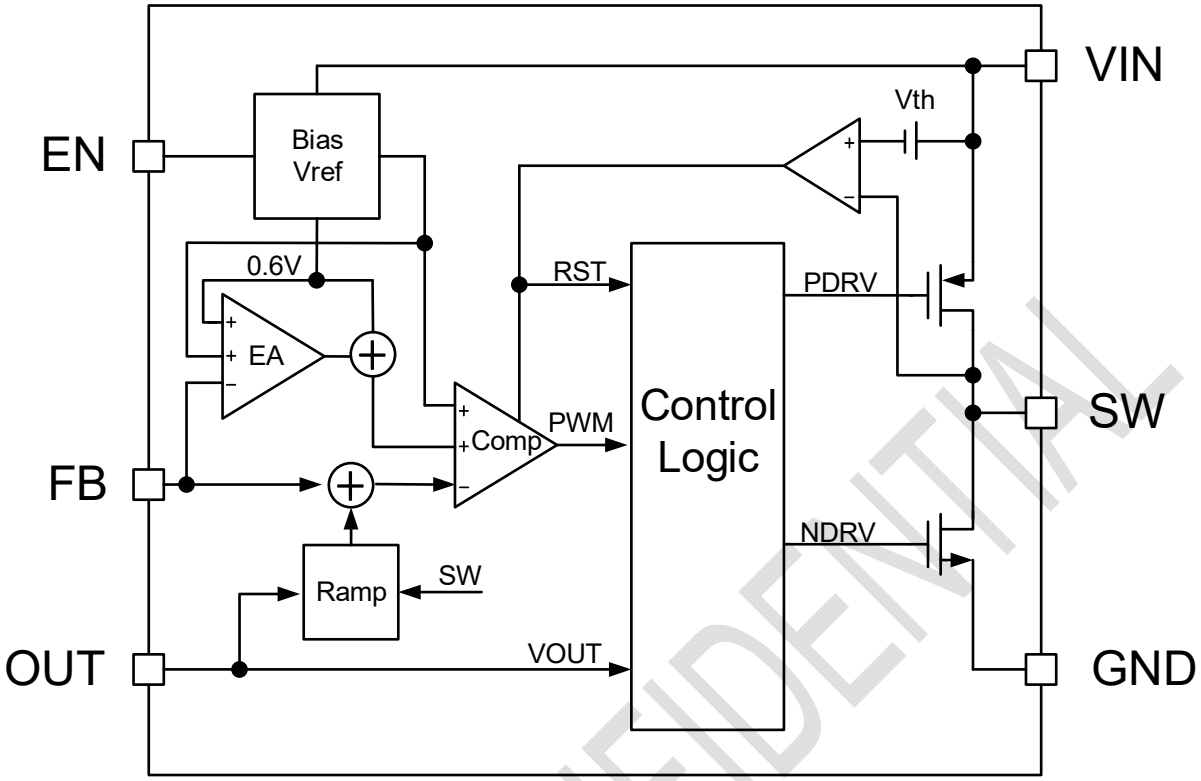


AAH: Product code of LA1163S
Y: Year code
LLL: Lot Number

Pin Description

Pin No.	Symbol	Pin Description
1	GND	**Power Ground terminal.**
2	SW	**Output switching node.** SW is the drain of the internal, high-side, P-channel MOSFET. Connect the inductor to SW to complete the converter.
3	VIN	**Supply voltage.** The LA1163S operates from a 2.3V to 5.5V unregulated input. A decoupling capacitor is needed to prevent large voltage spikes from appearing at the input.
4	EN	**On/off control.**
5	FB	**Feedback input to the convertor**. Connect a resistor divider to set the output voltage. Never short this terminal to ground during operation.
6	OUT	**Output voltage power rail and input sense pin for the output voltage.** Connect the load to OUT. An output capacitor is needed to decrease the output voltage ripple

BLOCK DIAGRAM



Absolute Maximum Ratings (note 1)

T_A=25^{0}C, unless otherwise specified.

Symbol	Definition	Ratings	Unit
VIN	VIN to GND	-0.3~6.5	V
V_{SW_DC}	V_{SW} to GND	-0.3~6.5	V
V_{SW_10ns}	V_{SW} to GND	-5~10	V
All other pins		-0.3~6.5	V
T_{STG}	Storage temperature	-65 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are not tested at manufacturing.

Recommended Operating Conditions

Symbol	Definition	Ratings	Unit
OUT	Out voltage to GND	0.6~5.5	V
GND	IC ground.	0	V
FB	FB to GND	0~1	V
EN	EN to GND	2~5	V
VIN	VIN to GND	2.3~5.5	V
SW	SW to GND	-0.7~5.5	V
I_{OUT}	Maximum Output Current	3	A
T_j	Junction temperature	-40 to +125	°C

Thermal Resistance

Symbol	Definition	Ratings	Unit
$\mathbf{R}_{\theta JC}$	Junction to case thermal resistance	60	°C/W
$\mathbf{R}_{\theta JA}$	Junction to ambient thermal resistance	130	°C/W

Electrical Characteristics

V_{IN}=3.6V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Control Part

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{FB}	Feedback voltage	2.3V ≤ VIN ≤ 5.5V	0.594	0.6	0.606	V
		T_J = -40°C to +125°C	0.591		0.609	
I_{FB}	Feedback current			50	100	nA
R_{ON_Pmos}	High-side switch on resistance			65		mΩ
R_{ON_Nmos}	Low-side switch on resistance			35		mΩ
LKG	Switch leakage current	V_{EN} = 0V		0	1	μA
VIN_{UVU}	VIN UVLO Up threshold			2.3	2.45	V
VIN_{UV_Hys}	VIN UVLO hysteresis			200		mV
I_{LIM_Pmos}	PMOS peak Current limit		4		6	A
I_{LIM_Nmos}	NMOS valley Current limit			3.5		A
I_{ZCD}	Zero current detection			50		mA
T_{ON}(2)	On time	VIN=5V,V_O=1.2V	180	220	260	ns
		VIN=3.6V,V_O=1.2V	240	300	360	ns
T_{SS}	Soft-start time	FB from 10% to 90%		0.5		ms
f_{SW}	Oscillator frequency	VIN = 5V, V_{OUT} = 1.2V, I_{OUT} = 500mA,		1100		KHz
T_{ON_MIN}(2)	Minimum switch on time			60		ns
T_{OFF_MIN}(2)	Minimum switch off time			100		ns
R_{dis}	Output discharge resistor	V_{EN}=0V V_{OUT}=1.2V		200		Ω
I_Q	Quiescent supply current	V_{EN}=2V, V_{FB}=0.63V, VIN=5V		25	30	μA
Isd	Shutdown current	V_{EN}=0V		0	1	μA

Electrical Characteristics

V_{IN}=3.6V, V_{EN}=2V, T_A=25°C, unless otherwise specified.

Control Part

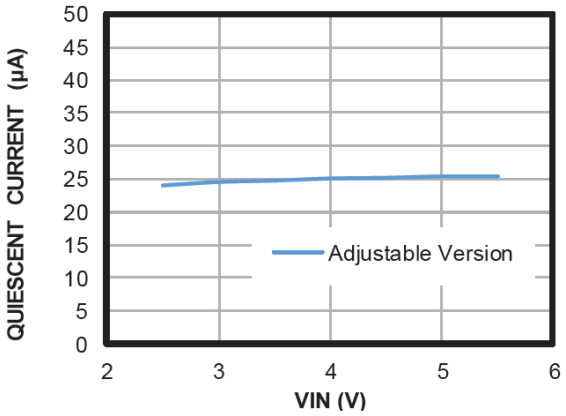
Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{O_OVP}	Output Over-voltage threshold		110%	115%	120%	V_{FB}
V_{OUT_HYS}				10%		V_{FB}
t_{OV_DELAY}	OVP delay			12		μs
NOCP	Low-side negative current limit	Current flow from SW to GND		1.5		A
V_{IN_OVP}	Absolute VIN OVP	VOUT OV triggered		6.1		V
$V_{IN\_OVP\_HYS}$	Input OVP hysteresis			400		mV
t_{EN_DELAY}				150		μs
V_{EN_R}	Enable rising threshold	Low to high	1.2			V
V_{EN_F}	Enable falling threshold	High to low			0.4	V
$V_{EN\_Leakage}$	V_{EN}=2V			1.2		μA
	V_{EN}=0V			0		μA
T_{OTP_R}(2)	Thermal shutdown			160		°C
T_{OTP_Hys}(2)	Thermal hysteresis			30		°C

NOTE 2: Guaranteed by design and engineering sample characterization.

Typical Performance Characteristic

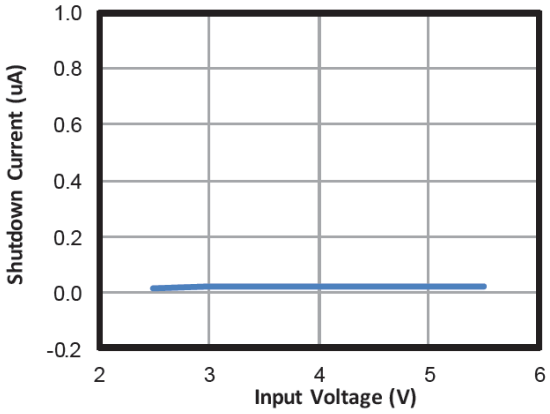
V_{OUT}=1.2V: V_{IN} = 5V, C_{OUT} = 22μF, L1 = 1.0μH, and T_A = +25°C, unless otherwise noted.

Quiescent Current vs. VIN

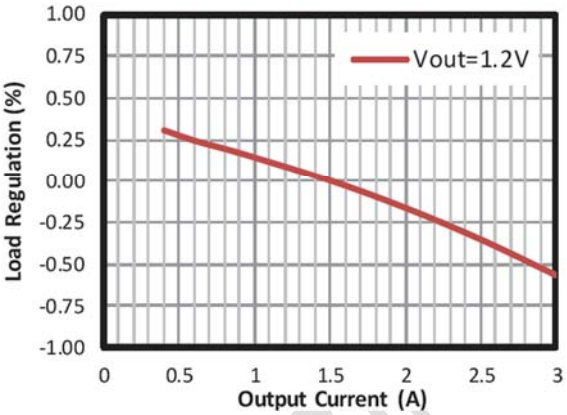


Shutdown Current vs. Input Voltage

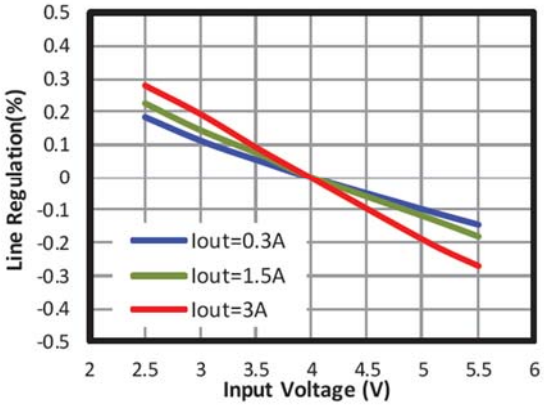
V_{EN} = 0V



Load Regulation

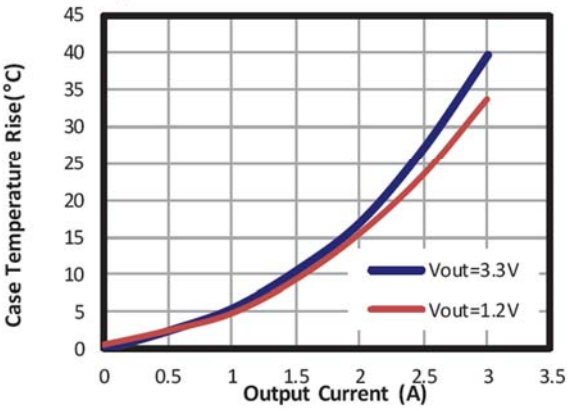


Line Regulation



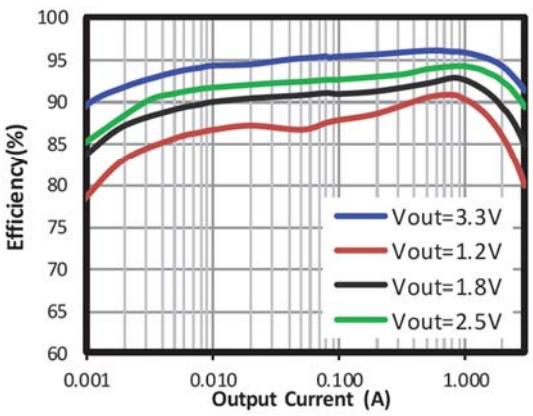
Case Temperature Rising vs. Output Current

V_{IN} = 5V



Efficiency vs. Output Current

V_{IN} = 5V

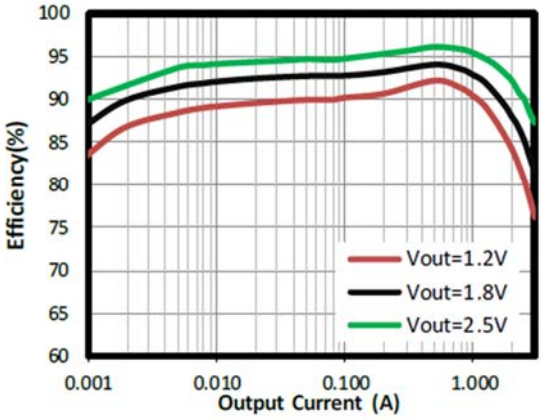


Typical Performance Characteristic

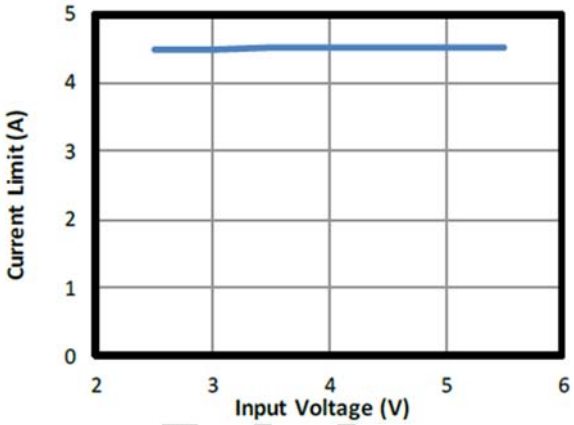
V_{OUT}=1.2V: V_{IN} = 5V, C_{OUT} = 22μF, L1 = 1.0μH, and T_A = +25°C, unless otherwise noted.

Efficiency vs. Output Current

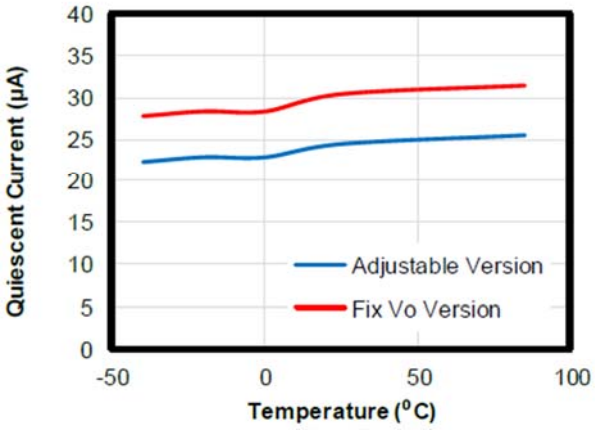
V_{IN} = 3.6V



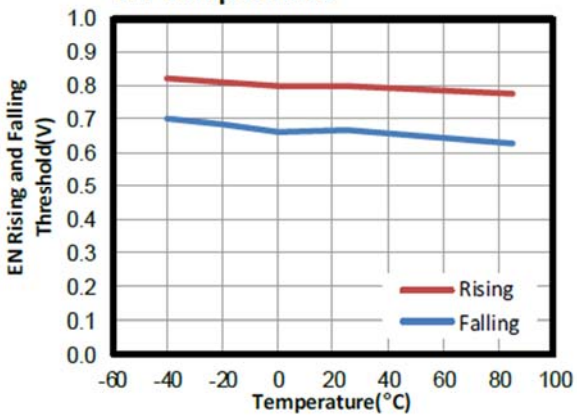
Peak Current Limit vs. V_{IN}



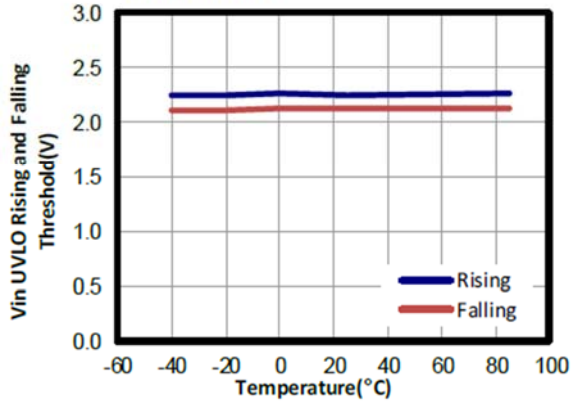
Quiescent Current vs. Temperature



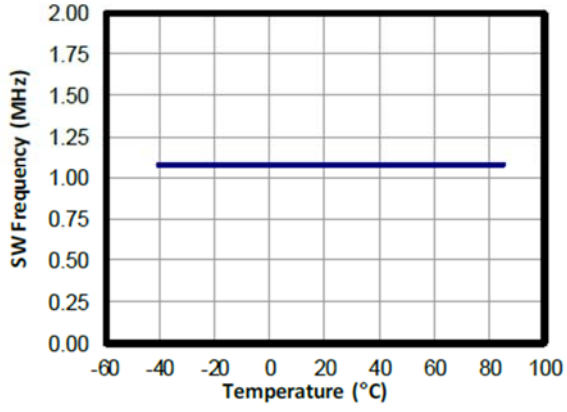
EN Rising and Falling Threshold vs. Temperature



V_{IN} Rising and Falling Threshold vs. Temperature



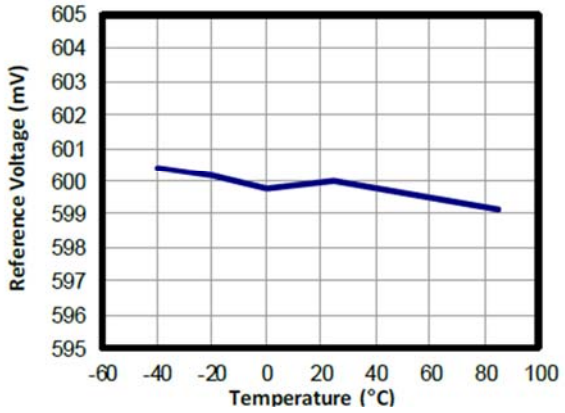
Switch Frequency vs. Temperature



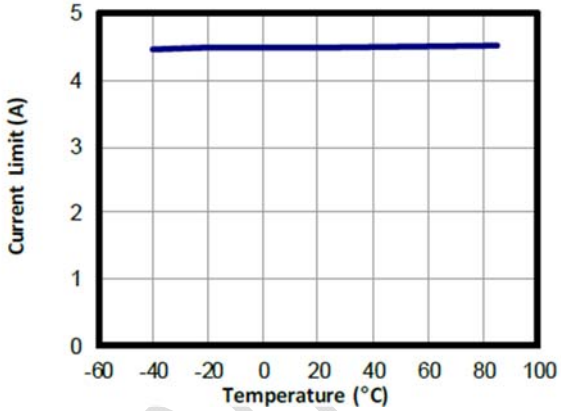
Typical Performance Characteristic

V_{OUT}=1.2V: V_{IN} = 5V, C_{OUT} = 22μF, L1 = 1.0μH, and T_A = +25°C, unless otherwise noted.

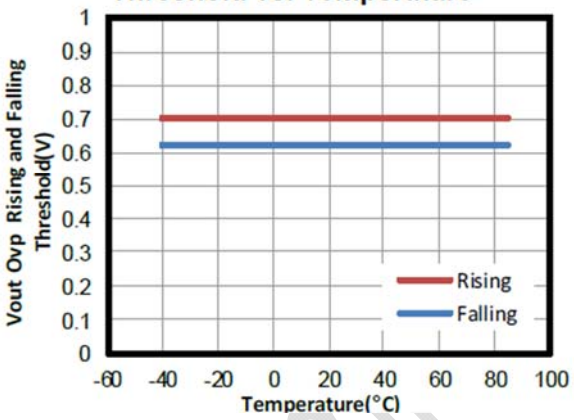
Reference Voltage vs. Temperature



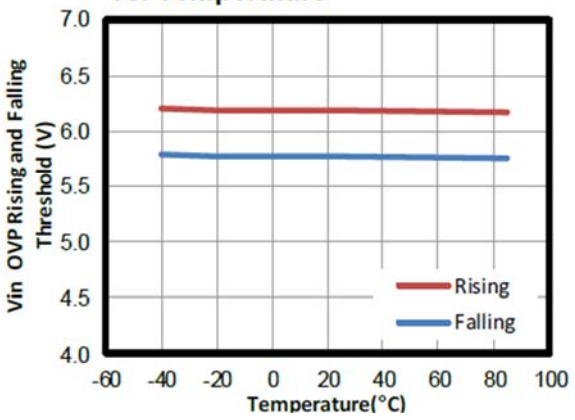
Peak Current Limit vs. Temperature



V_{OUT} OVP Rising and Falling Threshold vs. Temperature

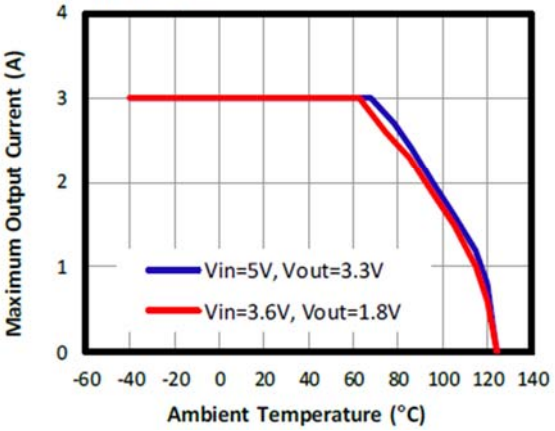


V_{IN} OVP Rising and Falling Threshold vs. Temperature



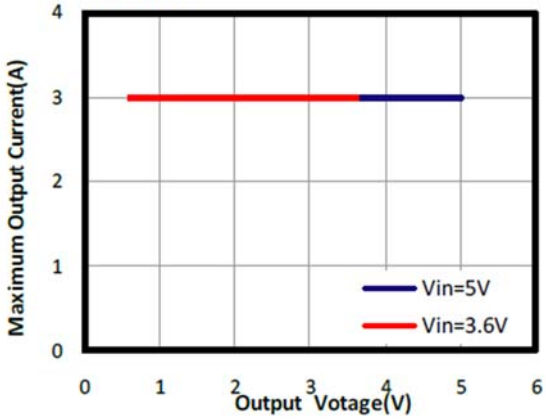
Output Current Derating vs. Ambient Temperature

$T_J \leq 125°C$



Output Current Derating vs. Output Voltage

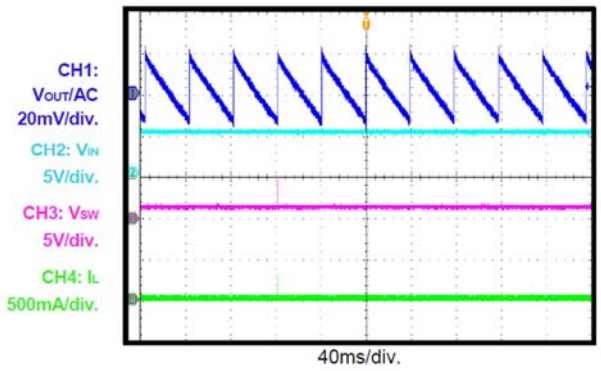
$T_J \leq 125°C$



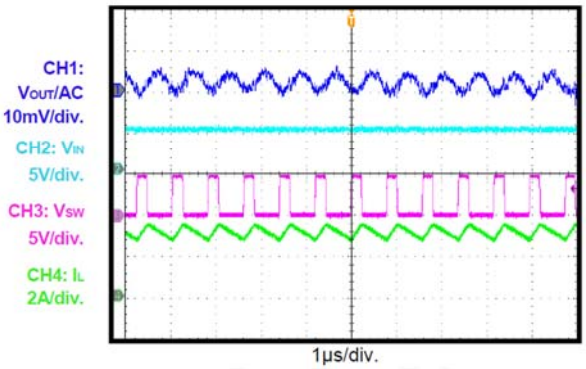
Typical Performance Characteristic

V_{OUT}=1.2V: V_{IN} = 5V, C_{OUT} = 22μF, L1 = 1.0μH, and T_A = +25°C, unless otherwise noted.

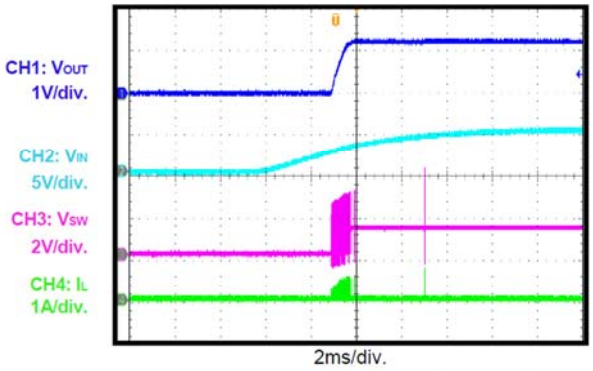
Steady State
I_{OUT}=0A



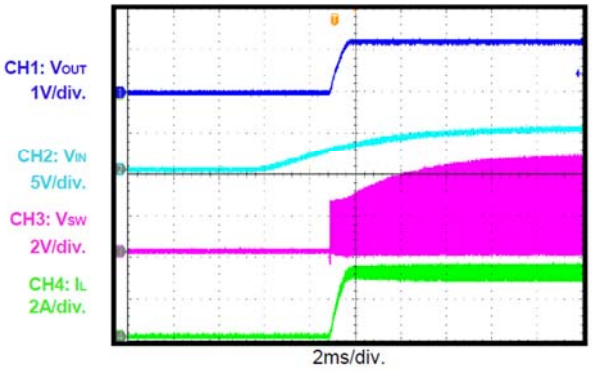
Steady State
I_{OUT}=3A



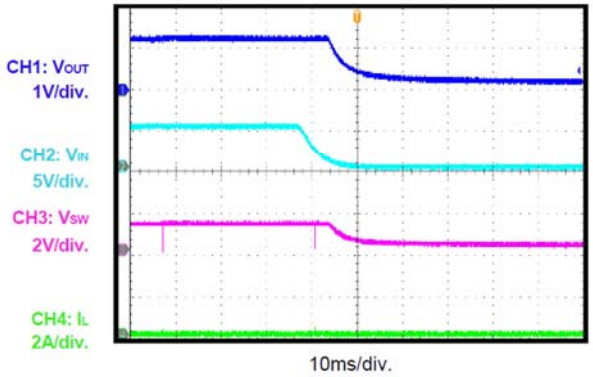
VIN Power-Up
I_{OUT}=0A



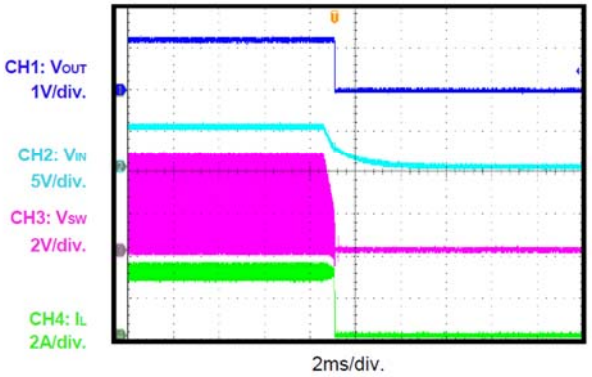
VIN Power-Up
I_{OUT}=3A



VIN Shutdown
I_{OUT}=0A



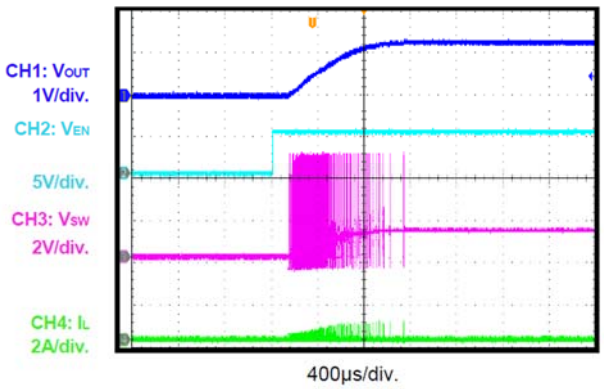
VIN Shutdown
I_{OUT}=3A



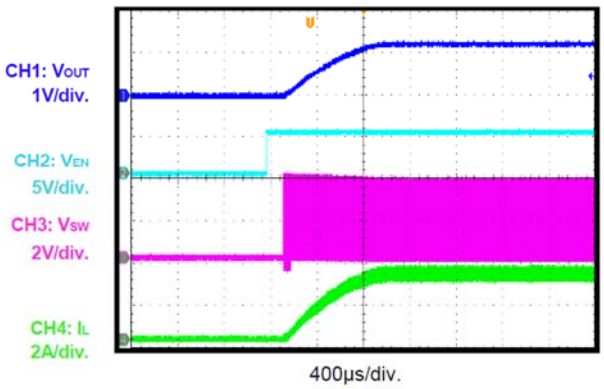
Typical Performance Characteristic

V_{OUT}=1.2V: V_{IN} = 5V, C_{OUT} = 22μF, L1 = 1.0μH, and T_A = +25°C, unless otherwise noted.

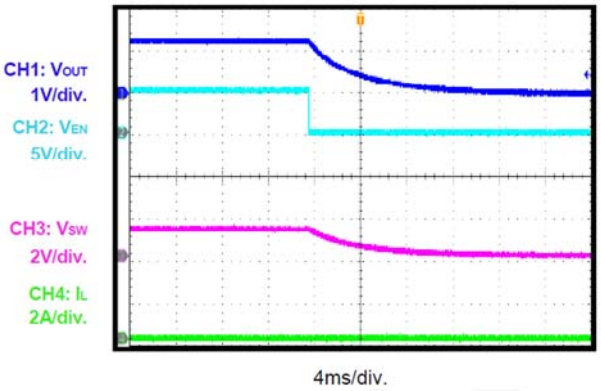
EN Power-Up
I_{OUT}=0A



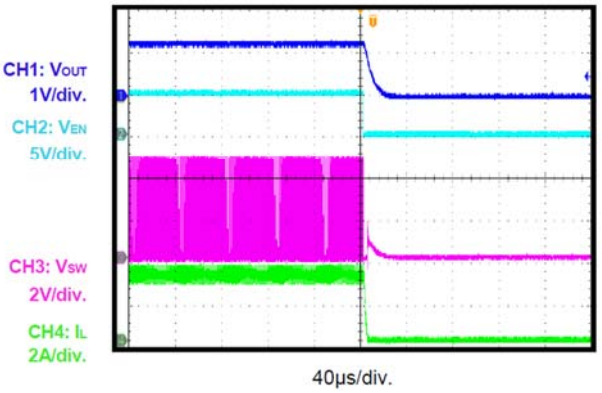
EN Power-Up
I_{OUT}=3A



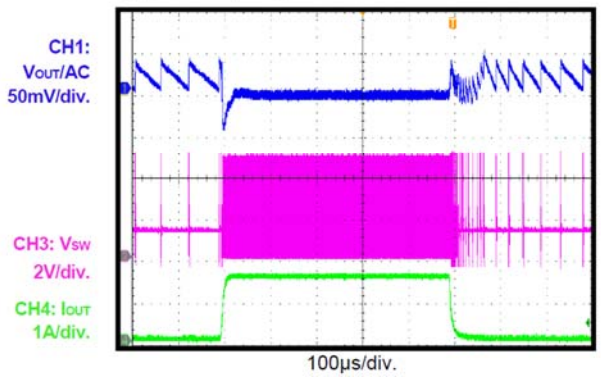
EN Shutdown
I_{OUT}=0A



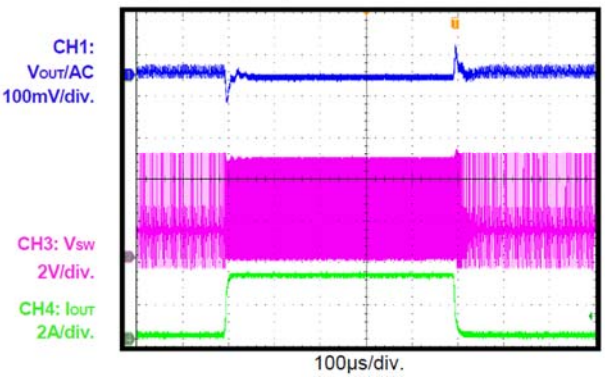
EN Shutdown
I_{OUT}=3A



Load Transient
I_{OUT}=0-1.5A, 1A/μs



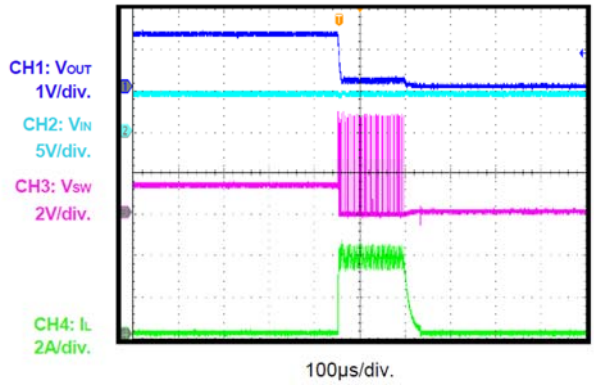
Load Transient
I_{OUT}=0.1-3A, 1A/μs



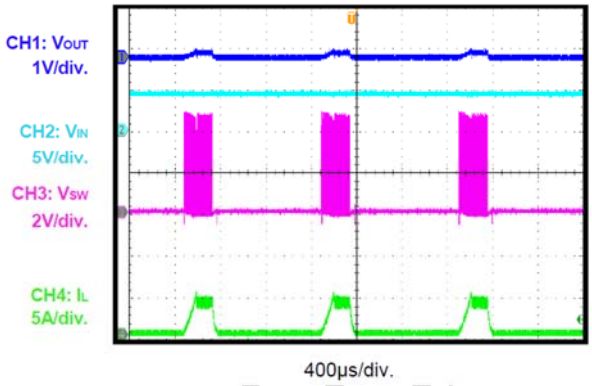
Typical Performance Characteristic

V_{OUT}=1.2V: V_{IN} = 5V, C_{OUT} = 22μF, L1 = 1.0μH, and T_A = +25°C, unless otherwise noted.

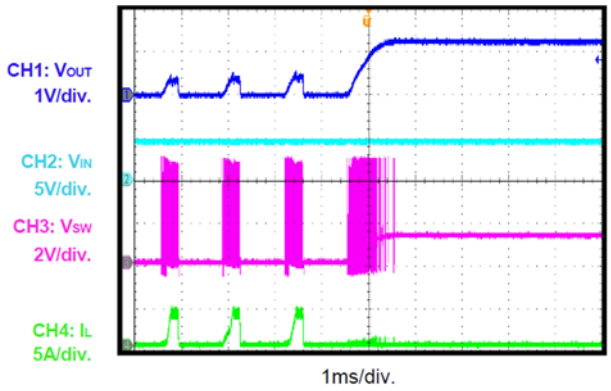
Short-Circuit Entry



Short-Circuit State



Short-Circuit Recovery



Function Descriptions

1. COT(Constant on time) Control

Compared to fixed-frequency pulse-width modulation (PWM) control. COT control offers a simpler control loop and a faster transient response. By using input voltage feed-forward, the LA1163S maintains a nearly constant switching frequency across the input and output voltage ranges. The switching pulse on time can be estimated with Equation (1):

$$T_{ON} = \frac{V_O}{V_{IN}} * 0.91 \ \mu s \quad \text{.....} \quad (1)$$

To prevent inductor current runaway during the load transient, the LA1163S uses a fixed minimum off time of 100ns.

2. Sleep Mode Operation

The LA1163S features sleep mode to achieve high efficiency at extreme light-load. In sleep mode, most of the circuit blocks are turned off except for the error amplifier and PWM comparator. The operation current is reduced to a minimal value.

When the load becomes lighter, the ripple of the output voltage becomes larger and drives the error amplifier output (EAO) lower. When the EAO reaches the internal low threshold, it is clamped at that level, and the LA1163S enters sleep mode. During sleep mode, the valley of the FB voltage is regulated to the internal reference voltage. Therefore, the average output voltage is slightly higher than the output voltage in DCM or CCM. The on-time pulse in sleep mode is around 40% larger than that in DCM or CCM.

When the LA1163S is in sleep mode, the average output voltage is higher than the internal reference voltage. The EAO is kept low and clamped in sleep mode. When the load increases, the PWM switching period decreases to keep the output voltage regulated, and the output voltage ripple decreases relatively. Once the EAO is higher than the internal low threshold, the LA1163S exits sleep mode and enters DCM or CCM depending on the load. In DCM or CCM, the error amplifier (EA) regulates the average output voltage to the internal reference.

There is always a loading hysteresis when entering and exiting sleep mode due to the EA clamping response time.

3. LPM Operation at Light-Load

The LA1163S uses advanced LPM power-save mode with zero-current cross detection (ZCD) circuit for light load.

The LA1163S uses LPM power-save mode for light load. The LPM current (ILPM) is set internally. The SW on pulse time is determined by the on-time generator and LPM comparator. At light-load condition, the SW on pulse time is longer. If the LPM comparator pulse is longer than the on-time generator, the operation mode.
The LPM circuit has another 150ns of LPM blank time in sleep mode. If the on-timer is less than 150ns, the high-side MOSFET may turn off after the on-time generator pulse without LPM control. The on-time pulse at sleep mode is about 40% larger than in DCM or CCM. In this condition, IL may not reach the LPM threshold. The LPM threshold

decreases as TON increases (Figure 1). For CCM state, IOUT requires more than half of the LPM threshold.

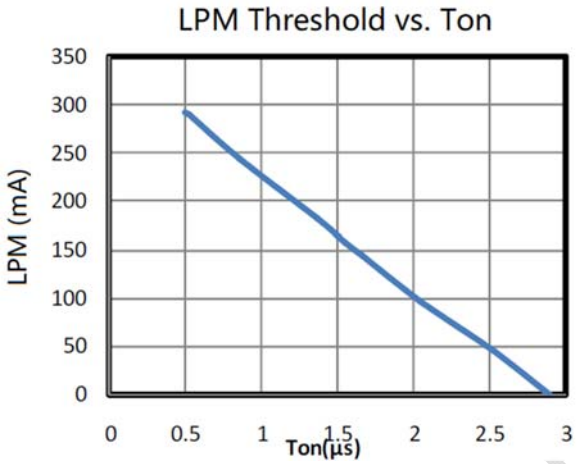


Figure 1 LPM Threshold Decrease vs. Ton Increase

The LA1163S uses a zero-current cross detect circuit (ZCD) to determine when the inductor current begins reversing. When the inductor current reaches the ZCD threshold, the low-side switch is turned off.

LPM mode with the ZCD circuit makes the LA1163S work continuously in DCM at light load, even if VOUT is close to VIN.

4. Enable (EN) Control

The LA1163S has a dedicated enable control pin EN. With high enough VIN, the chip can be enabled and disabled by EN pin. This is a HIGH effective logic. Its rising threshold is 1.2V typically and its failing threshold is about 300mV lower.

When floating, EN pin is internally pulled down to GND so the chip is disabled. There is an internal about 1.6MΩ resistor from EN to ground. When EN is pulled down to 0V, the chip is put into the lowest shutdown current mode. When EN is higher than zero but lower than its rising threshold, the chip is still in shutdown mode but the shutdown current increases slightly.

5. Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The LA1163S UVLO comparator monitors the input voltage. The UVLO rising threshold is about 2.3V, while its falling threshold is consistently 2.1V.

6. Current Limit

The LA1163S has a 6A max high-side, switch current limit, typically. When the high-side switch reaches its current limit, the LA1163S remains in hiccup mode until the current drops. This prevents the inductor current from continuing to rise and damaging components.

7. Short circuit protection (SCP)

The LA1163S enters short-circuit protection (SCP) mode when it reaches the current limit

and attempts to recover with hiccup mode. In this process, the LA1163S disables the output power stage, discharges the soft-start capacitor, and then attempts to soft start automatically. If the short-circuit condition remains after the soft start ends, the LA1163S repeats this cycle until the short circuit disappears and the output rises back to regulation levels.

8. Over-Voltage Protection (V_{OUT} OVP)

The LA1163S monitors the feedback voltage to detect over-voltage. When the feedback voltage becomes higher than 115% of the target voltage, the controller enters a dynamic regulation period. During this period, the low side turns on until the low-side current drops to -1.5A. This discharges the output to keep it within the normal range. If the over-voltage condition still remains, the low side turns on again after a 1μs delay. The LA1163S exits this regulation period when the feedback voltage decreases below 105% of the reference voltage. If the dynamic regulation cannot limit the increasing VOUT, once the input detects the 6.1V input, over-voltage protection (OVP)occurs, the LA1163S stops switching until the input voltage drops below 5.7V, and then the LA1163S resumes operation

9. Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the entire chip shuts down. When the temperature falls below its lower threshold (typically 130°C), the chip is enabled again.

Application Information

1. Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application on page 2). Select the feedback resistor (R1) to reduce the VOUT leakage current, typically between 100kΩ to 200kΩ. There is no strict requirement on the feedback resistor. R1 > 10kΩ is reasonable for the application. R2 can then be calculated with Equation (2):

$$R_2 = \frac{R_1}{\left({}^{V_{OUT}}/_{0.6}\right)-1} \quad \text{.....} \quad (2)$$

Table 1 lists the recommended resistor values for common output voltages.

V_{OUT} (V)	R1 (KΩ)	R2 (KΩ)
1.0	200	300
1.2	200	200
1.8	200	100
2.5	200	63.2
3.3	200	44.2

Table 1: Resistor Values for Common Output Voltages

2. Selecting the Inductor

Most applications work best with a 0.47μH to 2.2μH inductor. Select an inductor with a DC resistance less than 50mΩ to optimize efficiency. High-frequency, switch-mode power supplies with a magnetic device have strong electronic magnetic inference for the system. Any unshielded power inductor should be avoided since it has poor magnetic shielding. Metal alloy or multiplayer chip power shield inductors are recommended for the application since they can decrease influence effectively.

Table 2 lists some recommended inductors.

Manufacturer P/N	Inductance (μH)	Manufacturer
PIFE25201B-1R0MS	1.0	CYNTEC CO.LTD.
74437324010	1.0	Wurth

Table 2: Suggested Inductor List

For most designs, the inductance can be estimated with Equation (3)

$$L_1 = \frac{V_{OUT}(V_{IN}-V_{OUT})}{V_{IN}\Delta I_L f_{osc}} \text{ ..... } (3)$$

Where ΔI_L is the inductor ripple current. Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (4):

$$I_{L\ (MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad \text{.....} \quad (4)$$

3. Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. Higher output voltages may require a 22μF capacitor to increase system stability. The input capacitor requires an adequate ripple current rating since it absorbs the input switching current. Estimate the RMS current in the input capacitor with Equation (5):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad \text{.....} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current. The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality, 0.1μF, ceramic capacitor as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{F_{OSC}C_1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{.....} \quad (6)$$

4. Selecting the Output Capacitor

The output capacitor (C2) stabilizes the DC output voltage. Low ESR ceramic capacitors are recommended to limit the output voltage ripple. Estimate the output voltage ripple with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC}L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(ESR + \frac{1}{8F_{OSC}C_2}\right) \quad \text{.....} \quad (7)$$

Where L1 is the inductor value, and RESR is the equivalent series resistance (ESR) value of the output capacitor. When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8F_{OSC}^2 L_1 C_2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{.....} \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{OSC}L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times ESR \quad \text{.....} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system.

5. PCB Layout Guidelines

Efficient layout of the switching power supplies is critical for stable operation. For the high frequency switching converter, poor layout design can result in poor line or load regulation and stability issues. For best results, refer to Figure 1 and follow the guidelines below.

- Place the high-current paths (GND, VIN and SW) as close to the device as possible with short, direct, and wide traces.
- Place the input capacitor as close to VIN and GND as possible.
- Place the external feedback resistors next to FB.

- Keep the switching node (SW) short and away from the feedback network.
- Keep the VOUT sense line as short as possible or away the from power inductor and surrounding inductors.

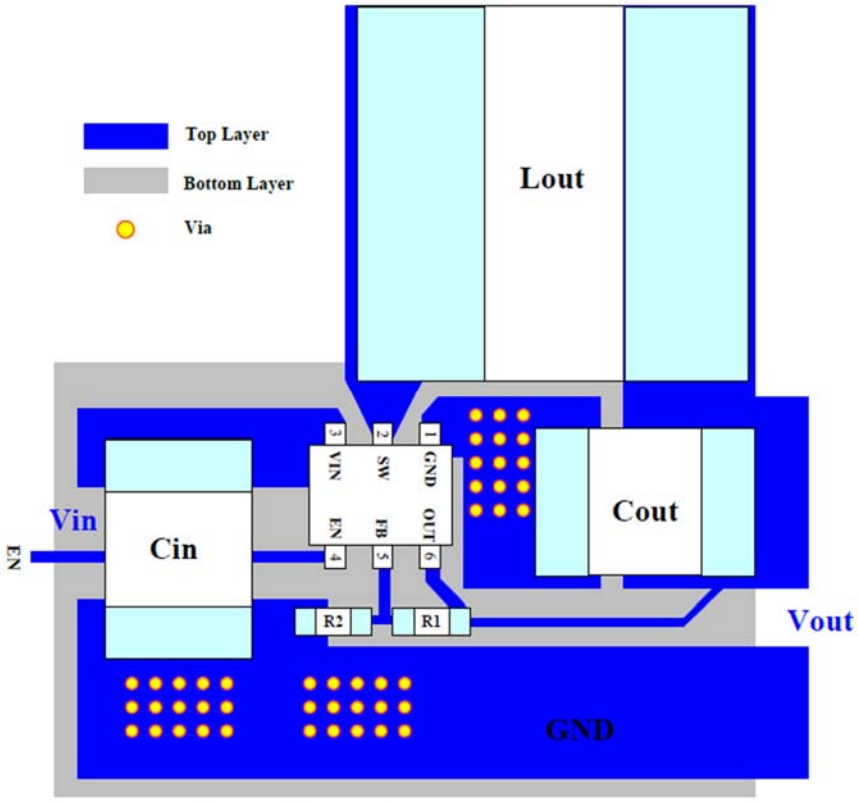
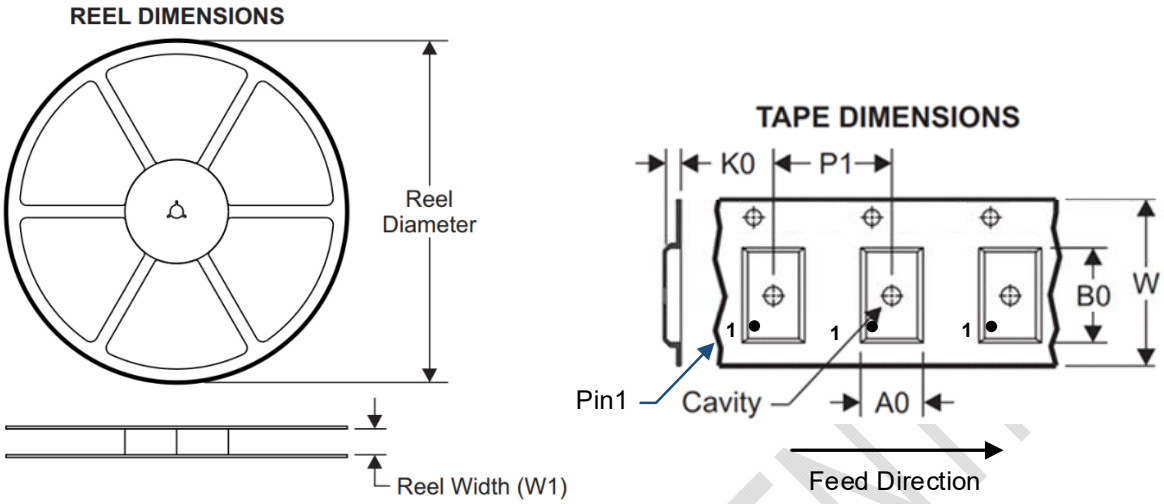


Figure 1: Two Ends of Input Decoupling Capacitor Close to Pin 2 and Pin 3

Tape and Reel Information

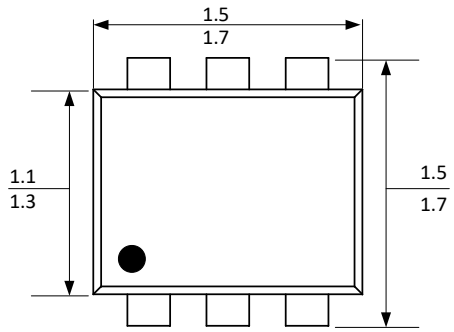


Information

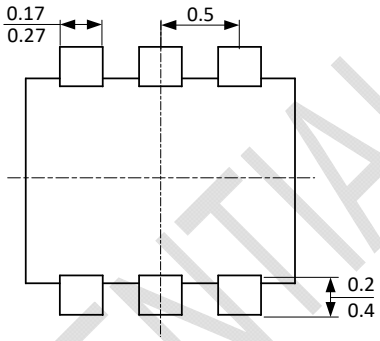
Device	Package Type	Pins	SPQ	Real Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
LA1163S	SOT563	6	5000	150	8.6	1.80	1.83	0.75	4	8

Detail Package Outline Drawing

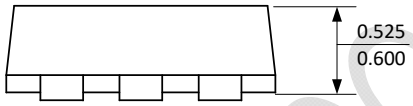
Package type: SOT563



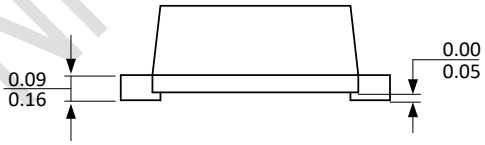
TOP VIEW



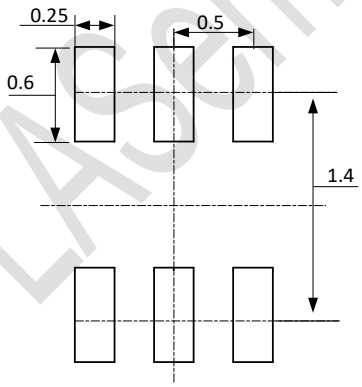
BOTTOM VIEW



FRONT VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1. ALL DIMENSIONS ARE IN MILLMETERS
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4. LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLMETERS MAX.
5. DRAWING IS NOT TO SCALE.