ANALOG DEVICES

12-Bit, 10 MSPS A/D Converter

AD9007

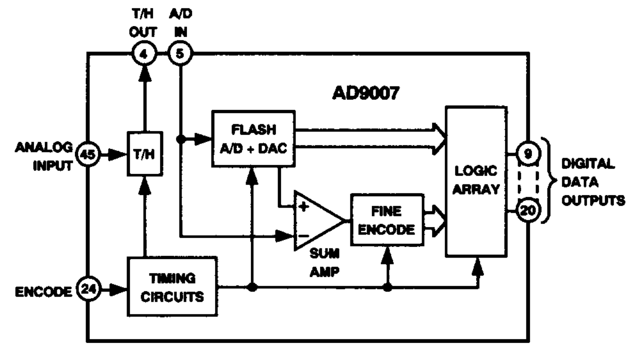
FEATURES

Complete 12-Bit A/D Converter
Includes Track and Hold, Reference, and Timing
Bipolar Analog Input (±1.25 V)
Up to 10 MSPS Sampling Rate
Dual Supply: +5 V, −5.2 V Only
Tristate Outputs

APPLICATIONS

Radar
Digital Receivers
Electro-Optics
Medical Scanners
Signal Intelligence
Spectrum Analyzers

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9007 is a complete 12-bit A/D converter which includes on-board track-and-hold amplifier, voltage reference, and timing circuits. Featuring sampling rates from dc to 10 MSPS, the AD9007 uses a subranging converter architecture to achieve high speed and high resolution. Vertical integration of advanced monolithic components allows the AD9007 to operate on only +5 V and −5.2 V supplies.

The AD9007 is a functional replacement for the Burr-Brown ADC603 (12 bits @ 10 MSPS) and the ADC604 (12 bits @ 5 MSPS). The AD9007 will fit existing sockets for those parts in many applications, but the user needs to be aware of the differences between the AD9007 and the Burr-Brown parts.

Critical to the performance of the AD9007 is the use of advanced bipolar integrated circuits, custom designed for this device and manufactured by Analog Devices. The AD9007 is TTL-compatible, with 2s complement outputs. It is available in a 46-pin hermetic metal DIP in a −25°C to +85°C industrial range (case temperature).

REV. 0

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AD9007—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (+V_S = +5 V, −V_S = −5.2 V, unless otherwise stated)

Parameter	Temp	Test Level	AD9007AM Min	AD9007AM Typ	AD9007AM Max	AD9007BM Min	AD9007BM Typ	AD9007BM Max	Units
RESOLUTION	+25°C	I	12			12			Bits
LSB Weight	Full	V		0.61			0.61		mV
STATIC ACCURACY									
Differential Nonlinearity	Full	VI	−1.0	±0.75	+1.0	−1.0	±0.75	+1.0	LSB
Integral Nonlinearity	+25°C	V		±1.5			±1.5		LSB
	Full	V		±2.0			±2.0		LSB
No Missing Codes	Full	VI		GUARANTEED			GUARANTEED		
Gain Error	+25°C	I		±0.5	±3.0		±0.5	±3.0	% FS
	Full	VI			±3.5			±3.5	% FS
Offset Error	+25°C	I		±4	±15		±4	±15	mV
	Full	VI			±25			±25	mV
ANALOG INPUT									
Input Voltage Range	Full	V		±1.25			±1.25		V p-p
Input Resistance	Full	V		650			650		kΩ
Input Capacitance	+25°C	IV		7	10		7	10	pF
Analog Input Bandwidth[1]	Full	V		150			150		MHz
DYNAMIC CHARACTERISTICS[2]									
Maximum Conversion Rate	Full	I	10.24			10.24			MSPS
Output Data Delay[3, 4] (t_{PD})	+25°C	V		90			90		ns
Aperture Delay (t_A)	+25°C	V		10			10		ns
Aperture Uncertainty (jitter)	+25°C	IV		10	20		10	20	ps rms
Transient Response[5] (to ±1 LSB)	+25°C	V		60			60		ns
Overvoltage Recovery Time[6] (to ±1 LSB)	+25°C	V		65			65		ns
Harmonic Distortion[7, 8]									
f_{IN} = 100 kHz	+25°C	IV	−74	−78		−80	−87		dBc
f_{IN} = 2.3 MHz	+25°C	I	−71	−76		−77	−82		dBc
	Full	VI	−70			−74			dBc
f_{IN} = 4.3 MHz	+25°C	I	−70	−72		−75	−78		dBc
	Full	VI	−68			−71			dBc
Signal-to-Noise Ratio[8, 9]									
f_{IN} = 100 kHz	+25°C	IV	65	67		67	70		dB
f_{IN} = 2.3 MHz	+25°C	I	64	67		66	69		dB
	Full	VI	63			64			dB
f_{IN} = 4.3 MHz	+25°C	I	63	64		65	68		dB
	Full	VI	61			62			dB
Two-Tone Intermodulation Distortion[10]									
f_{IN} = 2.2 MHz + 2.3 MHz	+25°C	V		−79			−81		dBc
DIGITAL INPUT[11]									
Logic "1" Voltage	Full	IV	2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8	V
Logic "1" Current	Full	I			150			150	μA
Logic "0" Current	Full	I			150			150	μA
Input Capacitance	+25°C	V		5			5		pF
Encode Pulse Width (High)	+25°C	IV	25			25			ns
DIGITAL OUTPUTS									
Logic "1" Voltage (2 mA Source)	Full	I	2.4			2.4			V
Logic "0" Voltage (4 mA Sink)	Full	I			0.4			0.4	V
Logic Coding	Full	IV		2s Complement			2s Complement		

Parameter	Temp	Test Level	AD9007AM Min	AD9007AM Typ	AD9007AM Max	AD9007BM Min	AD9007BM Typ	AD9007BM Max	Units
POWER SUPPLY									
Supply Voltage $+V_S$	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	V
Supply Current Analog $+V_S$	Full	VI		200	275		200	275	mA
Supply Current Digital $+V_S$	Full	VI		50	80		50	80	mA
Supply Voltage $-V_S$	Full	VI	−4.95	−5.2	−5.45	−4.95	−5.2	−5.45	V
Supply Current Analog $-V_S$	Full	VI		270	360		270	360	mA
Supply Current Digital $-V_S$	Full	VI		80	110		80	110	mA
Nominal Power Dissipation	Full	VI		3.0	3.9		3.0	3.9	W
PSRR[12, 13]	+25°C	I		0.01	0.02		0.01	0.02	

NOTES
[1]Determined by 3 dB reduction in reconstructed output.
[2]Measured at 10 MSPS encode rate.
[3]Measured from ENCODE into data out for LSB only.
[4]Excludes pipeline delay of two clock cycles (see timing diagram).
[5]For full-scale step input; 12-bit accuracy is attained in the specified time.
[6]Recovers to 12-bit accuracy in specified time following 200% full-scale input voltage.
[7]Worst case spurious in-band signal relative to input level.
[8]Input at 1 dB below full scale.
[9]RMS signal to rms noise, including harmonics.
[10]Worst case spurious signal relative to level of input tones, which are both −7 dB below full scale.
[11]ENCODE signal rise and fall times should be less than 5 ns for normal operation. Transition from "0" to "1" initiates conversion.
[12]Sensitivity of full-scale gain error with respect to power supply variation within supply Min/Max limits.
[13]PSRR is tested over given voltage range.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . +6 V
Negative Supply Voltage ($-V_S$) . . . . −6 V
Analog Input Voltage (Pin 45) . . . . ±3.0 V dc
Digital Input Voltage . . . . −0.5 V to $+V_S$
Digital Output Current . . . . 4 mA
Operating Temperature Range (Case)
AD9007AM/BM . . . . −25°C to +85°C
Storage Temperature Range . . . . −65°C to +150°C
Junction Temperature[2] . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . +300°C

NOTES
[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute rating conditions for extended periods of time may affect device reliability.
[2]Maximum junction temperature should not be allowed to exceed +175°C. Hybrid thermal model:
$T_{JUNCTION} = T_{AMBIENT} + P_{DISSIPATION} \times (\theta_{CA}) + (T_S - T_C)$ max
where $(T_S - T_C)$ max = 10°C
46-Pin metal DIP: θ_{CA} = 14°C/W in still air;
θ_{CA} = 6°C/W with 500 LFPM air flow

EXPLANATION OF TEST LEVELS

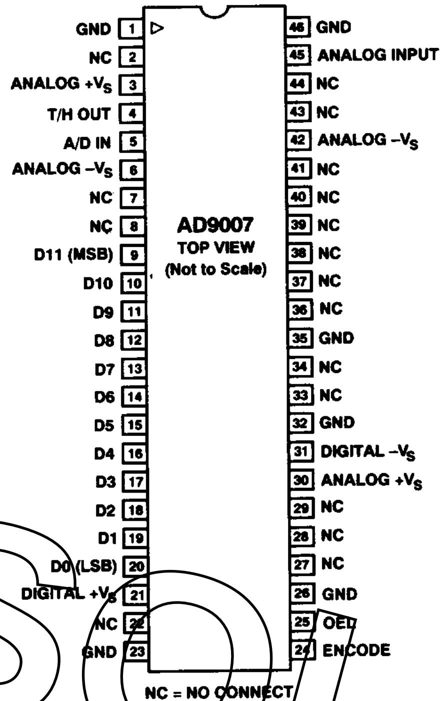
Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

ORDERING INFORMATION

Model	Temperature Range	Package Option
AD9007AM	−25°C to +85°C	46-Pin DIP, Industrial Temperature
AD9007BM	−25°C to +85°C	46-Pin DIP, Industrial Temperature

PIN CONFIGURATION



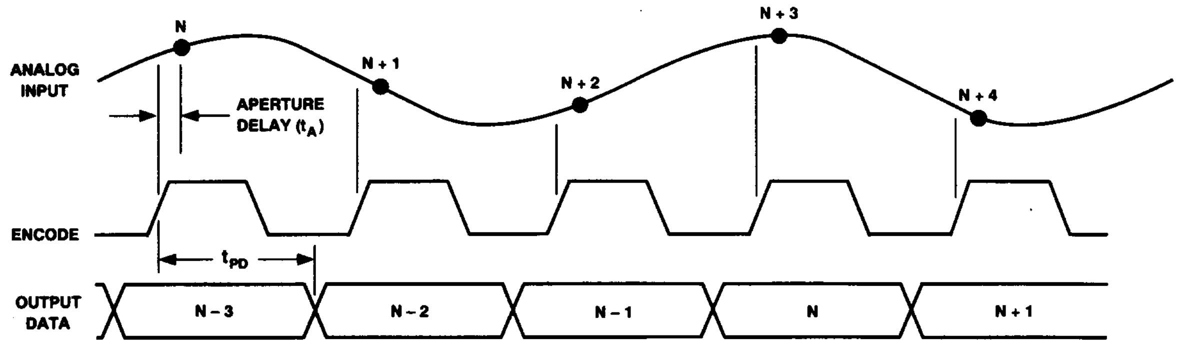
AD9007 PIN DESCRIPTIONS

Pin	Name	Description
1	GROUND	Circuit ground. All grounds should be connected together near the AD9007.
2	NC	Not internally connected.
3	ANALOG $+V_S$	Positive analog supply pin. Nominally +5 V dc.
4	T/H OUT	Output of internal track-and-hold amplifier. Connect to Pin 5 for normal operation.
5	A/D IN	Input to internal A/D encoder. Connect to Pin 4 for normal operation.
6	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2 V dc.
7, 8	NC	Not internally connected.
9	D_{11} (MSB)	Most significant bit of digital output data.
10–19	D_1–D_{10}	Digital data outputs.
20	D_0 (LSB)	Least significant bit of digital output data.

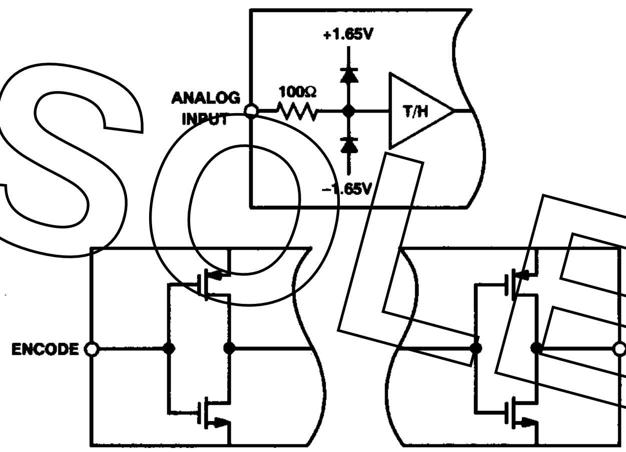
OUTPUT CODING

ANALOG INPUT	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
≥+1.25 V	0	1	1	1	1	1	1	1	1	1	1	1
≥−1.25 V	1	0	0	0	0	0	0	0	0	0	0	0

Pin	Name	Description
21	DIGITAL $+V_S$	Positive digital supply pin. Nominally +5 V dc.
22	NC	Not internally connected.
23	GROUND	Circuit ground. All grounds should be connected together near the AD9007.
24	ENCODE	Convert command. TTL compatible; rising edge triggered.
25	OEL	Output Enable Latch. Enables tristate outputs when active (LOW). Disables tristate D_0–D_{11} when HIGH.
26	GROUND	Circuit ground. All grounds should be connected together near the AD9007.
27–29	NC	Not internally connected.
30	ANALOG $+V_S$	Positive analog supply pin. Nominally +5 V dc.
31	DIGITAL $-V_S$	Negative digital supply pin. Nominally −5.2 V dc.
32	GROUND	Circuit ground. All grounds should be connected together.
33, 34	NC	Not internally connected.
35	GROUND	Circuit ground. All grounds should be connected together.
36–41	NC	Not internally connected.
42	ANALOG $-V_S$	Negative analog supply pin. Nominally −5.2 V dc.
43, 44	NC	Not internally connected.
45	ANALOG INPUT	Analog input. Full scale = ±1.25 V.
46	GROUND	Circuit ground. All grounds should be connected together near the AD9007.



Timing Diagram



Equivalent Input/Output Circuits

APPLICATIONS INFORMATION

The AD9007 is a complete analog-to-digital converter. It uses a subranging A/D architecture enhanced by hybrid technology. This includes an on-board track-and-hold (T/H) amplifier, on-board references, timing circuits, and output latches.

Analog input signals for the AD9007 are applied to the internal T/H, thereby eliminating the need for external signal conditioning for most applications. The T/H amplifier provides high input impedance and a bipolar (±1.25 V) analog input range.

If the amplitude, bandwidth, or dc voltage level of the analog input signal requires external signal conditioning, it is advisable to select an amplifier with low harmonic distortion and low noise characteristics, such as the Analog Devices AD9617 wideband , low noise feedback amplifier. The choice of the external amplifier is important for assuring optimum performance from the AD9007. It is also important to remember that band limiting the analog input signal can avoid aliasing during the A/D conversion process.

Timing in the AD9007 is critical, and careful techniques must be used to support the converter's 12-bit accuracy. One simple way to enhance performance of the AD9007 is to synchronize the system clock to a crystal oscillator. This will eliminate clock jitter, a must for maintaining the spectral purity of analog signals near the Nyquist limits. Since the conversion cycle begins with the rising edge of the ENCODE signal, a fast (≤5 ns rise time), "clean" rising edge also helps reduce clock jitter.

When the ENCODE signal applied to the AD9007 goes to a logic HIGH, the internal track-and-hold enters the "hold" state; after 65 ns, it return to the "track" mode. In applications in which the AD9007 is clocked slowly or intermittently (i.e., in burst mode), the encode signal should be returned to a logic LOW level during the idle periods.

The width of the ENCODE pulse should also be adjusted so it remains in the HIGH (hold) state for a minimum of 25 ns. This ensures that the T/H enters the hold mode before the A/D conversion takes place.

In many applications, the AD9007 can be used as a "drop in" replacement for the Burr-Brown ADC603 and ADC604 with little or no modification of the circuit. Unlike its counterparts, the AD9007 does not provide a data valid output signal; Pin 22 of the AD9007 is not connected. But the encode command can be used to latch output data.

Other functions such as logic invert (Pin 27), pipeline selection (Pins 28, 29), or gain (Pin 36) and offset (Pin 37) adjustment are not included on the AD9007. These pins are not electrically connected in the AD9007 converter.

Layout Information

The accuracy of a 12-bit converter, especially one with the dynamic performance level of the AD9007, requires that designers pay careful attention to printed circuit board layouts. Analog signal paths should be impedance matched, with termination/load resistors at or near package connections.

Analog signal paths should also be isolated from digital signal paths. If they are not, digital signals can be capacitively coupled into the analog section of the circuit, degrading the overall performance of the A/D converter.

Digital switching noise on power supplies can also degrade converter performance. Because of this noise (inherent with TTL logic), the digital power supplies of the AD9007 should be separated from the analog power supplies. In addition, each power supply should be capacitively coupled to ground. To accomplish this, a single large value capacitor with a high resonant frequency (a 10 μF tantalum capacitor, for example) should be used on each of the AD9007's power supplies, at or near the package. In addition, a lower value capacitor with good high frequency characteristics (a 0.1 μF ceramic chip capacitor is recommended) should be connected to each power supply pin connection.

Noise on the circuit ground is often the limiting factor in A/D converter performance. Perhaps the most critical concerns of circuit layout are the ground connections. To reduce ground noise, a two-sided printed circuit board is recommended, with the component side being reserved as much as possible for a single, low impedance ground plane. The other side should be used for all (possible) power and signal connections. Each of the ground connections of the AD9007 should be connected to the ground plane, and most of the area under the AD9007 should be part of this ground plane. The metal case of the AD9007 is connected to ground.

Operation of the AD9007 requires that Pin 4, the output of the internal track-and-hold, be connected to Pin 5, the input to the AD9007's A/D converter circuits.

A final suggestion regarding circuit layout concerns the use of sockets. Ideally, parts should be soldered into boards in final designs. If sockets must be used, individual pin sockets are recommended to avoid lead inductance, and capacitive coupling between adjacent pins. Pin sockets are available from Amp as Part #6-33808-0.

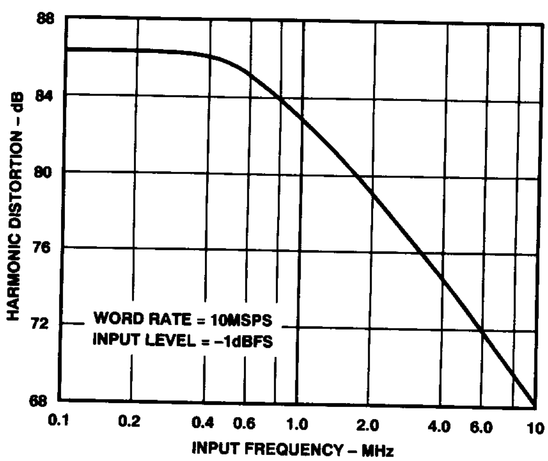


Figure 1. Harmonic Distortion vs. Analog Input

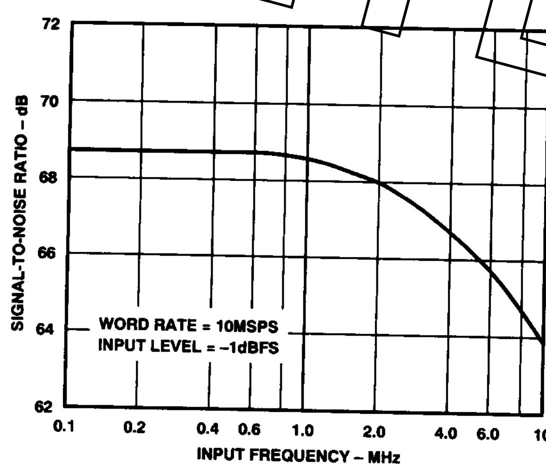


Figure 2. SNR vs. Analog Input

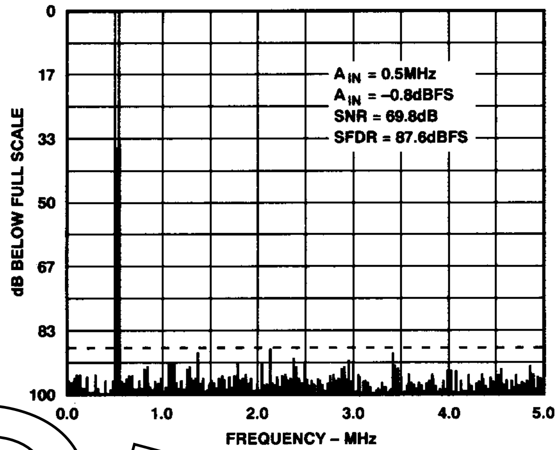


Figure 3. FFT

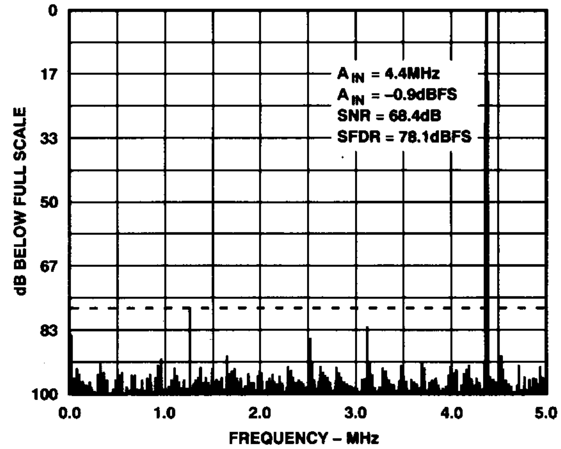


Figure 4. FFT

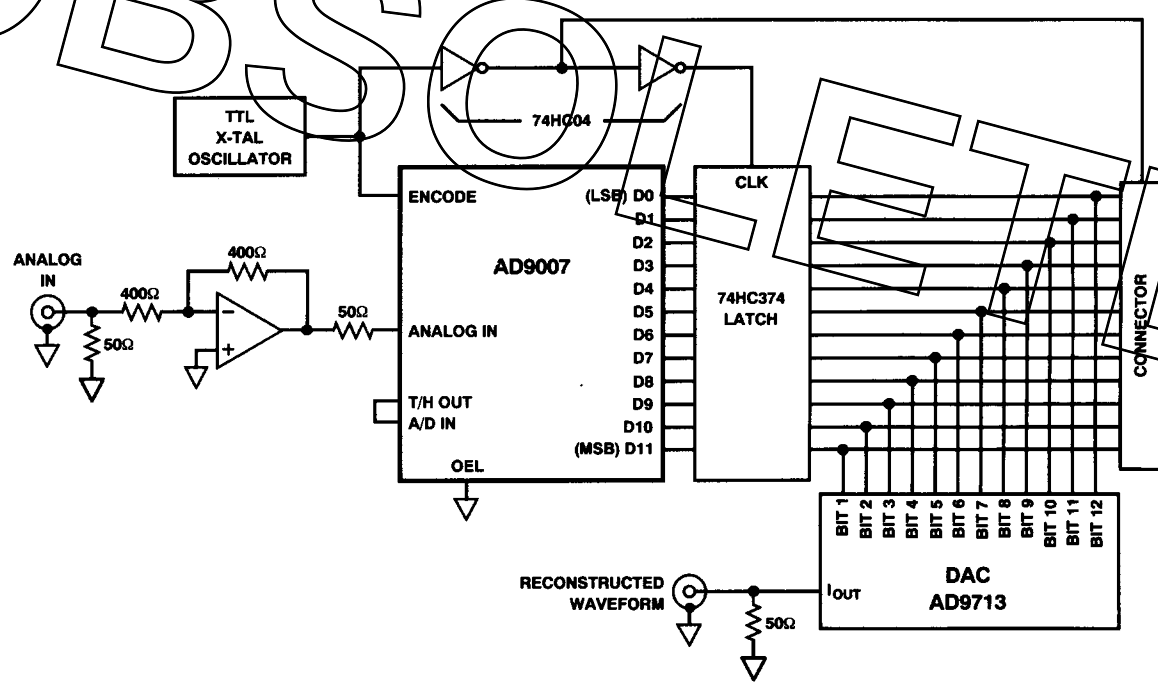
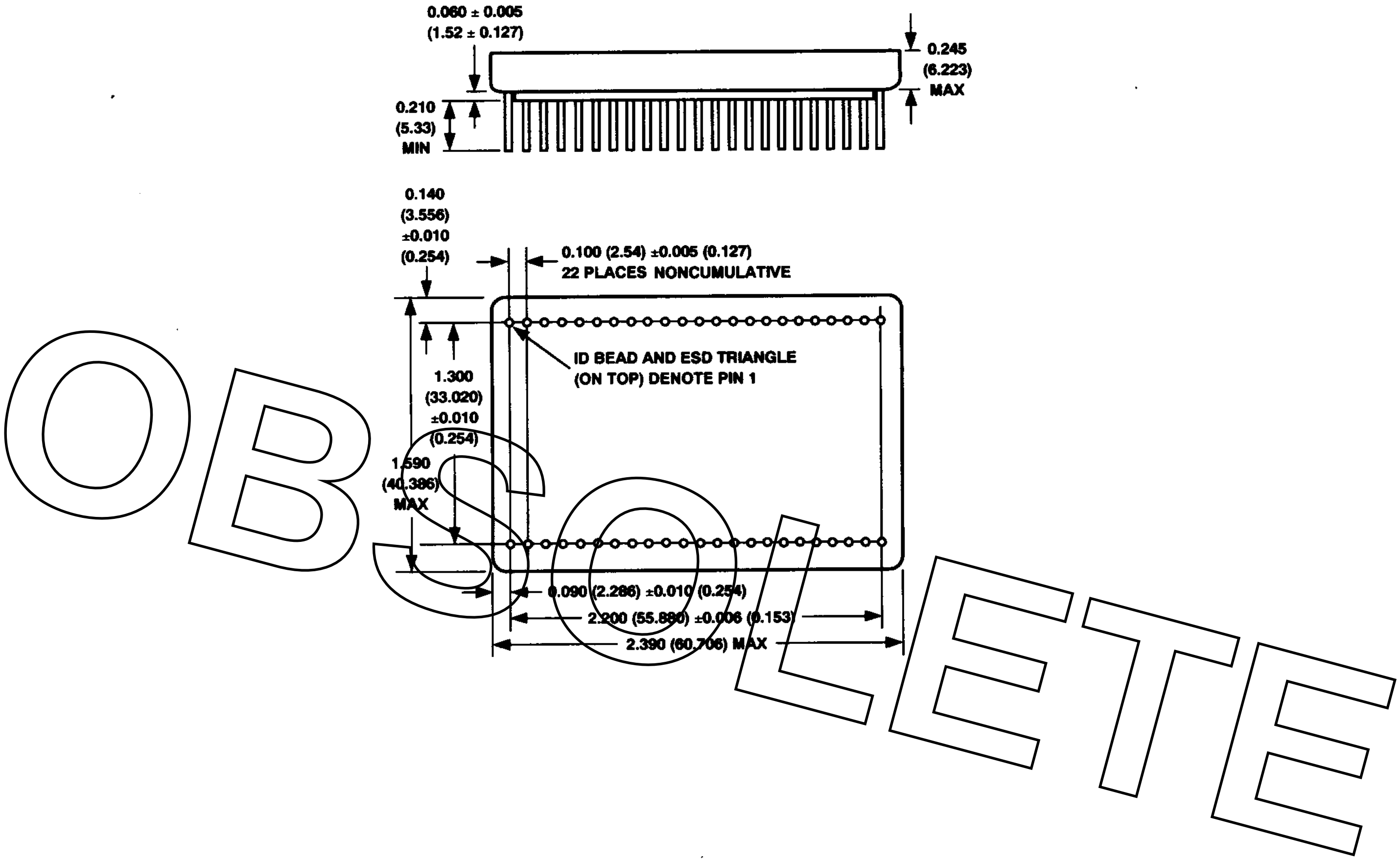


Figure 5. Evaluation Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



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