ANALOG DEVICES

Very Fast, Complete 12-Bit A/D Converter

AD578

FEATURES

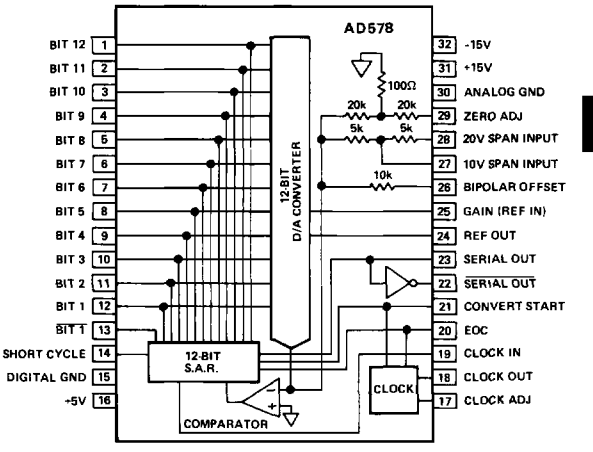
Performance

- **Complete 12-Bit A/D Converter with Reference and Clock**
- **Fast Conversion: 3μs (max)**
- **Buried Zener Reference for Long Term Stability and Low Gain T.C.: ±30ppm/°C max**
- **Max Nonlinearity: < ±0.012%**
- **No Missing Codes Over Temperature**
- **Low Power: 875mW**
- **Hermetic Package Available**
- **Available to MIL-STD-883**

Versatility

- **Positive-True Parallel or Serial Logic Outputs**
- **Short Cycle Capability**
- **Precision +10V Reference for External Applications**
- **Adjustable Internal Clock**
- **"Z" Models for ±12V Supplies**

AD578 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD578 is a high speed 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference and comparator. Its hybrid IC design utilizes MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide superior performance and versatility with IC size, price and reliability.

Important performance characteristics of the AD578 include a maximum linearity error at +25°C of ±0.012%, maximum gain temperature coefficient of ±30ppm/°C, typical power dissipation of 875mW and maximum conversion time of 3μs.

The fast conversion speeds of 3μs (L grade) 4.5μs (K, T grades) and 6μs (J, S grades) make the AD578 an excellent choice in a variety of applications where system throughput rates from 166kHz to 333kHz are required. In addition, it may be short cycled to obtain faster conversion speeds at lower resolutions.

The design of the AD578 includes scaling resistors that provide analog input signal ranges of ±5V, ±10V, 0 to +10V or 0 to +20V. Adding flexibility and value is the +10V precision reference which can be used for external applications.

The AD578 is available with either the polymer seal (N) for use in benign environmental applications or hermetic solder-seal (D) for more harsh or rigorous surroundings. Both are contained in a 32-pin side-brazed, ceramic DIP.

The AD578S, T are available processed to MIL-STD-883 Level B, Method 5008.

PRODUCT HIGHLIGHTS

1. The AD578 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. The fast conversion rate of the AD578 makes it an excellent choice for high speed data acquisition and digital signal processing applications.
3. The internal buried zener reference is laser trimmed to 10.00V ±1.0% and ±15ppm/°C typical T.C. The reference is available for external use and can provide up to 1mA.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The component count is minimized, resulting in low bond wire and chip count and high MTBF.
6. Short cycle and external clock capabilities are provided for applications requiring faster conversion speeds and/or lower resolutions.
7. The integrated package construction provides high quality and reliability with small size and weight.

SPECIFICATIONS (typical @ +25°C, ±15V and +5V unless otherwise noted)

Model	AD578J	AD578K	AD578L	AD578SD[1]	AD578TD[1]
RESOLUTION	12 Bits	*	*	*	*
ANALOG INPUTS					
Voltage Ranges					
Bipolar	±5.0V, ±10V	*	*	*	*
Unipolar	0 to +10V, 0 to +20V	*	*	*	*
Input Impedance					
0 to +10V, ±5V	5kΩ	*	*	*	*
±10V, 0 to +20V	10kΩ	*	*	*	*
DIGITAL INPUTS					
Convert Command[2]	1LSTTL Load	*	*	*	*
Clock Input	1LSTTL Load	*	*	*	*
TRANSFER CHARACTERISTICS					
Gain Error[3,4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Unipolar Offset[4]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Bipolar Error[4,5]	±0.1% FSR, ±0.25% FSR max	*	*	*	*
Linearity Error, 25°C	±1/2LSB max	*	*	*	*
T_{min} to T_{max}	±3/4LSB	*	*	±3/4LSB max	±3/4LSB max
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)					
+25°C	12 Bits	*	*	*	*
T_{min} to T_{max}	12 Bits	*	*	*	*
POWER SUPPLY SENSITIVITY					
+15V ±10%	0.005%/%ΔV_S max	*	*	*	*
−15V ±10%	0.005%/%ΔV_S max	*	*	*	*
+5V ±10%	0.005%/%ΔV_S max	*	*	*	*
TEMPERATURE COEFFICIENTS					
Gain	±15ppm/°C typ	*	*	*	*
	±30ppm/°C max	*	*	±50ppm/°C max	±30ppm/°C max
Unipolar Offset	±3ppm/°C typ	*	*	*	*
	±10ppm/°C max	*	*	±15ppm/°C max	±10ppm/°C max
Bipolar Offset	±8ppm/°C typ	*	*	*	*
	±20ppm/°C max	*	*	±25ppm/°C max	±20ppm/°C max
Differential Linearity	±2ppm/°C typ	*	*	*	*
CONVERSION TIME[6,7,8](max)	6.0μs	4.5μs	3μs	6.0μs	4.5μs
PARALLEL OUTPUTS					
Unipolar Code	Binary	*	*	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*	*	*
Output Drive	2LSTTL Loads	*	*	*	*
SERIAL OUTPUTS (NRZ FORMAT)					
Unipolar Code	Binary/Complementary Binary	*	*	*	*
Bipolar Code	Offset Binary/Comp. Offset Binary	*	*	*	*
Output Drive	2LSTTL Loads	*	*	*	*
END OF CONVERSION (EOC)	Logic "1" During Conversion	*	*	*	*
Output Drive	8LSTTL Loads	*	*	*	*
INTERNAL CLOCK[8]					
Output Drive	2LSTTL Loads	*	*	*	*
INTERNAL REFERENCE					
Voltage	10.000 ±100mV	*	*	*	*
Drift	±12ppm/°C, ±20ppm/°C max	*	*	*	*
External Current	±1mA max	*	*	*	*
POWER SUPPLY REQUIREMENTS[9]					
Range for Rated Accuracy	4.75 to 5.25 and ±13.5 to ±16.5	*	*	*	*
Supply Current +15V	3mA typ, 8mA max	*	*	*	*
−15V	22mA typ, 35mA max	*	*	*	*
+5V	100mA typ, 140mA max	*	*	*	*
Power Dissipation	875mW typ	*	*	*	*
TEMPERATURE RANGE					
Operating	0 to +70°C	*	*	−55°C to +125°C	−55°C to +125°C
Storage	−55°C to +150°C	*	*	−65°C to +150°C	−65°C to +150°C

NOTES

[1]Available to MIL-STD-883, Level B. See ADI Military Products Databook for detail specifications.

[2]Positive pulse 200ns wide (min) leading edge (0 to 1) resets outputs. Trailing edge initiates conversion.

[3]With 50Ω, 1% fixed resistor in place of gain adjust potentiometer.

[4]Adjustable to zero.

[5]With 50Ω, 1% resistor between Ref Out and Bipolar Offset (Pins 24 & 26).

[6]Conversion time is defined as the time between the falling edge of convert start and the falling edge of the EOC.

[7]Each grade is specified at the conversion speed shown.

[8]Externally adjustable by a resistor or capacitor (see Figure 7).

[9]For "Z" models order AD578ZJ, ZK, ZL (±11.6V to ±16.5V).

*Specifications same as AD578J.

Specifications subject to change without notice.

THEORY OF OPERATION

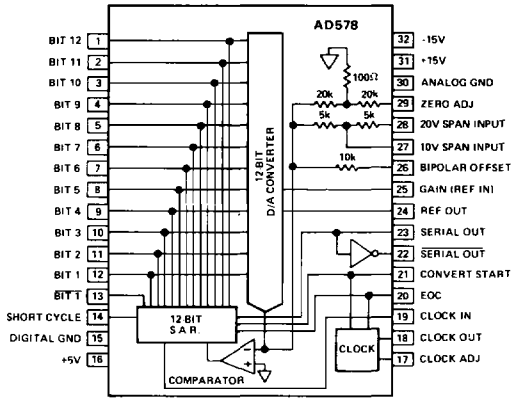


Figure 1. AD578 Functional Diagram and Pinout

The AD578 is a complete pretrimmed 12-bit A/D converter which requires no external components to provide the successive-approximation analog-to-digital conversion function. A block diagram of the AD578 is shown in Figure 1.

When the control section is commanded to initiate a conversion it enables the clock and resets the successive-approximation register (SAR). The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section. The control section disables the clock and brings the output status flag low. The parallel data bits become valid on the rising edge of the clock pulse starting with t_1 and ending with t_{12} (Figure 2), and accurately represent the input signal to within ± 1/2LSB.

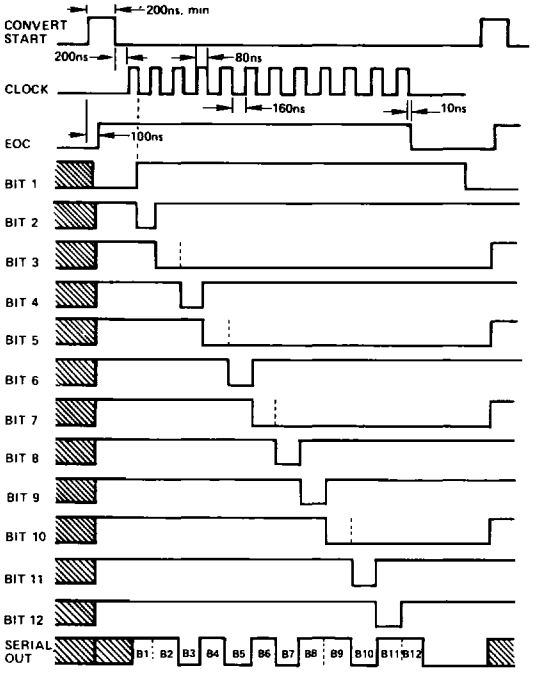
The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ± 1.0%, it is buffered and can supply up to 1.0mA to an external load in addition to the current required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA). The thin-film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

UNIPOLAR CALIBRATION

The AD578 is intended to have a nominal 1/2LSB offset so that the exact analog input for a given code will be in the middle of that code (halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 26 is connected to pin 30, the unit will behave in this manner, within specifications. Refer to Table I and Figure 3 for further clarification. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±25mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963V for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).



CLOCK
INTERNAL: CONNECT CLOCK OUT (18) TO CLOCK IN (19)
EXTERNAL: CONNECT EXTERNAL CLOCK TO CLOCK IN (19)
CLOCK SHOULD BE AT LEAST 30% DUTY CYCLE WITH MINIMUM PERIOD, T_{MIN} OF 100ns.

NOTE
[1]THE RISING EDGE OF CONVERT START PULSE RESETS THE MSB TO ZERO, AND THE LSBs TO ONE. THE TRAILING EDGE INITIATES CONVERSION.

Figure 2. AD578 3µs Timing Diagram

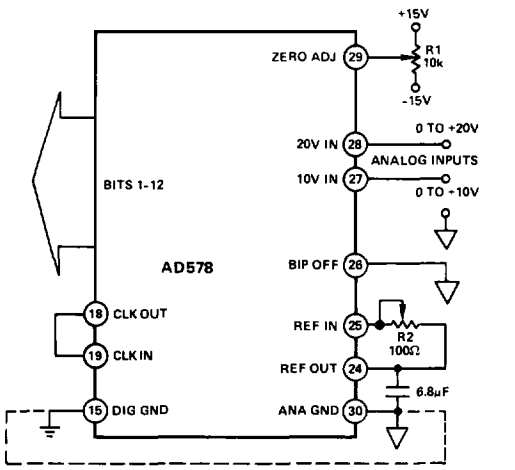


Figure 3. Unipolar Input Connections

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient the 100Ω trimmer shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal 1/2LSB above negative full scale (−4.9988V for the ±5V range) is applied, and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1 1/2LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

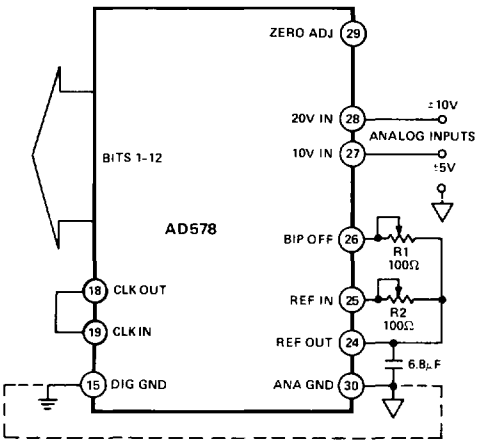


Figure 4. Bipolar Input Connections

LAYOUT CONSIDERATION

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD578. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD578's supply terminals should be capacitively decoupled as close to the AD578 as possible. A large value capacitor such as 10μF in parallel with a 0.1μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Digital GND pin.

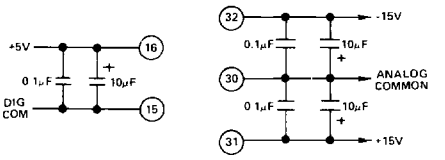


Figure 5. Basic Grounding Practice

To minimize noise the reference output (pin 24) should be decoupled by a 6.8μF capacitor to pin 30.

CLOCK RATE CONTROL

The internal clock is preset to a nominal conversion time of 5.6μs. It can be adjusted for either faster or slower conversions. For faster conversion connect the appropriate 1% resistor between pin 17 and pin 18 and short pin 18 to pin 19.

For slower conversions connect a capacitor between pin 15 and pin 17.

The curves in Figure 6 characterize the conversion time for a given resistor or capacitor connection.

Note: 12-bit operation with no missing codes is not guaranteed when operating in this mode if a particular grade's conversion speed specification has been exceeded.

Short Cycle Input – A Short Cycle Input, pin 14, permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, allowing somewhat shorter conversion times in applications not requiring full 12-bit resolution. Short cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table II.

Analog Input – Volts (Center of Quantization Interval)				Digital Output Code (Binary For Unipolar Ranges; Offset Binary for Bipolar Ranges)
0 to +10V Range	0 to +20V Range	−5V to +5V Range	−10V to +10V Range	B1 (MSB) B12 (LSB)
+9.9976	+19.9951	+4.9976	+9.9951	1 1 1 1 1 1 1 1 1 1 1 1
+9.9952	+19.9902	+4.9952	+9.9902	1 1 1 1 1 1 1 1 1 1 1 0
•	•	•	•	•
•	•	•	•	•
+5.0024	+10.0049	+0.0024	+0.0049	1 0 0 0 0 0 0 0 0 0 0 1
+5.0000	+10.0000	+0.0000	+0.0000	1 0 0 0 0 0 0 0 0 0 0 0
•	•	•	•	•
•	•	•	•	•
+0.0024	+0.0051	−4.9976	−9.9951	0 0 0 0 0 0 0 0 0 0 0 1
+0.0000	+0.0000	−5.0000	−10.0000	0 0 0 0 0 0 0 0 0 0 0 0

Table I. Digital Output Codes vs. Analog Input for Unipolar and Bipolar Ranges

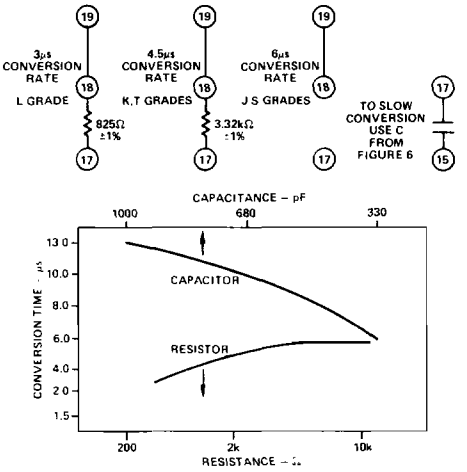


Figure 6. Conversion Times vs. R or C Values

Resolution (Bits)	12	10	8
Connect Pin 14 to Pin	16	2	4
Conversion Speed (μs)	3	2.5	2

Table II. Short Cycle Connections

External Clock – An external clock may be connected directly to the clock input, pin 19. When operating in this mode, the convert start should be held high for a minimum of one clock period in order to reset the SAR and synchronize the conversion cycle. A positive going pulse width of 100 to 200 nanoseconds will provide a continuous string of conversions that start on the first rising edge of the external clock after the EOC output has gone low.

External Buffer Amplifier – In applications where the AD578 is to be driven from high impedance sources or directly from an analog multiplexer a fast slewing, wideband op amp like the AD711 should be used.

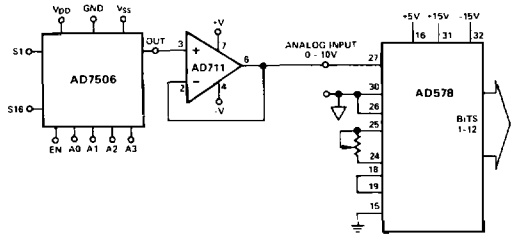


Figure 7. Input Buffer

MICROPROCESSOR INTERFACING

The 3μs conversion times of the AD578 suggests several different methods of interface to microprocessors. In systems where the AD578 is used for high sampling rates on a single signal which is to be digitally processed, CPU-controlled conversion may be inefficient due to the slow cycle times of most microprocessors. It is generally preferable to perform conversions independently, inserting the resultant digital data directly into memory. This can be done using direct memory access (DMA) which is totally transparent to the CPU. Interface to user-designed DMA hardware is facilitated by the guaranteed data validity on the falling edge of the EOC signal.

In many multichannel data acquisition systems, the processor spends a good deal of time waiting for the ADC to complete its cycle. Converters with total conversion times of 25μs to 100μs are not slow enough to justify use of interrupts, nor fast enough to finish converting during one instruction and are usually timed out with loops, or continuously polled for status. The AD578 allows the microprocessor to time out the converter with just a few dummy instructions. For example, an 8085 system running at a 5MHz clock rate will time out an AD578 by pushing a register pair onto the stack and popping the same pair back off the stack. Such a time-out routine only occupies two bytes of program memory but requires 22 clock cyles (4.4μs). The time saved by not having to wait for the converter allows the processor to run much more efficiently particularly in multichannel systems.

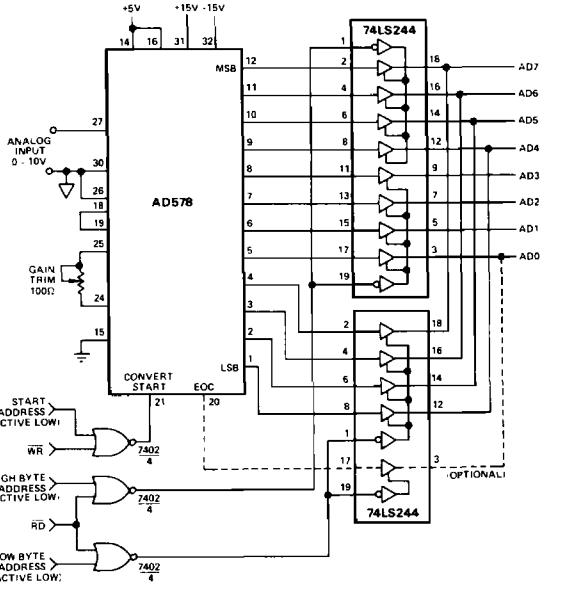


Figure 8. AD578–8085A Interface Connections

Clearly, 12 bits of data must be broken up for interface to an 8-bit wide data bus. There are two possible formats: right-justified and left-justified. In a right-justified system, the least-significant 8 bits occupy one byte and the four MSBs reside in the low nybble of another byte. This format is useful when the data from the ADC is being treated as a binary number between 0 and 4095. The left-justified format supplies the eight most-significant bits in one byte and the 4LSBs in the high nybble of another byte. The data now represents the fractional binary number relating the analog signal to the full-scale voltage. An advantage to this organization is that the most-significant eight bits can be read by the processor as a coarse indication of the true signal value. The full 12-bit word can then be read only when all 12 bits are needed. This allows faster and more efficient control of a process.

Figure 8 shows a typical connection to an 8085-type bus, using left-justified data format for unipolar inputs. Status polling is

optional, and can be read simultaneously with the 4LSBs. If it is desired to right-justify the data, pins 1 through 12 of the AD578 should be reversed, as well as the connections to the data bus and high and low byte address signals.

When dealing with bipolar inputs ($\pm 5V$, $\pm 10V$ ranges), using the MSB directly yields an offset binary-coded output. If two's complement coding is desired, it can be produced by substituting $\overline{MSB}$ (pin 13) for the MSB. This facilitates arithmetic operations which are subsequently performed on the ADC output data.

SAMPLED DATA SYSTEMS

The conversion speed of the AD578 allows accurate digitization of high frequency signals and high throughput rates in multi-channel data acquisition systems. The AD578LD, for example, is capable of a full accuracy conversion in 3μs. In order to benefit from this high speed, a fast sample-hold amplifier (SHA) such as the HTC-0300 is required. This SHA has an acquisition time to 0.01% of approximately 300ns, so that a complete sample-convert-acquire cycle can be accomplished in approximately 4μs. This means a sample rate of 250kHz can be realized, allowing a signal with no frequency components above 125kHz to be sampled with no loss of information. Note that the EOC signal from the AD578 places the SHA in the hold mode in advance of the actual start of the conversion cycle, and releases the SHA from the HOLD mode only after completion of the conversion. After allowing at least 300ns for the SHA to acquire the next analog value, the converter can again be started.

AD578 ORDERING GUIDE*

	Conversion Speed	Temperature Range	Package Option[1]
AD578JN(JD)	6.0μs	0 to +70°C	Solder Seal (DH-32B)
AD578KN(KD)	4.5μs	0 to +70°C	Solder Seal (DH-32B)
AD578LN(LD)	3.0μs	0 to +70°C	Solder Seal (DH-32B)
AD578SD	6.0μs	−55°C to +125°C	Solder Seal (DH-32B)
AD578SD/883B	6.0μs	−55°C to +125°C	Solder Seal (DH-32B)
AD578TD/883B	4.5μs	−55°C to +125°C	Solder Seal (DH-32B)

*For ±12V operation "Z" version order: AD578ZJN, . . .

[1] See Section 14 for package outline information.