# *MAXIM*

# *Quad LVDS Receiver with Hysteresis*

**MAX9179**

## General Description

The MAX9179 is a quad low-voltage differential signaling (LVDS) line receiver designed for applications requiring high data rates, low power dissipation, and noise immunity. The receiver accepts four LVDS input signals and translates them to 3.3V LVCMOS output levels at speeds up to 400Mbps. The receiver features built-in hysteresis, which improves noise immunity and prevents multiple switching on slow transitioning inputs.

The device supports a wide 0.038V to 2.362V common-mode input voltage range, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe circuit sets the output high when the input is open, undriven and shorted, or undriven and terminated. Common enable inputs control the high-impedance outputs.

The MAX9179 has a flow-through pinout for easy PC board layout, and is pin compatible with the MAX9121 and the DS90LV048A with the additional features of high ESD tolerance and built-in hysteresis.

The MAX9179 operates from a single 3.3V supply, and is specified for operation from -40°C to +85°C. The device is offered in 16-pin TSSOP and thin QFN packages.

## Applications

Laser Printers

Digital Copiers

Cell-Phone Base Stations

Telecom Switching Equipment

LCD Displays

Network Switches/Routers

Backplane Interconnect

Clock Distribution

## Features

♦ **Guaranteed 400Mbps Data Rate**

♦ **50mV (typ) Hysteresis**

♦ **Overshoot/Undershoot Protection (-1.0V or $V_{CC}$ + 1.0V) on Enables**

♦ **IEC61000-4-2 Level 4 ESD Tolerance**

♦ **AC Specifications Guaranteed with |$V_{ID}$| $_=$ 100mV**

♦ **Single 3.3V Supply**

♦ **Fail-Safe Circuit**

♦ **Flow-Through Pinout**
   **Simplifies PC Board Layout**
   **Reduces Crosstalk**

♦ **Low-Power CMOS Design**

♦ **Conforms to ANSI TIA/EIA-644 LVDS Standard**

♦ **High-Impedance Inputs when Powered Off**

♦ **Pin Compatible with the MAX9121 and the DS90LV048A**

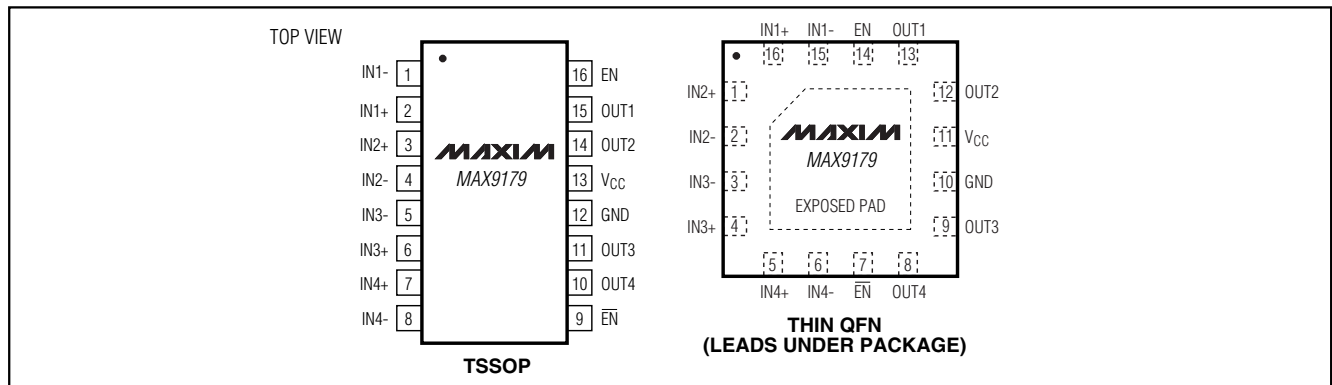♦ **Small Thin QFN Package Available**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX9179EUE | -40°C to +85°C | 16 TSSOP |
| MAX9179ETE* | -40°C to +85°C | 16 Thin QFN-EP** |

*Future product—contact factory for availability.*
***EP = Exposed paddle.*

*Functional Diagram appears at end of data sheet.*

## Pin Configurations



**TSSOP**

**THIN QFN
(LEADS UNDER PACKAGE)**

*For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.*

# Quad LVDS Receiver with Hysteresis

## ABSOLUTE MAXIMUM RATINGS

$V_{CC}$ to GND ...........................................................-0.3V to +4.0V
IN_+, IN_- to GND .................................................-0.3V to +4.0V
EN, $\overline{EN}$ to GND ...........................................-1.4V to ($V_{CC}$ + 1.4V)
OUT_ to GND ...........................................-0.3V to ($V_{CC}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
  16-Pin TSSOP (derate 9.4mW/°C above +70°C) .........755mW
  16-Pin Thin QFN (derate 16.9mW/°C
  above +70°C)...............................................................1349mW
Junction Temperature .....................................................+150°C

Storage Temperature Range .............................-65°C to +150°C
ESD Protection
  Human Body Model ($R_D$ = 1.5kΩ, $C_S$ = 100pF)
    (IN_+, IN_-) ................................................................±16kV
  IEC61000-4-2 ($R_D$ = 330Ω, $C_S$ = 150pF) (IN_+, IN_-)
    Contact Discharge ......................................................±8kV
    Air-Gap Discharge .....................................................±15kV
Soldering Temperature (soldering, 10s).........................+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## DC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.0V to 3.6V, differential input voltage $|V_{ID}|$ = 0.075V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.2V, $T_A$ = +25°C.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **INPUTS (IN_+, IN_-)** | | | | | | | |
| Differential Input High Threshold | $V_{TH}$ | Figure 1 | | | 25 | 75 | mV |
| Differential Input Low Threshold | $V_{TL}$ | Figure 1 | | -75 | -25 | | mV |
| Hysteresis | $V_{TH}$ - $V_{TL}$ | Figure 1 | | | 50 | | mV |
| Input Current | $I_{IN+}$, $I_{IN-}$ | | | -20 | | +20 | µA |
| Power-Off Input Current | $I_{OFF+}$, $I_{OFF-}$ | $V_{CC}$ = 0V | | -20 | | +20 | µA |
| Fail-Safe Input Resistor 1 | $R_{IN1}$ | $V_{CC}$ = 3.6V or 0V, Figure 2 | | 40 | | 65 | kΩ |
| Fail-Safe Input Resistor 2 | $R_{IN2}$ | $V_{CC}$ = 3.6V or 0V, Figure 2 | | 280 | | 455 | kΩ |
| **OUTPUTS (OUT_)** | | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA | Open, undriven short, or undriven parallel termination | $V_{CC}$ - 0.2 | $V_{CC}$ - 0.1 | | V |
| | | | $V_{ID}$ = +50mV | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 4.0mA, $V_{ID}$ = -50mV | | | 0.1 | 0.25 | V |
| Output Short-Circuit Current | $I_{OS}$ | Enabled, $V_{ID}$ = +50mV, $V_{OUT}$ = 0 (Note 3) | | -40 | -70 | -120 | mA |
| Output High-Impedance Current | $I_{OZ}$ | Disabled, $V_{OUT}$ = 0 or $V_{CC}$ | | -1.0 | | +1.0 | µA |
| **ENABLE INPUTS (EN, $\overline{EN}$)** | | | | | | | |
| Input High Voltage | $V_{IH}$ | | | 2.0 | | $V_{CC}$ + 1.0 | V |
| Input Low Voltage | $V_{IL}$ | | | -1.0 | | +0.8 | V |
| Input Current | $I_{IN}$ | -1.0V ≤ EN, $\overline{EN}$ ≤ 0V | | -1800 | | +10 | µA |
| | | 0V ≤ EN, $\overline{EN}$ ≤ $V_{CC}$ | | -20 | | +20 | |
| | | $V_{CC}$ ≤ EN, $\overline{EN}$ ≤ $V_{CC}$ + 1.0V | | -10 | | +1800 | |
| **POWER SUPPLY** | | | | | | | |
| Supply Current | $I_{CC}$ | Enabled, inputs open | | | 10.4 | 15 | mA |
| Disabled Supply Current | $I_{CCZ}$ | Disabled, inputs open | | | 0.6 | 1.0 | |

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## AC ELECTRICAL CHARACTERISTICS

($V_{CC}$ = 3.0V to 3.6V, $C_L$ = 15pF, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage $V_{CM}$ = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{CC}$ = 3.3V, $|V_{ID}|$ = 0.2V, $V_{CM}$ = 1.2V, $T_A$ = +25°C.) (Notes 4, 5, 6)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Propagation Delay High to Low | $t_{PHLD}$ | Figures 3, 4 | 2.0 | 2.6 | 4.6 | ns |
| Differential Propagation Delay Low to High | $t_{PLHD}$ | Figures 3, 4 | 2.0 | 2.52 | 4.6 | ns |
| Differential Pulse Skew $\| t_{PHLD} - t_{PLHD} \|$ (Note 7) | $t_{SKD1}$ | $\|V_{ID}\|$ = 0.1V to 0.15V | | | 700 | ps |
| | | $\|V_{ID}\|$ = 0.15V to 0.2V | | | 400 | |
| | | $\|V_{ID}\|$ = 0.2V to 1.2V | | 80 | 300 | |
| Differential Channel-to-Channel Skew, Same Part (Note 8) | $t_{SKD2}$ | $\|V_{ID}\|$ = 0.1V to 0.15V | | | 900 | ps |
| | | $\|V_{ID}\|$ = 0.15V to 0.2V | | | 600 | |
| | | $\|V_{ID}\|$ = 0.2V to 1.2V | | 120 | 400 | |
| Differential Part-to-Part Skew (Note 9) | $t_{SKD3}$ | | | | 2.0 | ns |
| Differential Part-to-Part Skew (Note 10) | $t_{SKD4}$ | | | | 2.6 | ns |
| Rise Time | $t_{TLH}$ | | | 0.77 | 1.4 | ns |
| Fall Time | $t_{THL}$ | | | 0.74 | 1.4 | ns |
| Disable Time High to Z | $t_{PHZ}$ | $R_L$ = 2kΩ, Figures 5, 6 (Note 11) | | 10.6 | 14 | ns |
| Disable Time Low to Z | $t_{PLZ}$ | $R_L$ = 2kΩ, Figures 5, 6 (Note 11) | | 11 | 14 | ns |
| Enable Time Z to High | $t_{PZH}$ | $R_L$ = 2kΩ, Figures 5, 6 (Note 11) | | 4.8 | 14 | ns |
| Enable Time Z to Low | $t_{PZL}$ | $R_L$ = 2kΩ, Figures 5, 6 (Note 11) | | 4.8 | 14 | ns |
| Maximum Operating Frequency | $f_{MAX}$ | All channels switching, $C_L$ = 15pF, $V_{OL}$ (max) = 0.25V, $V_{OH}$ (min) = $V_{CC}$ - 0.2V, 44% < duty cycle < 56% | 200 | 250 | | MHz |

**Note 1:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Parts are production tested at $T_A$ = +25°C.
**Note 2:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except $V_{TH}$, $V_{TL}$, and $V_{ID}$.
**Note 3:** Short one output at a time.
**Note 4:** AC parameters are guaranteed by design and characterization. Limits are set at ±6 sigma.
**Note 5:** $C_L$ includes scope probe and test jig capacitance.
**Note 6:** Pulse generator differential output for all tests (unless otherwise noted): $t_R$ = $t_F$ < 1ns (0% to 100%), frequency = 100MHz, 50% duty cycle.
**Note 7:** $t_{SKD1}$ is the magnitude of the difference of the differential propagation delays in a channel. $t_{SKD1}$ = $\| t_{PHLD} - t_{PLHD} \|$.
**Note 8:** $t_{SKD2}$ is the magnitude of the difference of the $t_{PLHD}$ or $t_{PHLD}$ of one channel and the $t_{PLHD}$ or $t_{PHLD}$ of the other channel on the same part.
**Note 9:** $t_{SKD3}$ is the magnitude of the difference of any differential propagation delays between parts at the same $V_{CC}$ and within 5°C of each other.
**Note 10:** $t_{SKD4}$ is the magnitude of the difference of any differential propagation delays between parts operating over the rated supply and temperature ranges.
**Note 11:** Pulse generator output for $t_{PHZ}$, $t_{PLZ}$, $t_{PZH}$, and $t_{PZL}$ tests: $t_R$ = $t_F$ = 1.5ns ($0.2V_{CC}$ to $0.8V_{CC}$), 50% duty cycle, $V_{OH}$ = $V_{CC}$ + 1.0V settling to $V_{CC}$, $V_{OL}$ = -1.0V settling to 0, frequency = 1MHz.

# Quad LVDS Receiver with Hysteresis
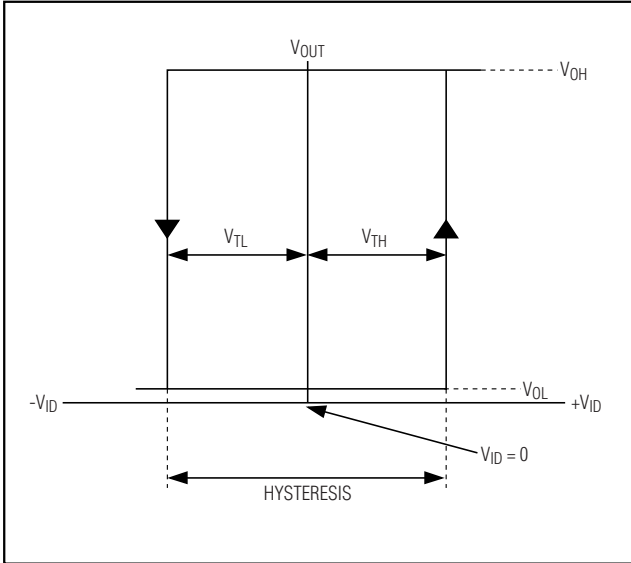
## Test Circuits/Timing Diagrams



Figure 1. Input Thresholds and Hysteresis
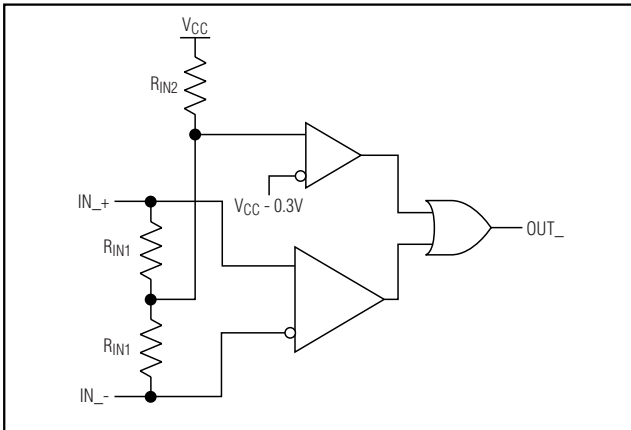


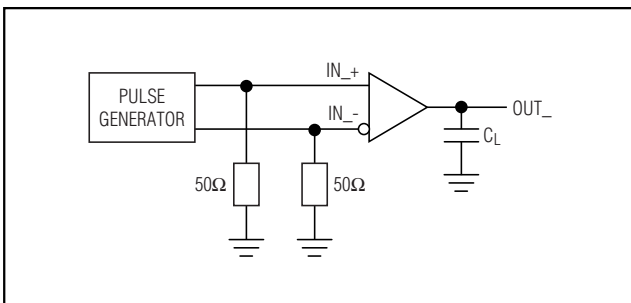Figure 2. Fail-Safe Input Circuit



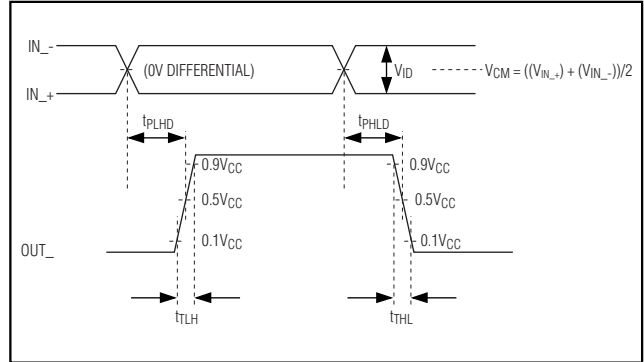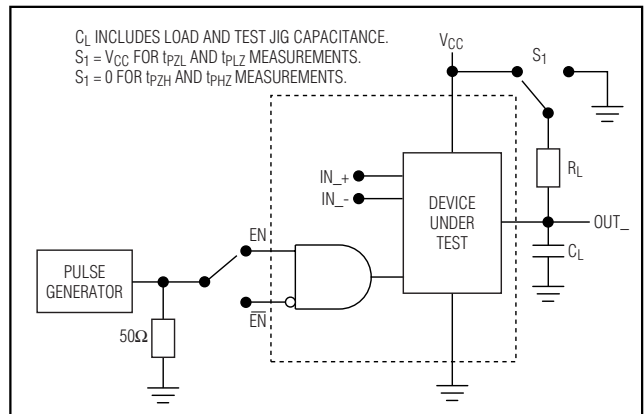Figure 3. Propagation Delay and Transition Time Test Circuit



Figure 4. Propagation Delay and Transition Time Waveforms
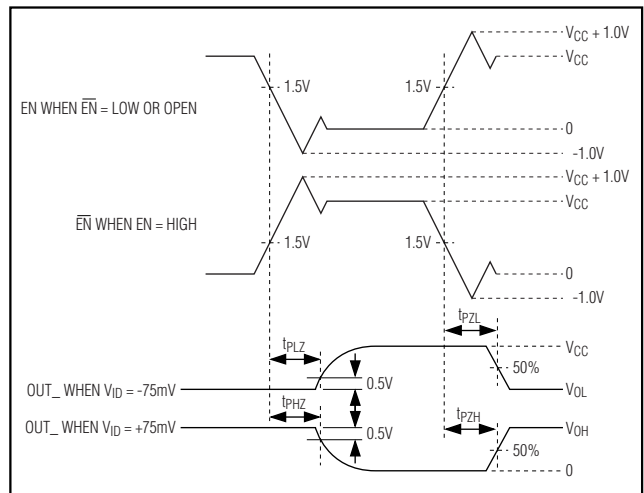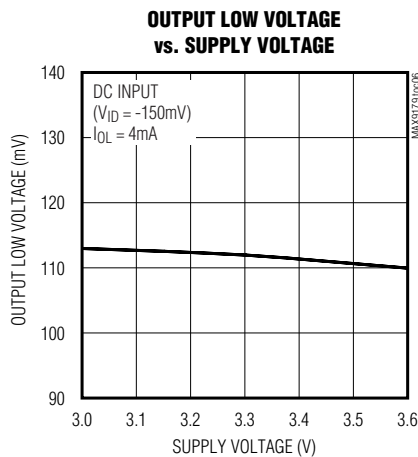


Figure 5. High-Impedance Delay Test Circuit



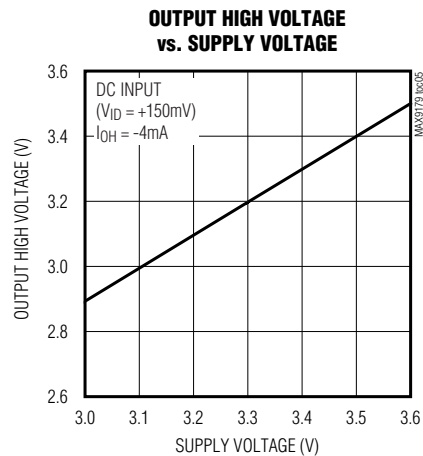Figure 6. High-Impedance Delay Waveforms

4

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(V$_{CC}$ = 3.3V, V$_{CM}$ = 1.2V, |V$_{ID}$| = 0.15V, C$_L$ = 15pF, f = 100MHz, T$_A$ = +25°C, unless otherwise noted.)

**SUPPLY CURRENT vs. FREQUENCY**

MAX9179 toc01

SUPPLY CURRENT (mA)

ALL CHANNELS DRIVEN

FREQUENCY (MHz)

**SUPPLY CURRENT vs. TEMPERATURE**

MAX9179 toc02

SUPPLY CURRENT (mA)

INPUTS OPEN

TEMPERATURE (°C)

**DC DIFFERENTIAL THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE**

MAX9179 toc03

DC DIFFERENTIAL THRESHOLD VOLTAGE (mV)

V$_{TH}$

V$_{TL}$

SUPPLY VOLTAGE (V)

**OUTPUT SHORT-CIRCUIT CURRENT vs. SUPPLY VOLTAGE**

MAX9179 toc04

OUTPUT SHORT-CIRCUIT CURRENT (mA)

DC INPUT
(V$_{ID}$ = +150mV)

SUPPLY VOLTAGE (V)

**OUTPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE**

MAX9179 toc05

OUTPUT HIGH VOLTAGE (V)

DC INPUT
(V$_{ID}$ = +150mV)
I$_{OH}$ = -4mA

SUPPLY VOLTAGE (V)

**OUTPUT LOW VOLTAGE vs. SUPPLY VOLTAGE**

MAX9179 toc06

OUTPUT LOW VOLTAGE (mV)

DC INPUT
(V$_{ID}$ = -150mV)
I$_{OL}$ = 4mA

SUPPLY VOLTAGE (V)

**DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE**

MAX9179 toc07

DIFFERENTIAL PROPAGATION DELAY (ns)

t$_{PHLD}$

t$_{PLHD}$

SUPPLY VOLTAGE (V)

*MAXIM* _____ 5

# Quad LVDS Receiver with Hysteresis

_____Typical Operating Characteristics (continued)

($V_{CC}$ = 3.3V, $V_{CM}$ = 1.2V, $|V_{ID}|$ = 0.15V, $C_L$ = 15pF, f = 100MHz, $T_A$ = +25°C, unless otherwise noted.)
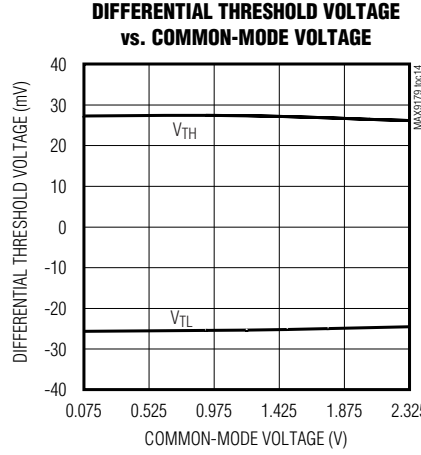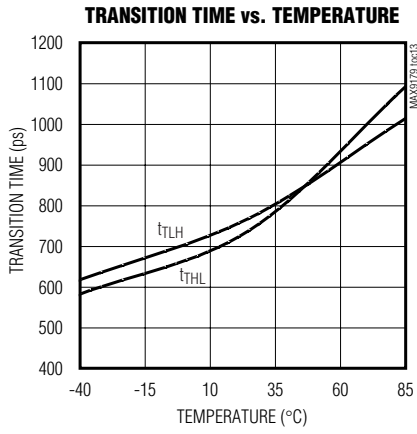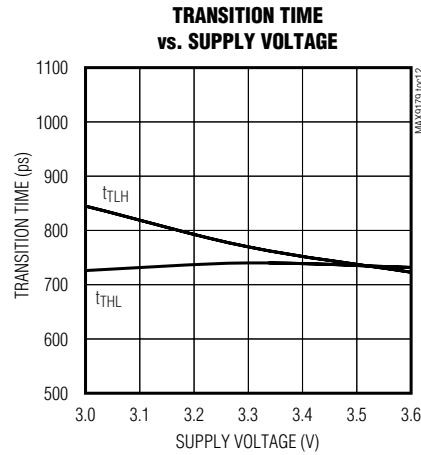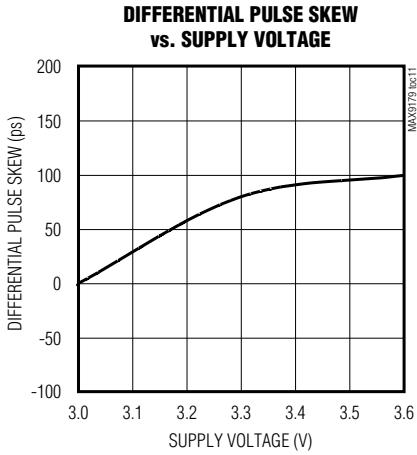
**DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE**

**DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE**

**DIFFERENTIAL PROPAGATION DELAY vs. DIFFERENTIAL INPUT VOLTAGE**

**DIFFERENTIAL PULSE SKEW vs. SUPPLY VOLTAGE**

**TRANSITION TIME vs. SUPPLY VOLTAGE**

**TRANSITION TIME vs. TEMPERATURE**

**DIFFERENTIAL THRESHOLD VOLTAGE vs. COMMON-MODE VOLTAGE**

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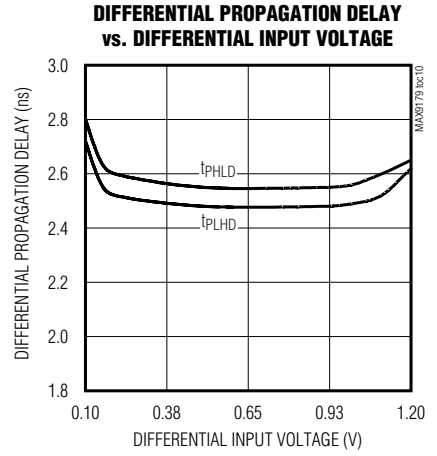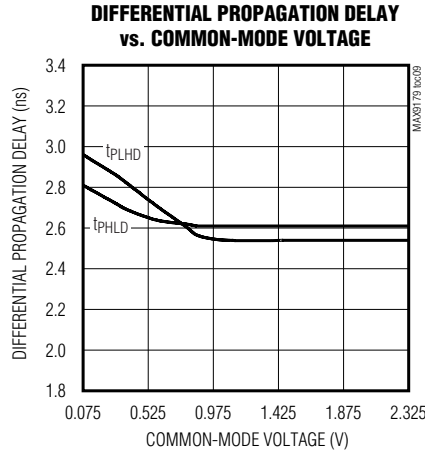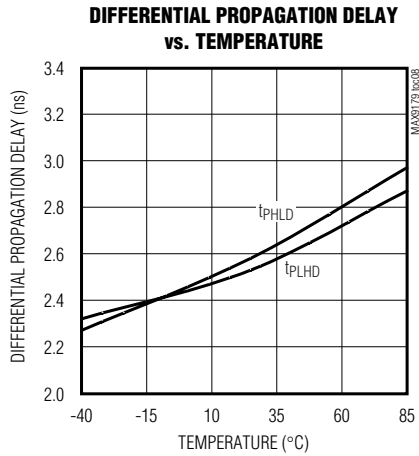
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## _Pin Description_

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| TSSOP | QFN | | |
| 1 | 15 | IN1- | Inverting LVDS Input 1 |
| 2 | 16 | IN1+ | Noninverting LVDS Input 1 |
| 3 | 1 | IN2+ | Noninverting LVDS Input 2 |
| 4 | 2 | IN2- | Inverting LVDS Input 2 |
| 5 | 3 | IN3- | Inverting LVDS Input 3 |
| 6 | 4 | IN3+ | Noninverting LVDS Input 3 |
| 7 | 5 | IN4+ | Noninverting LVDS Input 4 |
| 8 | 6 | IN4- | Inverting LVDS Input 4 |
| 9 | 7 | $\overline{EN}$ | Enable Complementary Input. The outputs are active when EN = high and $\overline{EN}$ = low or open. For all other combinations of EN and $\overline{EN}$, the outputs are disabled and in high impedance. |
| 10 | 8 | OUT4 | LVCMOS/LVTTL Output 4 |
| 11 | 9 | OUT3 | LVCMOS/LVTTL Output 3 |
| 12 | 10 | GND | Ground |
| 13 | 11 | $V_{CC}$ | Power-Supply Input. Bypass $V_{CC}$ to GND with 0.1µF and 0.001µF ceramic capacitors. |
| 14 | 12 | OUT2 | LVCMOS/LVTTL Output 2 |
| 15 | 13 | OUT1 | LVCMOS/LVTTL Output 1 |
| 16 | 14 | EN | Enable Input. The outputs are active when EN = high and $\overline{EN}$ = low or open. For all other combinations of EN and $\overline{EN}$, the outputs are disabled and in high impedance. |
| — | EP | Exposed Pad | Exposed Pad. Connect to ground. |

**MAX9179**

## Table 1. Functional Table

| ENABLES | | INPUTS | OUTPUT |
|---|---|---|---|
| EN | $\overline{EN}$ | (IN_+) - (IN_-) | OUT_ |
| H | L or open | ≥ +75mV | H |
| | | ≤ -75mV | L |
| | | Open, undriven short, or undriven terminated | H |
| All other combinations of enable inputs | | X | Z |

H = High logic level
L = Low logic level
X = Don't care
Z = High impedance

## Detailed Description

The LVDS is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards.

The MAX9179 is a quad LVDS line receiver with built-in hysteresis, intended for high-speed, point-to-point, low-power applications. The receiver accepts four LVDS input signals and translates them to 3.3V LVCMOS output levels at speeds up to 400Mbps over controlled-impedance media of 100Ω. The hysteresis improves noise immunity and prevents multiple switching due to noise on slow input transitions at the end of a long cable.

The receiver is capable of detecting differential signals as low as 75mV and as high as 1.2V within a 0 to 2.4V input voltage range. The 250mV to 450mV differential output of an LVDS driver is nominally centered on a 1.2V offset. This offset, coupled with the receiver's 0 to 2.4V input voltage range, allows an approximate ±1V shift in the signal (as seen by the receiver). This allows for a difference in ground references of the transmitter and the receiver, the common-mode effects of coupled noise, or both. The LVDS standards specify an input voltage range of 0 to 2.4V referenced to receiver ground.

### Hysteresis

The MAX9179 incorporates hysteresis of 50mV (typ), which rejects noise and prevents false switching during low-slew-rate transitions at the end of a long cable. The receiver typically switches at 25mV above or below $V_{ID}$ = 0V (Figure 1). The hysteresis is designed to be symmetrical around $V_{ID}$ = 0V for low pulse distortion (see the *Typical Operating Characteristics*).

### Input Fail-Safe

The fail-safe feature of the MAX9179 sets the output high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the input is undriven, noise at the input may switch the output and it may appear to the system that data is being sent. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when a driver output is in high impedance. A shorted input can occur because of a cable failure.

When the input is driven with a differential signal of $|V_{ID}|$ = 75mV to 1.2V within a voltage range of 0 to 2.4V, the fail-safe circuit is not activated. If the input is open, undriven and shorted, or undriven and terminated, an internal resistor in the fail-safe circuit pulls both inputs above $V_{CC}$ - 0.3V, activating the fail-safe circuit and forcing the output high (Figure 2).

### Overshoot and Undershoot Voltage Protection

The MAX9179 is designed to protect the enable inputs (EN and $\overline{EN}$) against latchup due to transient overshoot and undershoot voltage. If the enable input voltage goes above $V_{CC}$ or below GND by up to 1V, an internal circuit clamps and limits input current to 1.8mA.

## Applications Information

### Power-Supply Bypassing

Bypass the $V_{CC}$ pin with high-frequency surface-mount ceramic 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to $V_{CC}$.

### Differential Traces

Input trace characteristics affect the performance of the MAX9179. Use controlled-impedance differential traces (100Ω is typical). To reduce radiated noise and ensure that noise couples as common mode, route the differential input signals within a pair close together. Reduce skew by matching the electrical length of the signal paths making up the differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

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## Cables and Connectors

Interconnect for LVDS typically has a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities. Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

## Termination

The MAX9179 requires external termination resistors. The input termination resistor used on each active channel should match the differential impedance of the transmission line. Place the termination resistor as close to the MAX9179 receiver input as possible. Use 1% surface-mount resistors.

## Board Layout

Keep the LVDS input and LVCMOS output signals separated from each other to reduce crosstalk; 180 degrees of separation between LVDS inputs and LVCMOS outputs is recommended. Because there are leads on all sides, this separation requires special attention when laying out traces for the QFN package.

A four-layer printed circuit board with separate layers for power, ground, LVDS inputs, and single-ended logic signals is recommended. Separate the LVDS signals from the single-ended signals with power and ground planes for best results.

## IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard (Figure 7) specifies ESD tolerance for electronic systems. The IEC61000-4-2 model specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9179 LVDS inputs are rated for IEC61000-4-2 level 4 (±8kV Contact Discharge and ±15kV Air-Gap Discharge). The Human Body Model (HBM) (Figure 8) specifies a 100pF capacitor that is discharged into the device through a 1.5kΩ resistor. The IEC 61000-4-2 discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor.

## Chip Information

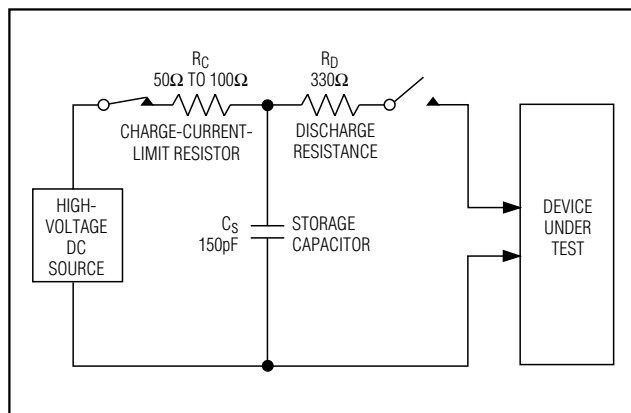TRANSISTOR COUNT: 1173
PROCESS: CMOS
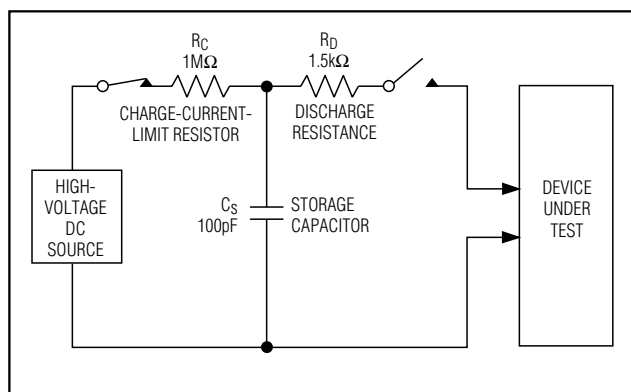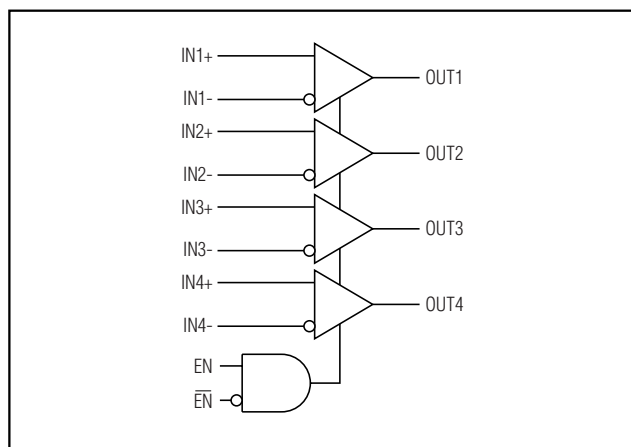


Figure 7. IEC61000-4-2 Test Model



Figure 8. Human Body Test Model

## Functional Diagram

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS

**TOP VIEW**

3 2 1

H

N

**BOTTOM VIEW**

**SIDE VIEW**

SEE DETAIL A

e

A

A₁

0.10 C 6

SEATING PLANE

D

**END VIEW**

A₂

C

C

E

0.25 BSC

PARTING LINE

CC

L

**DETAIL A**

WITH PLATING

BASE METAL

**LEAD TIP DETAIL**

b

b1

c1 c

### COMMON DIMENSIONS

| SYMBOL | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | — | 1.10 | | .043 |
| A₁ | 0.05 | 0.15 | .002 | .006 |
| A₂ | 0.85 | 0.95 | .033 | .037 |
| b | 0.19 | 0.30 | .007 | .012 |
| b₁ | 0.19 | 0.25 | .007 | .010 |
| c | 0.09 | 0.20 | .004 | .008 |
| c₁ | 0.09 | 0.14 | .004 | .006 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BSC | | .026 BSC | |
| H | 6.25 | 6.55 | .246 | .258 |
| L | 0.50 | 0.70 | .020 | .028 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

### VARIATIONS

| JEDEC MO-153 | N | | MILLIMETERS | | INCHES | |
|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. |
| AB-1 | 14 | D | 4.90 | 5.10 | .193 | .201 |
| AB | 16 | D | 4.90 | 5.10 | .193 | .201 |
| AC | 20 | D | 6.40 | 6.60 | .252 | .260 |
| AD | 24 | D | 7.70 | 7.90 | .303 | .311 |
| AE | 28 | D | 9.60 | 9.80 | .378 | .386 |

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. 'N' REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

**DALLAS SEMICONDUCTOR** **MAXIM**

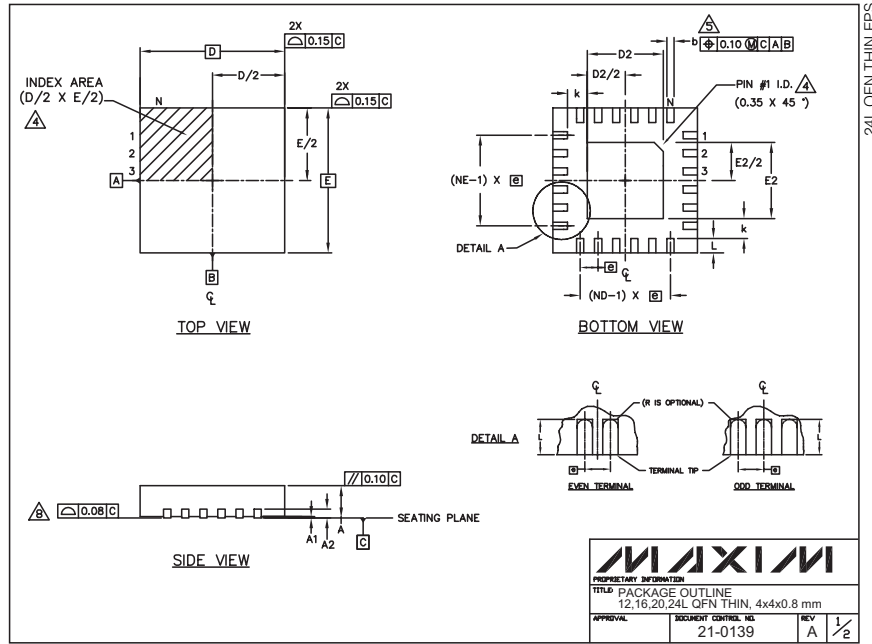PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, TSSOP 4.40mm BODY

| APPROVAL | DOCUMENT CONTROL NO. | REV. | 1/1 |
|---|---|---|---|
| | 21-0066 | F | |

**MAXIM**

# Quad LVDS Receiver with Hysteresis

## Package Information (continued)

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24L QFN THIN.EPS

TOP VIEW

BOTTOM VIEW

DETAIL A

SIDE VIEW

EVEN TERMINAL     ODD TERMINAL

**/V/I /I XI /V/I**
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV A | 1/2

### COMMON DIMENSIONS

| PKG REF. | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| A1 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | | 0.20 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | |
| k | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – | 0.25 | – | – |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | |
| Jedec Var. | WGGB | | | WGGC | | | WGGD-1 | | | WGGD-2 | | |

### EXPOSED PAD VARIATIONS

| PKG. CODES | D2 | | | E2 | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1244-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-1 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-1 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.

**/V/I /I XI /V/I**
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE
12,16,20,24L QFN THIN, 4x4x0.8 mm
APPROVAL | DOCUMENT CONTROL NO. 21-0139 | REV A | 2/2