1 MSPS/500 kSPS, 4-Channel, 16-Bit Dual, Simultaneous Sampling SAR ADCs

FEATURES

- 16-bit dual simultaneous sampling SAR ADC
- Single-ended analog inputs
- 4-channel with 2:1 multiplexers
- Channel sequencer mode
- Throughput rate
  - 1 MSPS (AD4684)
  - 500 kSPS (AD4685)
- SNR (typical)
  - 87.5 dB with V_{REF} = 3.3 V external
  - 93 dB with OSR_MODE = 1, OSR = 8, RES = 1, V_{REF} = 2.5 V internal
- On-chip oversampling functions
- INL ±1.5 LSB (typical)
- Resolution boost function
- 2.5 V internal reference at 10 ppm/°C (maximum)
- Alert function
- −40°C to +125°C temperature range
- 16-lead, 3 mm × 3 mm LFCSP

APPLICATIONS

- Motor control position feedback
- Motor control current sense
- Sonars
- Power quality
- Data acquisition systems
- Erbium doped fiber amplifier (EDFA) applications
- Inphase and quadrature demodulation

GENERAL DESCRIPTION

The AD4684/AD4685 are 16-bit, dual, simultaneous sampling, high speed, successive approximation register (SAR), analog-to-digital converters (ADCs) that operate from a 3.0 V to 3.6 V power supply and feature throughput rates of up to 1 MSPS for the AD4684 and 500 kSPS for the AD4685. The analog input types are single-ended and are sampled and converted on the falling edge of $\overline{CS}$.

The AD4684/AD4685 have an on-chip sequencer and integrated on-chip oversampling block to improve dynamic range and reduce noise at lower bandwidths. A buffered internal 2.5 V reference is included. Alternatively, an external reference up to 3.3 V can be used. The conversion process and data acquisition use standard control inputs, allowing interfacing to microprocessors or digital signal processors (DSPs). The AD4684/AD4685 is compatible with 1.8 V, 2.5 V, and 3.3 V interfaces by using the separate logic supply. The AD4684/AD4685 are available in a 16-lead, 3 mm × 3 mm lead frame chip scale package (LFCSP) with operation specified from −40°C to +125°C.

PRODUCT HIGHLIGHTS

1. 4-channel, dual simultaneous sampling ADC.
2. Pin-compatible product family.
3. High throughput rate: 1 MSPS (AD4684) and 500 kSPS (AD4685).
4. Space-saving, 16-lead, 3 mm × 3 mm LFCSP.
5. Integrated oversampling block to increase dynamic range and SNR and to reduce SCLK speed requirements.
6. Single-ended analog inputs.
7. Small sampling capacitor reduces amplifier drive burden.

FUNCTIONAL BLOCK DIAGRAM

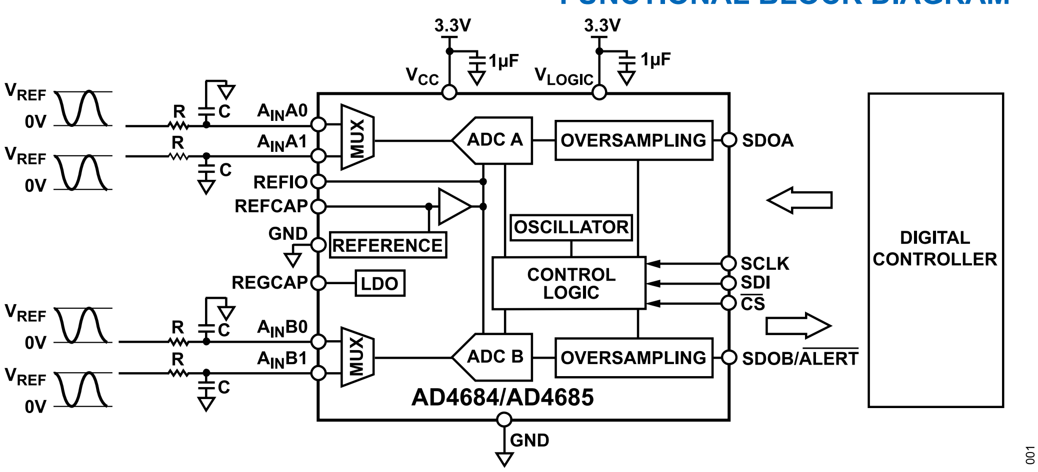

Figure 1. Functional Block Diagram

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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7/2022—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, reference voltage (V_{REF}) = 2.5 V internal, sampling frequency (f_{SAMPLE}) = 1 MSPS (AD4684) or 500 kSPS (AD4685), T_A = −40°C to +125°C, and no oversampling enabled, unless otherwise noted. R = 100 Ω (series with SDOA pin and SDOB pin).

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
THROUGHPUT					
Single Channel Pair	SEQ = 0				
	AD4684			1	MSPS
	AD4685			500	kSPS
Alternating Channels	SEQ = 1				
	AD4684			500	kSPS
	AD4685			250	kSPS
DC ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity (DNL)		−1.0	±0.5	+1.0	LSB
Integral Nonlinearity (INL)		−3.5	±1.5	+3.5	LSB
Gain Error		−0.025	±0.006	+0.025	%FS
Gain Error Temperature Drift		−3	±1	+3	ppm/°C
Gain Error Match		−0.025	±0.006	+0.025	%FS
Offset Error		−0.6	±0.1	+0.6	mV
Offset Error Temperature Drift		−3	±1	+3	µV/°C
Offset Error Match		−0.5	0.12	+0.5	mV
AC ACCURACY	Input frequency (f_{IN}) = 1 kHz				
Dynamic Range	V_{REF} = 3.3 V external		87.8		dB
			86		dB
Oversampled Dynamic Range	OSR_MODE = 1, OSR = 4, RES = 1		91.5		dB
Signal-to-Noise Ratio (SNR)	V_{REF} = 3.3 V external	85.5	87.5		dB
		83.5	85.5		dB
	OSR_MODE = 1, OSR = 8, RES = 1		93		dB
	f_{IN} = 100 kHz		85.3		dB
Spurious-Free Dynamic Range (SFDR)			−100		dB
Total Harmonic Distortion (THD)	V_{REF} = 3.3 V external		−99		dB
			−98		dB
	f_{IN} = 100 kHz		−96		dB
Signal-to-Noise-and-Distortion (SINAD)	V_{REF} = 3.3 V	85	87.4		dB
		83	85.5		dB
Channel to Channel Isolation			−109.7		dB
Channel to Channel Memory			−93.5		dB
ANALOG INPUT					
Voltage Input Range		0		V_{REF}	V
DC Leakage Current			0.1	1	µA
Input Capacitance	When in track mode		18		pF
	When in hold mode		5		pF
SAMPLING DYNAMICS					
Input Bandwidth	At −0.1 dB		5.3		MHz
	At −3 dB		22		MHz
Aperture Delay			2		ns
Aperture Delay Match			300	450	ps
Aperture Jitter			20		ps

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REFERENCE INPUT AND OUTPUT					
V_{REF} Input	External reference				
Voltage Range		2.49		3.4	V
Current			0.47	0.51	mA
V_{REF} Output Voltage	At 25°C	2.498	2.5	2.502	V
	−40°C to +125°C	2.496	2.5	2.505	V
V_{REF} Temperature Coefficient			1	10	ppm/°C
V_{REF} Noise			7		μV rms
DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$)					
Logic Levels					
Input Voltage					
Low (V_{IL})				0.2 × V_{LOGIC}	V
High (V_{IH})		0.8 × V_{LOGIC}			V
Input Current					
Low (I_{IL})		−1		+1	μA
High (I_{IH})		−1		+1	μA
DIGITAL OUTPUTS (SDOA, SDOB/$\overline{ALERT}$)					
Output Voltage					
Low (V_{OL})	Sink current (I_{SINK}) = 300 μA			0.4	V
High (V_{OH})	Source current (I_{SOURCE}) = −300 μA	V_{LOGIC} − 0.3			V
Floating State					
Leakage Current				±1	μA
Output Capacitance			10		pF
POWER SUPPLIES					
V_{CC}					
		3.0	3.3	3.6	V
	External reference = 3.3 V	3.2	3.3	3.6	V
V_{LOGIC}		1.65		3.6	V
V_{CC} Current (I_{VCC})					
Normal Mode (Operational)	AD4684, 1 MSPS		7	8.5	mA
	AD4685, 500 kSPS		5	6	mA
Normal Mode (Static)			2.2	3	mA
Shutdown Mode			100	200	μA
V_{LOGIC} Current (I_{VLOGIC})					
Normal Mode (Operational)	SDOA and SDOB at 0x1FFF		0.8	1	mA
Normal Mode (Static)			10	200	nA
Shutdown Mode			10	200	nA
Power Dissipation					
Total Power (P_{TOTAL}) (Operational)			27	35	mW
V_{CC} Power (P_{VCC})					
Normal Mode (Operational)	AD4684, 1 MSPS		24	31	mW
	AD4685, 500 kSPS		17	22	mW
Normal Mode (Static)			7.3	10.8	mW
Shutdown Mode			330	720	μW
V_{LOGIC} Power (P_{VLOGIC})					
Normal Mode (Operational)	SDOA and SDOB at 0x1FFF		2.6	3.6	mW
Normal Mode (Static)			33	720	nW
Shutdown Mode			33	720	nW

SPECIFICATIONS

TIMING SPECIFICATIONS

V_{CC} = 3.0 V to 3.6 V, V_{LOGIC} = 1.65 V to 3.6 V, V_{REF} = 2.5 V internal, and T_A = −40°C to +125°C, unless otherwise noted. All specifications include a 10 pF load.

Table 2. Timing Specifications

Parameter	Min	Typ	Max	Unit	Description
t_{CYC}					Time between conversions
	1			µs	AD4684
	2			µs	AD4685
	2			µs	AD4684 alternating conversion channels
	4			µs	AD4685 alternating conversion channels
t_{SCLKED}	0.8			ns	$\overline{CS}$ falling edge to first SCLK falling edge
t_{SCLK}	25			ns	SCLK period
t_{SCLKH}	10			ns	SCLK high time
t_{SCLKL}	10			ns	SCLK low time
t_{CSH}	10			ns	$\overline{CS}$ pulse width
t_{QUIET}	10			ns	Interface quiet time prior to conversion
t_{SDOEN}					$\overline{CS}$ low to SDOA and SDOB/$\overline{ALERT}$ enabled
			6	ns	V_{LOGIC} ≥ 2.25 V
			8	ns	1.65 V ≤ V_{LOGIC} < 2.3 V
t_{SDOH}	2			ns	SCLK rising edge to SDOA and SDOB/$\overline{ALERT}$ hold time
t_{SDOS}					SCLK rising edge to SDOA and SDOB/$\overline{ALERT}$ setup time
			6	ns	V_{LOGIC} ≥ 2.25 V
			8	ns	1.65 V ≤ V_{LOGIC} < 2.3 V
t_{SDOT}			8	ns	$\overline{CS}$ rising edge to SDOA and SDOB/$\overline{ALERT}$ high impedance
t_{SDIS}	1			ns	SDI setup time prior to SCLK falling edge
t_{SDIH}	1			ns	SDI hold time after SCLK falling edge
t_{SCLKCS}	0			ns	SCLK rising edge to $\overline{CS}$ rising edge
$t_{CONVERT}$			190	ns	Conversion time
t_{RESET}					Valid time to start conversion after software reset (see Figure 41)
		250		ns	Valid time to start conversion after soft reset
		800		ns	Valid time to start conversion after hard reset
$t_{ACQUIRE}$					Acquire time
	850/1700			ns	AD4684 single channel/alternating channel
	1850/3700			ns	AD4685 single channel/alternating channel
$t_{POWERUP}$					Supply active to conversion
			5	ms	First conversion allowed
			11	ms	Settled to within 1% with internal reference
			5	ms	Settled to within 1% with external reference
$t_{REGWRITE}$			5	ms	Supply active to register read write access allowed
$t_{STARTUP}$					Exiting power-down mode to conversion (see Figure 40)
			11	ms	Settled to within 1% with internal reference
			10	µs	Settled to within 1% with external reference
t_{ALERTS}			200	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ indication (see Figure 39)
t_{ALERTC}			12	ns	Time from $\overline{CS}$ to $\overline{ALERT}$ clear (see Figure 39)

SPECIFICATIONS

Timing Diagrams

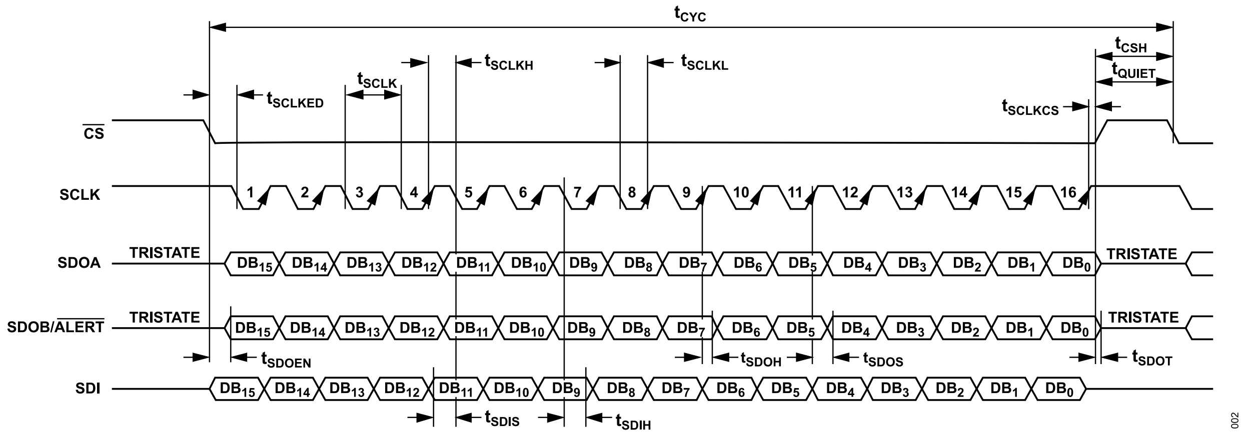


Figure 2. Serial Interface Timing Diagram

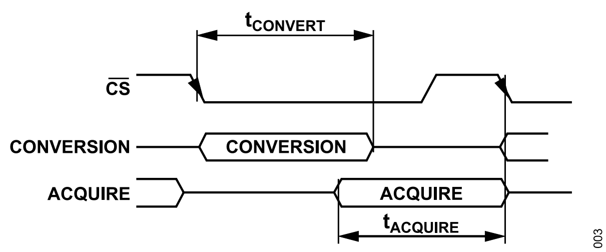


Figure 3. Internal Conversion Acquire Timing

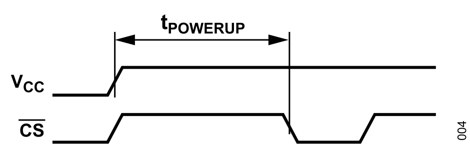


Figure 4. Power-Up Time to Conversion

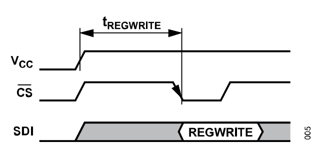


Figure 5. Power-Up Time to Register Read Write Access

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
V_{CC} to GND	–0.3 V to +4 V
V_{LOGIC} to GND	–0.3 V to +4 V
Analog Input Voltage to GND	–0.3 V to V_{REF} + 0.3 V, V_{CC} + 0.3 V or 4 V
Digital Input Voltage to GND	–0.3 V to V_{LOGIC} + 0.3 V or 4 V
Digital Output Voltage to GND	–0.3 V to V_{LOGIC} + 0.3 V or 4 V
REFIO Input to GND	–0.3 V to V_{CC} + 0.3 V or 4 V
Input Current to Any Pin Except Supplies	±10 mA
Temperature	
Operating Range	–40°C to +125°C
Storage Range	–65°C to +150°C
Junction	150°C
Pb-Free Soldering Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-16-45[1]	55.4	12.7	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

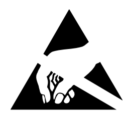
Field induced charge device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4684/AD4685

Table 5. AD4684/AD4685, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±4000	3A
FICDM	±1250	C3

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

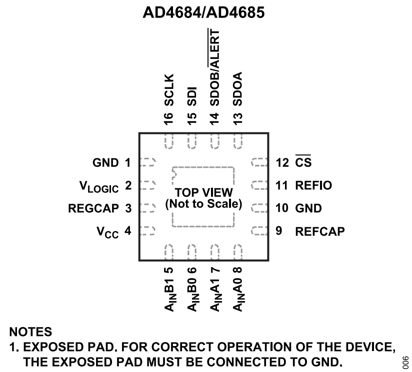


Figure 6. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10	GND	Ground Reference Point. These pins are the ground reference points for all circuitry on the device.
2	V_{LOGIC}	Logic Interface Supply Voltage, 1.65 V to 3.6 V. Decouple this pin to GND with a 1 µF capacitor.
3	REGCAP	Decoupling Capacitor Pin for Voltage Output from Internal Regulator. Decouple this pin to GND with a 1 µF capacitor. The voltage at this pin is 1.9 V typical.
4	V_{CC}	Power Supply Input Voltage, 3.0 V to 3.6 V. Decouple this pin to GND using a 1 µF capacitor.
5, 6	$A_{IN}B1$, $A_{IN}B0$	Analog Inputs of ADC B.
7, 8	$A_{IN}A1$, $A_{IN}A0$	Analog Inputs of ADC A.
9	REFCAP	Decoupling Capacitor Pin for Band Gap Reference. Decouple this pin to GND with a 0.1 µF capacitor. The voltage at this pin is 2.5 V typical. If the device is configured for external reference operation, the 0.1 µF capacitor is not required.
11	REFIO	Reference Input/Output. The on-chip reference of 2.5 V is available as an output on this pin for external use if the device is configured accordingly. Alternatively, an external reference of 2.5 V to 3.3 V can be input to this pin. The REFSEL bit in the CONFIGURATION1 register must be set correctly when choosing the reference voltage source. Decoupling is required on this pin for both the internal and external reference options. A 1 µF capacitor must be applied from this pin to GND.
12	$\overline{CS}$	Chip Select Input. Active low, logic input. This input provides the dual function of initiating conversions and framing the serial data transfer.
13	SDOA	Serial Data Output A. This pin functions as a serial data output pin to access the ADC A or ADC B conversion results or data from any of the on-chip registers.
14	SDOB/$\overline{ALERT}$	Serial Data Output B (SDOB). This pin functions as a serial data output pin to access the ADC B conversion results. Alert Indication Output ($\overline{ALERT}$). This pin operates as an alert pin going low to indicate that a conversion result exceeded a configured threshold.
15	SDI	Serial Data Input. This input provides the data written to the on-chip control registers.
16	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC.
	EPAD	Exposed Pad. For correct operation of the device, the exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

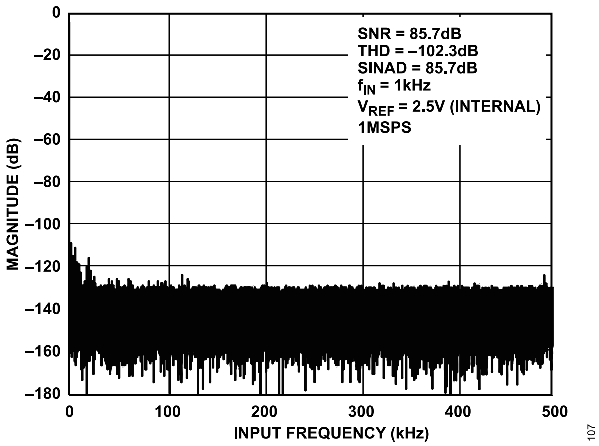


Figure 7. AD4684 Fast Fourier Transform (FFT), V_{REF} = 2.5 V (Internal)

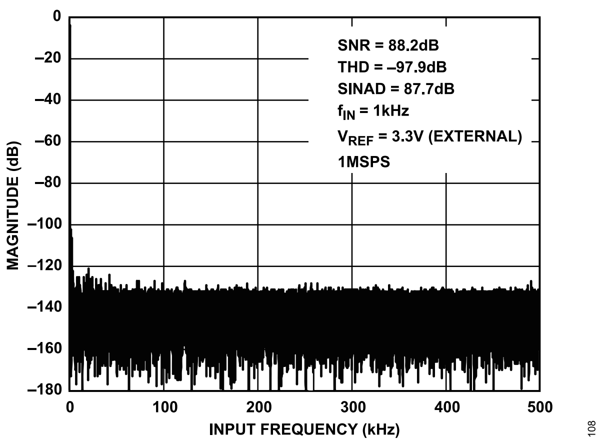


Figure 8. AD4684 FFT, V_{REF} = 3.3 V (External)

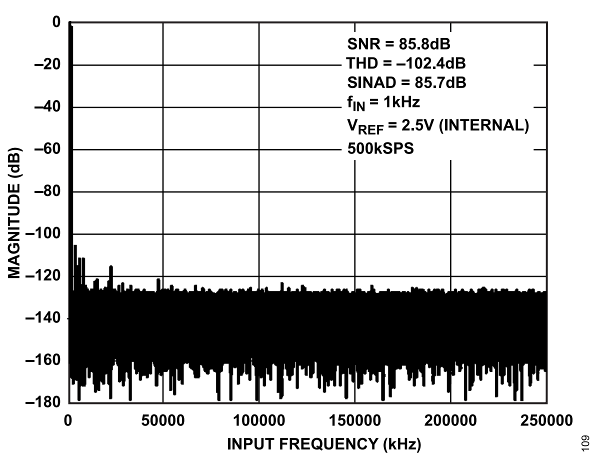


Figure 9. AD4685 FFT, V_{REF} = 2.5 V (Internal)

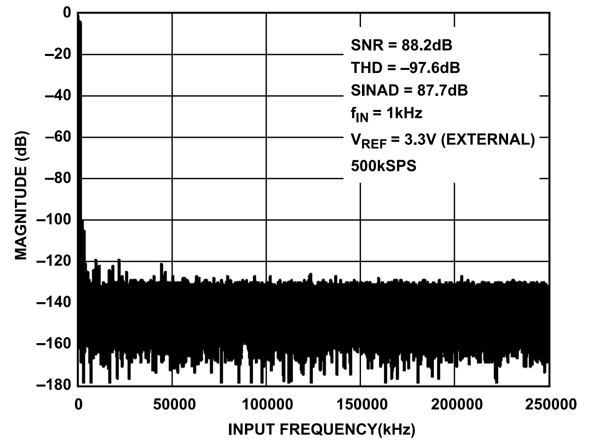


Figure 10. AD4685 FFT, V_{REF} = 3.3 V (External)

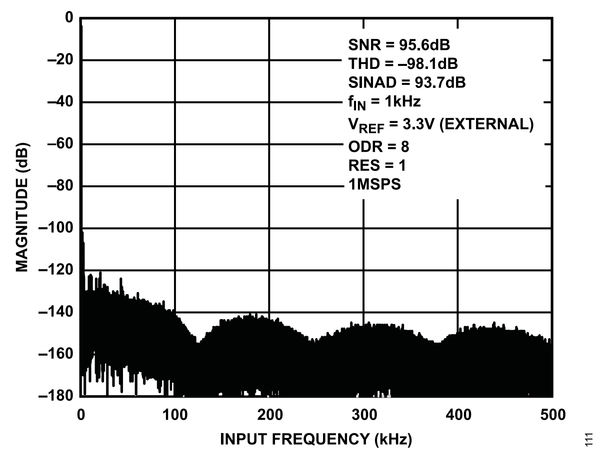


Figure 11. AD4684 FFT with Oversampling

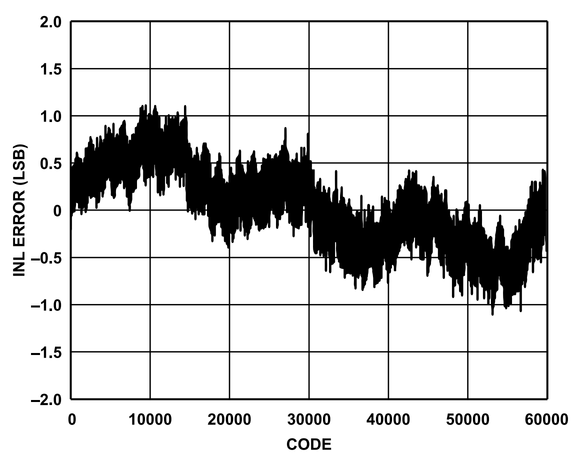


Figure 12. INL Error

TYPICAL PERFORMANCE CHARACTERISTICS

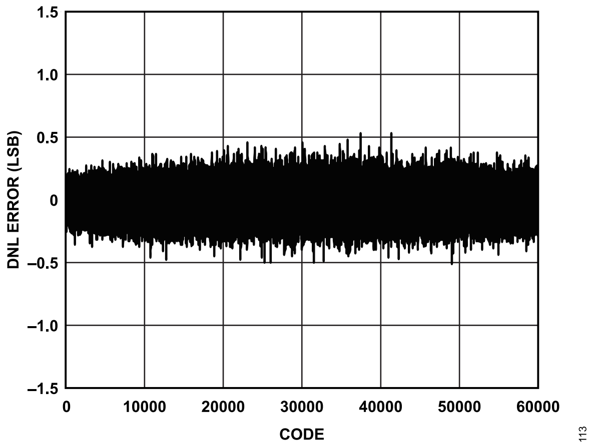


Figure 13. DNL Error

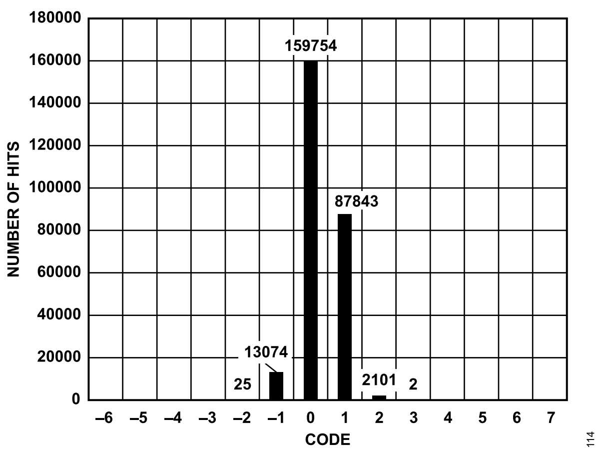


Figure 14. DC Histogram Codes at Code Center

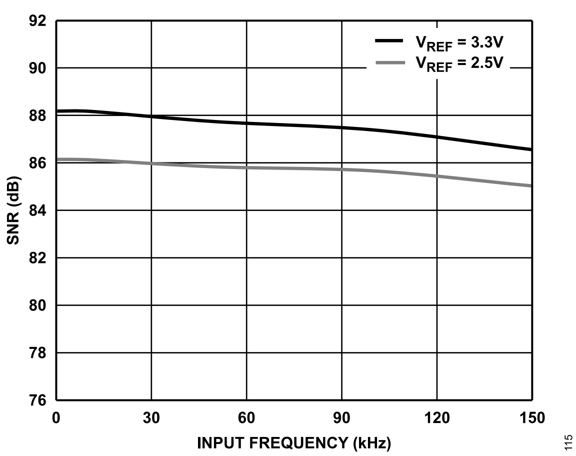


Figure 15. AD4684 SNR vs. Input Frequency

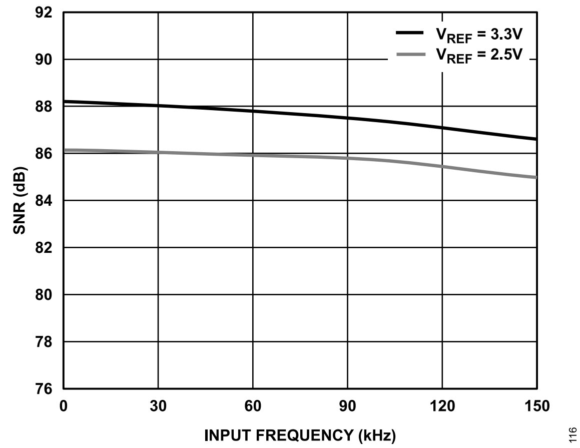


Figure 16. AD4685 SNR vs. Input Frequency

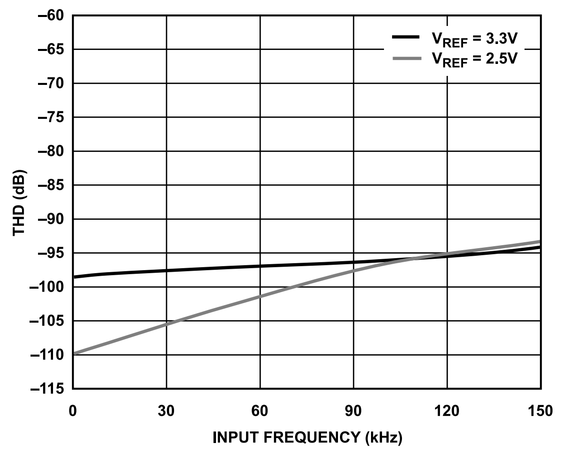


Figure 17. AD4684 THD vs. Input Frequency

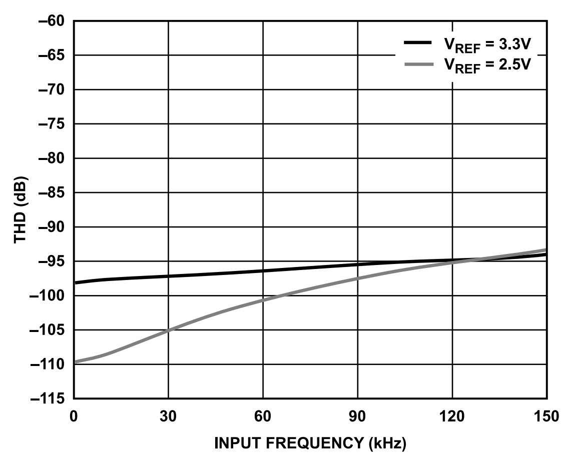


Figure 18. AD4685 THD vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

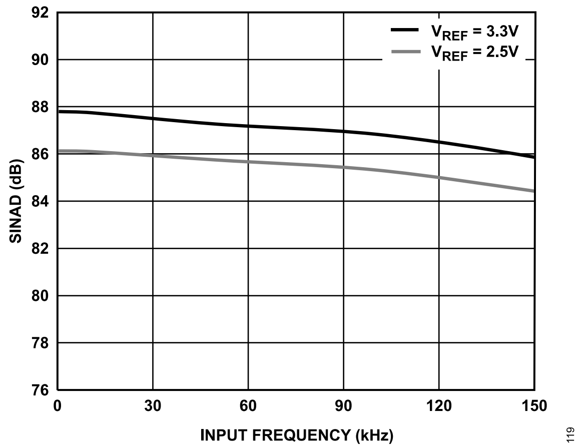


Figure 19. AD4684 SINAD vs. Input Frequency

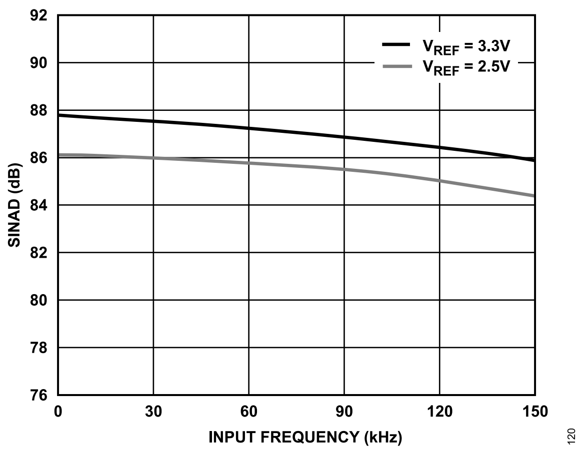


Figure 20. AD4685 SINAD vs. Input Frequency

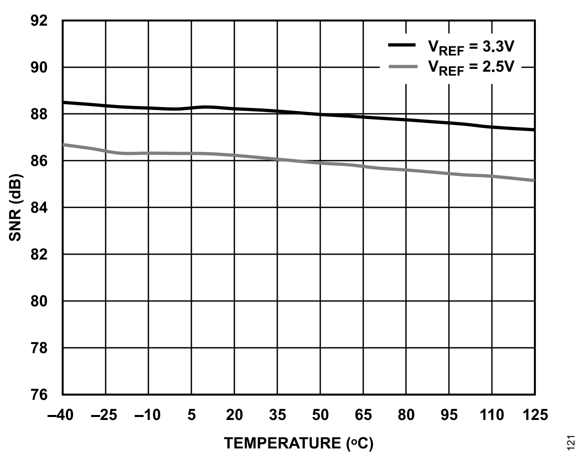


Figure 21. AD4684 SNR vs. Temperature

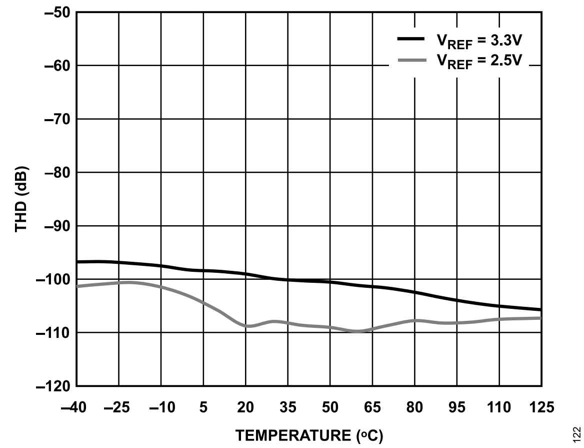


Figure 22. AD4684 THD vs. Temperature

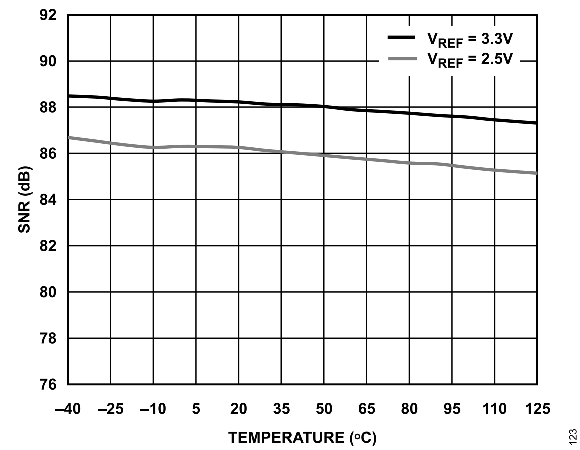


Figure 23. AD4685 SNR vs. Temperature

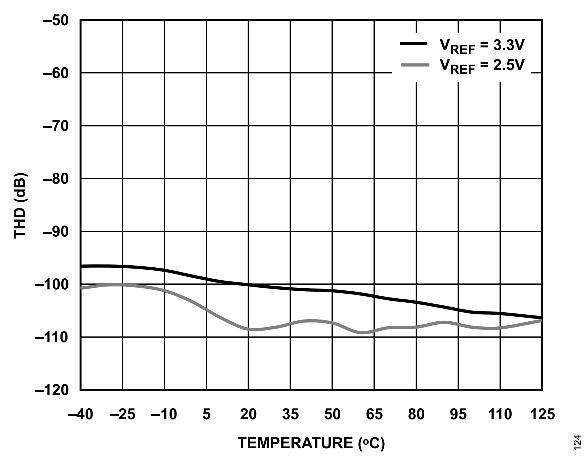


Figure 24. AD4685 THD vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

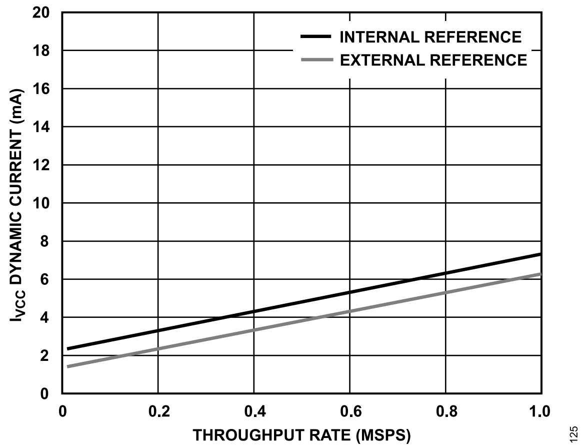


Figure 25. I_{VCC} Dynamic Current vs. Throughput Rate

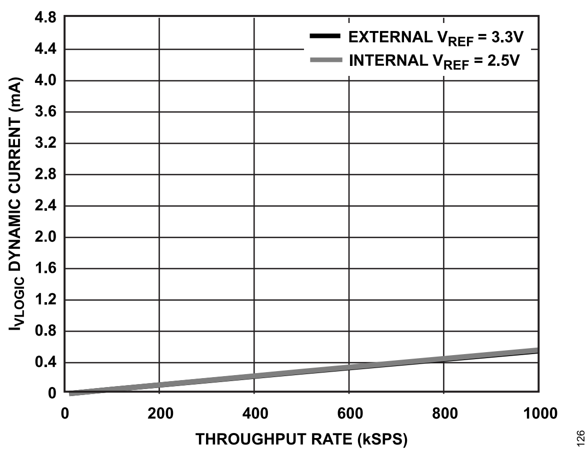


Figure 26. I_{VLOGIC} Dynamic Current vs. Throughput Rate

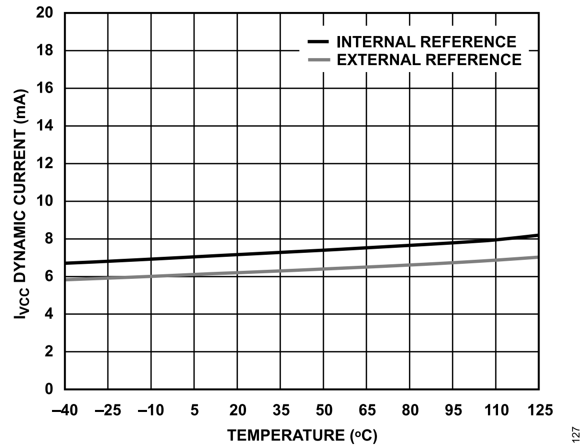


Figure 27. I_{VCC} Dynamic Current vs. Temperature

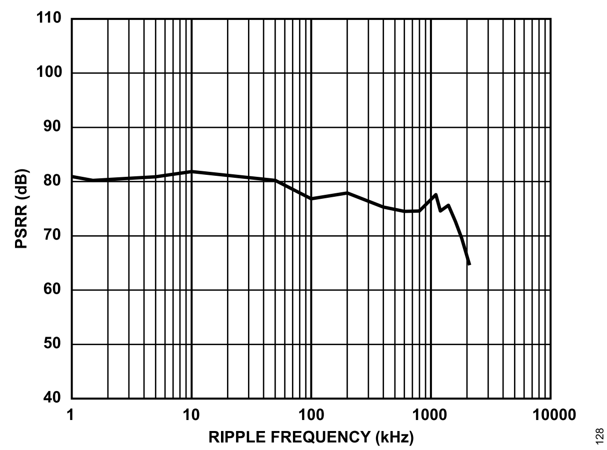


Figure 28. PSRR vs. Ripple Frequency

TERMINOLOGY

Differential Nonlinearity (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Integral Nonlinearity (INL)

INL is the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Gain Error

The first transition (from 000…000 to 000…001) must occur at a level ½ LSB above nominal negative full scale. The last transition (from 111…110 to 111…111) occurs for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

Gain Error Temperature Drift

The gain error change due to a temperature change of 1°C.

Gain Error Match

Gain error match is the difference in negative full-scale error between the input channels and the difference in positive full-scale error between the input channels.

Offset Error

The first transition must occur at a level ½ LSB above analog ground. The offset error is the deviation of the actual transition from that point.

Offset Error Temperature Drift

The zero error change due to a temperature change of 1°C.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Channel to Channel Memory

Channel to channel memory is a measure of the level of crosstalk between channels in sequencer mode. It is measured by applying a full-scale signal of a specific frequency in one analog input channel of the ADC and determining how much that signal is attenuated in the alternate ADC channel, when a full-scale signal of different frequency is applied. The figure given is the typical value in decibels and is measured for both ADC A and ADC B.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to the change in the power supply voltage from the nominal value. PSRR is the ratio of power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the V_{CC} supply of the ADC of the FS frequency.

$$PSRR\ (\text{dB}) = 10\log(Pf/Pfs)$$

where:
Pf is equal to the power at f in the ADC output.
Pfs is equal to the power at full-scale coupled onto the V_{CC} supply.

Aperture Delay

Aperture delay is the measure of the acquisition performance and is the time between the falling edge of the $\overline{CS}$ input and when the input signal is held for a conversion.

Aperture Jitter

Aperture jitter is the variation in aperture delay.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD4684/AD4685 are high speed, 4-channel, dual, simultaneous sampling, single-ended, 16-bit SAR ADCs. The devices operate from a 3.3 V power supply and feature throughput rates of up to 1 MSPS for the AD4684 and 500 kSPS for the AD4685.

The AD4684/AD4685 contain two SAR ADCs, a multiplexer, a sequencer, and a serial interface with two separate data output pins. The devices are housed in a 16-lead LFCSP, offering the user considerable space-saving advantages over alternative solutions.

Data is accessed from the device via the serial interface. The interface can operate with one or two serial outputs. The AD4684/AD4685 have an on-chip, 2.5 V internal reference, V_{REF}. If an external reference is desired, the internal reference buffer can be disabled and a reference value ranging from 2.5 V to 3.3 V can be supplied. If the internal reference is used elsewhere in the system, the reference output must be buffered. The analog input range for the AD4684/AD4685 is 0 V to V_{REF}.

The AD4684/AD4685 feature an on-chip oversampling block to improve performance. Rolling average oversampling modes is available. Power-down options to allow power saving between conversions are available. Configuration of the device is implemented via the standard serial interface. See the Interface section for more information.

CONVERTER OPERATION

The AD4684/AD4685 have two SAR ADCs, each based around two capacitive DACs. Figure 29 and Figure 30 show simplified schematics of one of these ADCs in acquisition and conversion phases, respectively. The ADC comprises control logic, an SAR, and two capacitive DACs. In Figure 29 (the acquisition phase), SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor (C_S) array acquires the signal on the input.

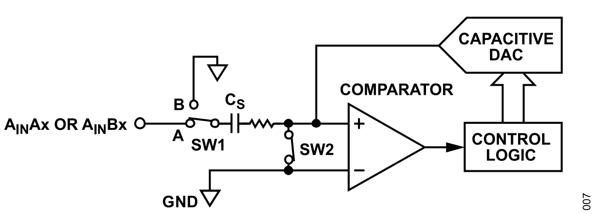


Figure 29. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 30), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the capacitive DAC to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

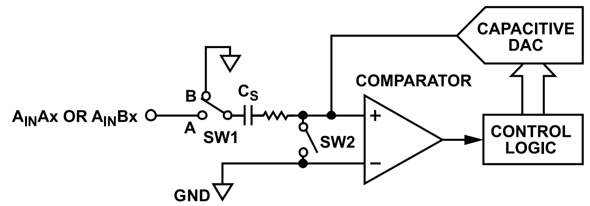


Figure 30. ADC Conversion Phase

ANALOG INPUT STRUCTURE

Figure 31 shows the equivalent circuit of the analog input structure of the AD4684/AD4685. The two diodes provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signals never exceed the supply rails by more than 300 mV. Exceeding the limit causes these diodes to become forward-biased and start conducting into the substrate. These diodes can conduct up to 10 mA without causing irreversible damage to the device.

The C1 capacitor in Figure 31 is typically 3 pF and can primarily be attributed to pin capacitance. The R1 resistor is a lumped component made up of the on resistance of the switches. The value of these resistors is typically about 200 Ω. The C2 capacitor is the sampling capacitor of the ADC with a capacitance of 15 pF, typically.

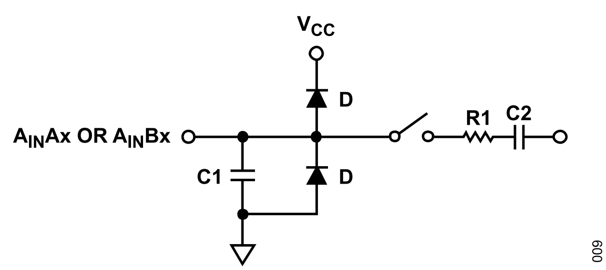


Figure 31. Equivalent Analog Input Circuit, Conversion Phase = Switch Open, Track Phase = Switch Closed

ADC TRANSFER FUNCTION

The AD4684/AD4685 use a 2.5 V to 3.3 V reference. The AD4684/AD4685 convert the voltage of the analog inputs (A_{IN}A0 and A_{IN}A1, A_{IN}B0 and A_{IN}B1) into a digital output.

The conversion result is MSB first, straight binary. The LSB size is $(V_{REF})/2^N$, where N is the ADC resolution. The ADC resolution is determined by the resolution of the device chosen and if resolution boost mode is enabled. Table 7 outlines the LSB size expressed in microvolts for different resolutions and reference voltages options.

The ideal transfer characteristic of the AD4684/AD4685 is shown in Figure 32.

Table 7. LSB Size

Resolution	2.5 V Reference (µV)	3.3 V Reference (µV)
16 Bits	38.1	50.4
18 Bits	9.55	12.6

THEORY OF OPERATION

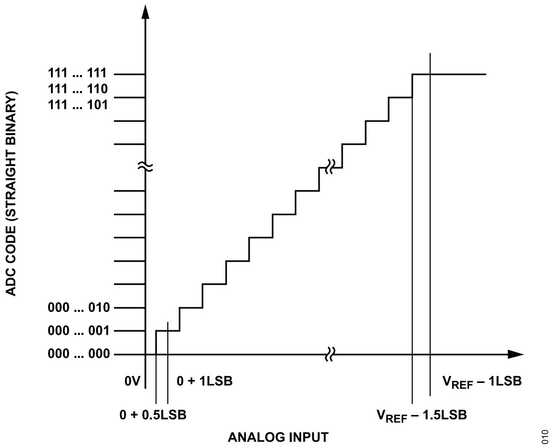


Figure 32. ADC Ideal Transfer Function

APPLICATIONS INFORMATION

Figure 33 shows an example of a complete signal chain connection diagram for the AD4684/AD4685. Decouple the V_{CC}, V_{LOGIC}, REGCAP, and REFIO pins with suitable decoupling capacitors, as shown in Figure 33.

The exposed pad is a ground reference point for circuitry on the device and must be connected to the board ground.

A differential RC filter must be placed on the analog inputs to ensure performance is achieved. For a typical application, the recommended resistor is R = 33 Ω, and C = 330 pF.

The performance of the AD4684/AD4685 can be impacted by noise on the digital interface. This impact is dependent on board layout and design. Keep a minimal distance of the digital line to the digital interface or place a 100 Ω resistor in series and close to the SDOA pin and SDOB/$\overline{\text{ALERT}}$ pin to reduce noise from digital interface coupling of the AD4684/AD4685.

Each of the single-ended analog inputs of the AD4684/AD4685 can accept a voltage from 0 V to V_{REF} and can easily be driven by an amplifier for optimum performance. Table 8 shows the recommended components for the complete signal chain solution that can best fit the application for the AD4684/AD4685.

The AD4684/AD4685 have a buffered internal 2.5 V reference that can be access via the REFIO pin. The buffered internal 2.5 V reference must use an external buffer like the ADA4807, when connecting it to the external circuitry. Both devices have the option to use an ultralow noise, high accuracy voltage reference ranging from 2.5 V to 3.3 V, such as the ADR4525 or ADR4533, as an external voltage source.

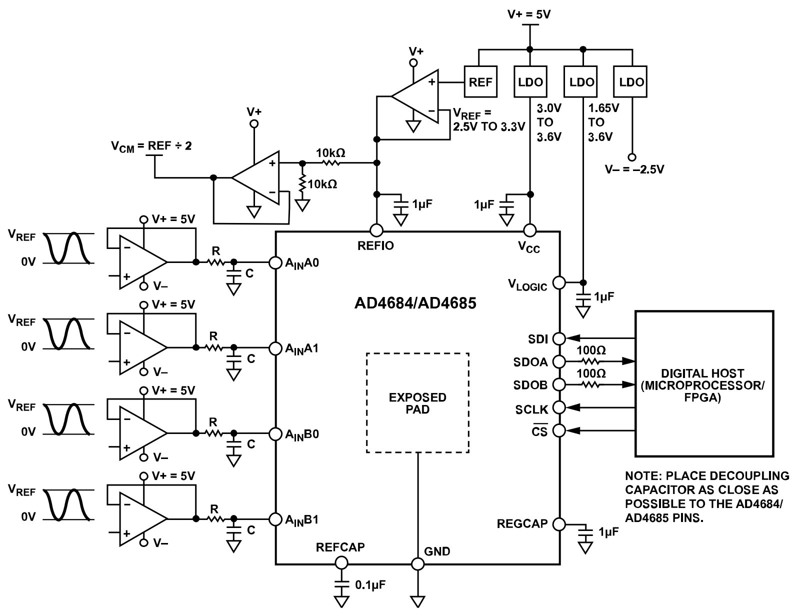


Figure 33. Typical Application Circuit (V_{CM} Is Common-Mode Voltage, See the Power Supply Section for Additional Information on V+ and V−)

Table 8. Signal Chain Components

Companion Devices	Device Name	Description	Typical Application
ADC Driver	ADA4896-2	1 nV/√Hz, rail-to-rail output amplifier	Precision, low noise, high frequency
	ADA4807-2	1 mA, rail-to-rail output amplifier	Precision, low power, high frequency
	ADA4940-2	Ultra low power, fully differential, low distortion	Precision, low density, low power
	LTC6227	Low distortion rail-to-rail output op amps	Precision, low noise, high frequency
External Reference	ADR4525	Ultralow noise, high accuracy, 2.5 V voltage reference	2.5 V reference voltage
	ADR4533	Ultralow noise, high accuracy, 3.3 V voltage reference	3.3 V reference voltage
LDO	ADP166	Low quiescent, 150 mA, LDO regulator	3.0 V to 3.6 V supply for V_{CC} and V_{LOGIC}
	ADP7104	Low noise, CMOS LDO regulator	5 V supply for driver amplifier
	ADP7182	Low noise line regulator	−2.5 V supply for driver amplifier

APPLICATIONS INFORMATION

POWER SUPPLY

The typical application circuit in Figure 33 can be powered by a single 5 V (V+) voltage source that supplies the whole signal chain. The 5 V supply can come from a low noise, CMOS low dropout (LDO) regulator (for example, the ADP7105). The driver amplifier supply is provided by +5 V (V+) and −2.5 V (V−), which is derived from the inverter (for example, the ADM660). The inverter then converts +5 V to −5 V and supplies this voltage to the ADP7182 low noise voltage regulator to output −2.5 V.

The two independent supplies of the AD4684/AD4685, V_{CC} and V_{LOGIC}, that supply the analog circuitry and digital interface, respectively, can be supplied by a low quiescent current LDO regulator like the ADP166. The ADP166 is a suitable supply with a fixed output voltage range from 1.2 V to 3.3 V for typical V_{CC} and V_{LOGIC} levels. Decouple both the V_{CC} supply and the V_{LOGIC} supply separately with a 1 µF capacitor, placed close to the AD4684/AD4685 and connected using short and wide traces, to provide low impedance paths and reduce the glitches in the power supply lines. Additionally, there is an internal LDO regulator to supply the AD4684/AD4685. The on-chip regulator provides a 1.9 V supply for internal use on the device only. Decouple the REGCAP pin with a 1 µF capacitor to GND with short and wide traces and place the capacitor close to the AD4684/AD4685 REGCAP and GND pins.

Power-Up

The AD4684/AD4685 are not easily damaged in power supply sequencing. V_{CC} and V_{LOGIC} can be applied in any sequence. An external reference must be applied after V_{CC} and V_{LOGIC} are applied. Analog and digital signals must be applied after the external reference is applied.

The AD4684/AD4685 require a $t_{POWERUP}$ time from applying V_{CC} and V_{LOGIC} until the ADC conversion results are stable. Figure 4 shows the recommended power-up timing and condition with $\overline{CS}$ held high. It is recommended and a good practice to perform a software reset after power-up. See the Software Reset section for details.

MODES OF OPERATION

The AD4684/AD4685 have several on-chip configuration registers for controlling the operational mode of the device.

CHANNEL SELECTION

The ADC channel pairs for conversion (A_{IN}A0 and A_{IN}B0, A_{IN}A1 and A_{IN}B1) are selected by setting the CH bit in the CONFIGURATION1 register. If the CH bit is set to 0, the A_{IN}A0 and A_{IN}B0 channels simultaneously convert. Alternatively, if the CH bit is set to 1, the A_{IN}A1 and A_{IN}B1 channels are selected for simultaneous conversion.

If the channel to convert is changing, the ADC requires additional settling time. The maximum throughput rate when changing between the A_{IN}x0 and A_{IN}x1 channels is 500 kSPS for the AD4684 and 250 kSPS for the AD4685.

SEQUENCER

The AD4684/AD4685 can be configured to automatically cycle through the A_{IN}x0 and A_{IN}x1 channels using the on-chip sequencer. The sequencer is controlled via the SEQ bit in the CONFIGURATION1 register. If the SEQ bit is set to 0, the sequencer is disabled. If SEQ is set to 1, the sequencer is enabled. The CH bit is not queried for the sequencer mode. The sequencer always starts at the A_{IN}x0 channels and then moves to the A_{IN}x1 channels. After converting the A_{IN}x1 channel, the sequencer loops back to the A_{IN}x0 channels and the sequence restarts.

If the channel to convert is changing, the ADC requires additional settling time. The maximum throughput rate when changing between A_{IN}x0 and A_{IN}x1 channels is 500 kSPS for the AD4684 and 250 kSPS for the AD4685.

Figure 34 shows the manual channel selection setup, and Figure 35 shows the channel sequencer setup.

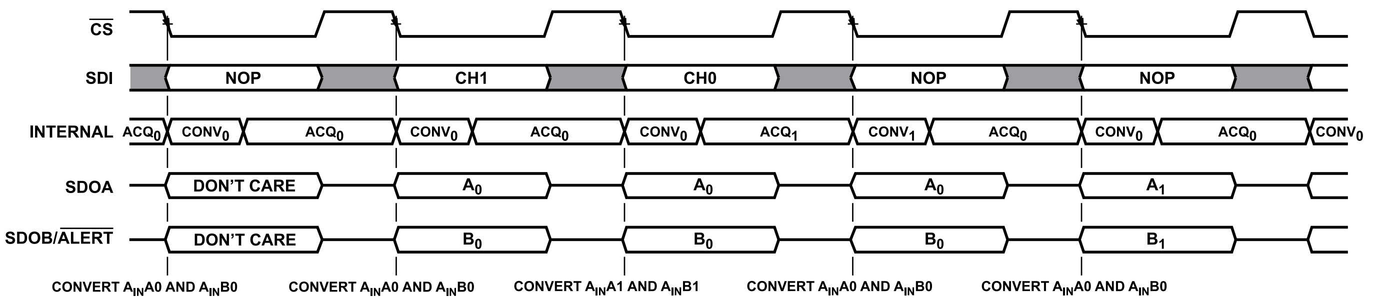


Figure 34. Manual Channel Selection Setup

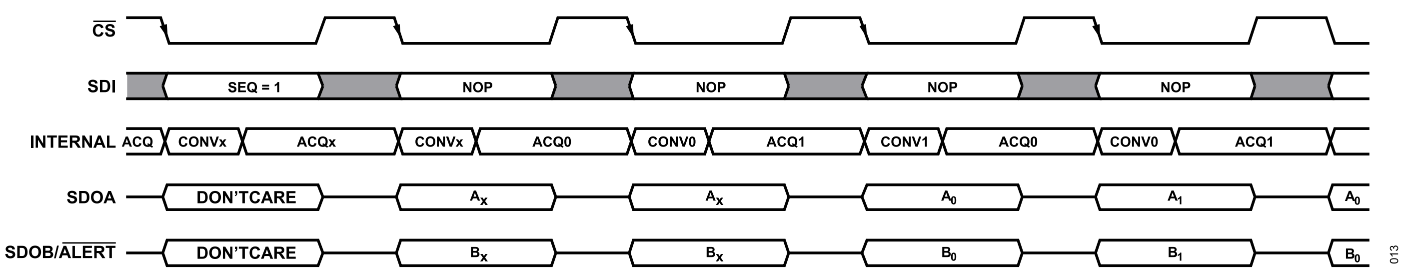


Figure 35. Channel Sequencer Setup

MODES OF OPERATION

OVERSAMPLING

Oversampling is a common method used in analog electronics to improve the accuracy of the ADC result. Multiple samples of the analog input are captured and averaged to reduce the noise component from quantization noise and thermal noise (kTC) of the ADC. The AD4684/AD4685 offer a rolling average oversampling function on chip.

The rolling average oversampling functionality is enabled by writing a 1 on the OS_MODE bit and a valid nonzero value on OSR, Bits[2:0], in the CONFIGURATION1 register. Oversampling can be disabled by writing 0 on the OS_MODE bit and a zero value on OSR, Bits[2:0] in the CONFIGURATION1 register.

Rolling Average Oversampling

Rolling average oversampling mode can be used in applications where higher output data rates are required and where higher SNR or dynamic range is desirable. Rolling average oversampling involves taking a number of samples, adding the samples together, and dividing the result by the number of samples taken. This result is then output from the device. The sample data is not cleared when the process is completed. The rolling oversampling mode uses a first in, first out (FIFO) buffer of the most recent samples in the averaging calculation, allowing the ADC throughput rate and output data rate to stay the same. Rolling average oversampling mode is configured by setting the OS_MODE bit to Logic 1 and having a valid nonzero value in the OSR bits. The oversampling ratio of the digital filter is controlled using the OSR bits. Table 9 provides the oversampling bit decoding to select the different oversample rates. The output result is decimated to 16-bit resolution for the AD4684/AD4685. If additional resolution is required, this resolution can be achieved by configuring the RES bit in the CONFIGURATION1 register. See the Resolution Boost section for further details.

In rolling average oversampling mode, all ADC conversions are controlled and initiated by the falling edge of $\overline{CS}$. When a conversion is complete, the result is loaded into the FIFO. The FIFO length is eight regardless of the oversampling ratio set. The FIFO is filled on the first conversion after a power-on reset (POR), the first conversion after a software controlled hard or soft reset, or the first conversion after the REFSEL bit is toggled. A new conversion result is shifted into the FIFO on completion of every ADC conversion, regardless of the status of the OSR bits and the OS_MODE bit. This shift allows a seamless transition from no oversampling to rolling average oversampling, or different rolling average oversampling ratios without waiting for the FIFO to fill.

The number of samples, n, defined by the OSR bits, are taken from the FIFO, added together, and the result is divided by n. The time between $\overline{CS}$ falling edges is the cycle time that can be controlled by the user, depending on the desired data output rate.

Figure 36 shows the rolling average oversampling mode configuration.

Table 9. Rolling Average Oversampling Overview for the AD4684

		SNR (dB Typical)			
		V_{REF} = 2.5 V		V_{REF} = 3.3 V	
Oversampling Ratio	Throughput Rate (kSPS)	RES = 0	RES = 1	RES = 0	RES = 1
Disabled	1000	86.1	86.1	88.1	88.2
2	1000	87.9	88.3	89.4	89.9
4	1000	90.5	91.3	91.8	92.8
8	1000	92.8	94.2	93.7	95.6

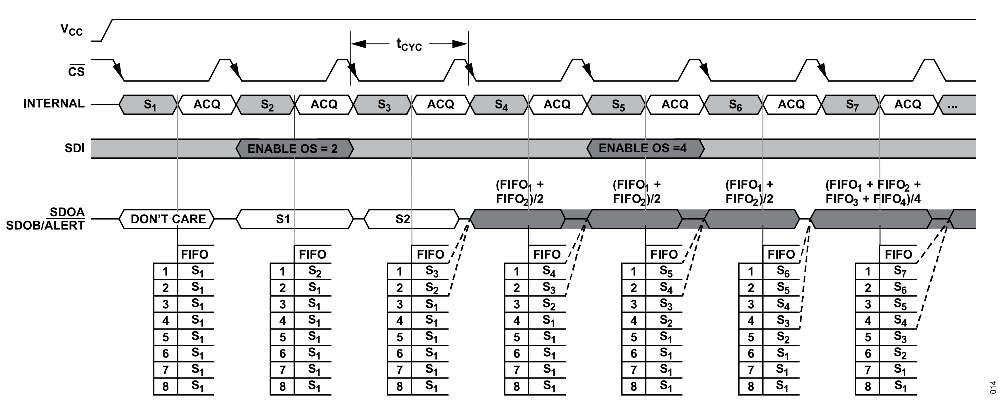


Figure 36. Rolling Average Oversampling Mode Configuration

MODES OF OPERATION

Oversampling in Sequencer Mode

While in sequencer mode, oversampling on the $A_{IN}x0$ and $A_{IN}x1$ channels can be performed in the AD4684/AD4685. There is a two-cycle latency before the register update and start conversion in oversampling mode and the AD4684/AD4685 automatically cycle through $A_{IN}x0$ and $A_{IN}x1$. Figure 37 shows the timing diagram of the rolling average oversampling in sequencer mode.

To perform oversampling in sequencer mode, write a nonzero value to enable the OSR bits in the CONFIGURATION1 register to select the number of samples to average. In addition, set the OS_MODE bit to 1, while simultaneously setting the SEQ bit in the CONFIGURATION1 register to 1.

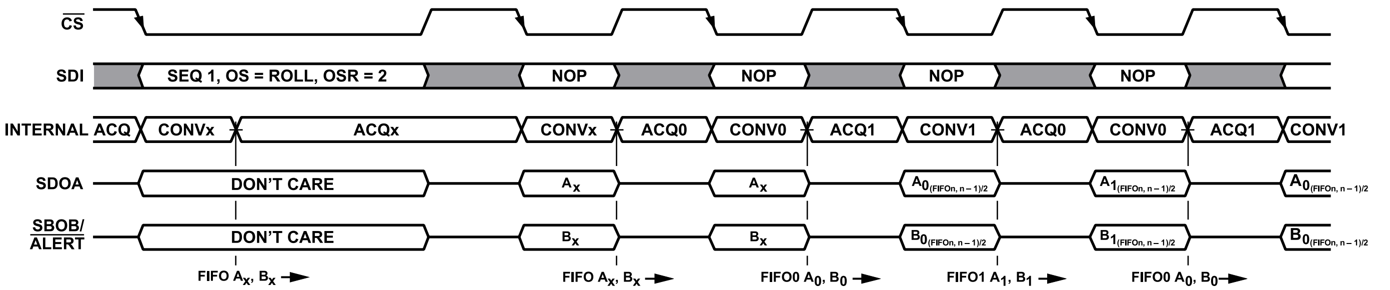


Figure 37. Rolling Average Oversampling Sequencer Mode

MODES OF OPERATION

RESOLUTION BOOST

The default conversion result output data size for the AD4684/ AD4685 is 16 bits. When the on-chip oversampling function is enabled, the performance of the ADC can exceed the 16-bit level. To accommodate the performance boost, it is possible to enable an additional two bits of resolution. If the RES bit in the CONFIGURATION1 register is set to Logic 1, and the AD4684/AD4685 are in a valid oversampling mode, the conversion result size is 18 bits for the AD4684/AD4685. In this mode, 18 SCLK cycles are required to propagate the data for the AD4684/AD4685. Figure 38 shows the resolution boost diagram.

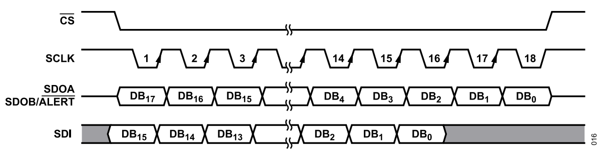


Figure 38. Resolution Boost

ALERT

The alert functionality is an out of range indicator and can be used as an early indicator of an out of bounds conversion result. An alert event triggers when the conversion result value register exceeds the alert high limit value in the ALERT_HIGH_THRESHOLD register, or falls below the alert low limit value in the ALERT_LOW_THRESHOLD register. The ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register are common to all ADCs. Detailed alert information is accessible in the Alert Register section. The register contains two status bits per ADC, one corresponding to the high limit and the other to the low limit. A logical OR of alert signals for all ADCs creates a common alert value. This value can be configured to drive out on the $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin. The SDOB/$\overline{\text{ALERT}}$ pin is configured as $\overline{\text{ALERT}}$ by configuring the following bits in the CONFIGURATION1 register and the CONFIGURATION2 register:

- Set the SDO bit to 1.
- Set the ALERT_EN bit to 1.

In addition, set a valid value to the ALERT_HIGH_THRESHOLD register and the ALERT_LOW_THRESHOLD register.

The alert indication function is available in oversampling and in nonoversampling modes.

The $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin is updated at the end of conversion. The alert indication status bits in the alert register update as well and must be read before the end of the next conversion. The $\overline{\text{ALERT}}$ function of the SDOB/$\overline{\text{ALERT}}$ pin is cleared with a falling edge of $\overline{\text{CS}}$. Issuing a software reset also clears the alert status in the alert register.

Figure 39 shows the alert operation.

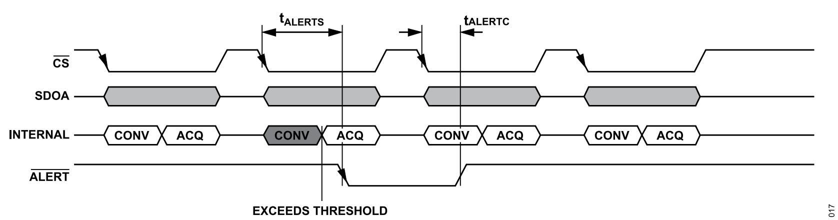


Figure 39. Alert Operation

MODES OF OPERATION

POWER MODES

The AD4684/AD4685 have two power modes, normal mode and power-down mode. These modes of operation provide flexible power management options, allowing optimization of the power dissipation and throughput rate ratio for different application requirements.

Program the PMODE bit in the CONFIGURATION1 register to configure the power modes in the AD4684/AD4685. Set PMODE to Logic 0 for normal mode and Logic 1 for power-down mode.

Normal Mode

Keep the AD4684/AD4685 in normal mode to achieve the fastest throughput rate. All blocks within the AD4684/AD4685 remain fully powered at all times, and an ADC conversion can be initiated by a falling edge of $\overline{CS}$ when required. When the AD4684/AD4685 are not converting, the devices are in static mode and power consumption automatically reduces. Additional current is required to perform a conversion. Therefore, power consumption of the AD4684/AD4685 scales with throughput.

Power-Down Mode

When slower throughput rates and lower power consumption are required, use power-down mode by either powering down the ADC between each conversion, or by performing a series of conversions at a high throughput rate and then powering down the ADC for a relatively long duration, depending on the user application, between these burst conversions. When the AD4684/AD4685 are in power-down mode, all analog circuitry powers down, including the internal reference, if enabled. The serial interface remains active during power-down mode to allow the AD4684/AD4685 to exit power-down mode.

To enter power-down mode, write to the power mode configuration bit, PMODE, in the CONFIGURATION1 register to a Logic 1. The AD4684/AD4685 shut down and current consumption reduces.

To exit power-down mode and return to normal mode, set the PMODE bit in the CONFIGURATION1 register to Logic 0. All register configuration settings remain unchanged entering or leaving power-down mode. After exiting power-down mode, allow sufficient time for the circuitry to turn on before starting a conversion. If the internal reference is enabled, the reference must be allowed to settle for accurate conversions to occur.

Figure 40 shows the power-down mode operation.

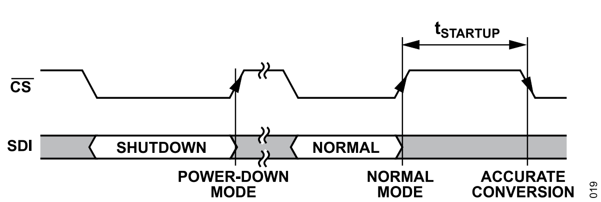


Figure 40. Power-Down Mode Operation

INTERNAL AND EXTERNAL REFERENCES

The AD4684/AD4685 have a buffered 2.5 V internal reference primarily used as reference voltage for device operation. When using the buffered internal 2.5 V reference externally via the REFIO pin, the AD4684/AD4685 must use an external buffer before connecting to the external circuitry. Alternatively, if a more accurate reference or higher dynamic range is required, an external reference can be supplied. An externally supplied reference can range from 2.5 V to 3.3 V. The recommended external voltage reference is the ADR4525 for a 2.5 V reference, and the ADR4533 for a 3.3 V reference.

Reference selection, internal and external, is configured by the REFSEL bit in the CONFIGURATION1 register. If the REFSEL bit is set to 0, the internal reference buffer is enabled. If an external reference is preferred, the REFSEL bit must be set to 1, and an external reference must be supplied to the REFIO pin.

SOFTWARE RESET

The AD4684/AD4685 have two reset modes, a soft reset and a hard reset. A reset is initiated by writing to the RESET bits in the CONFIGURATION2 register. Figure 41 shows the software reset operation.

A soft reset maintains the contents of the configurable registers but refreshes the interface and the ADC blocks. Any internal state machines are reinitialized, and the oversampling block and FIFO are flushed. The alert register is cleared. The reference and LDO regulator remain powered.

A hard reset, in addition to the blocks reset by a soft reset, resets all user registers to the default status, resets the reference buffer, and resets the internal oscillator block.

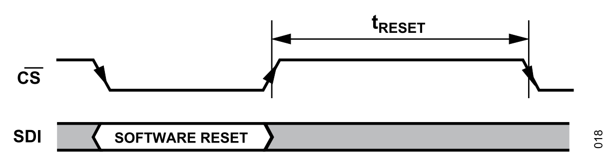


Figure 41. Software Reset Operation

DIAGNOSTIC SELF TEST

The AD4684/AD4685 run a diagnostic self test after a POR or software hard reset to ensure that the correct configuration is loaded into the device.

The result of the self test is displayed in the SETUP_F bit in the alert register. If the SETUP_F bit is set to Logic 1, the diagnostic self test failed. If the self test fails, perform a software hard reset to reset the AD4684/AD4685 to default status.

INTERFACE

The interface to the AD4684/AD4685 is via an SPI. The interface consists of the CS, SCLK, SDOA, SDOB/ALERT, and SDI pins.

The CS signal frames a serial data transfer and initiates an ADC conversion process. The falling edge of CS puts the track-and-hold into hold mode at which point the analog input is sampled and the bus is taken out of three-state.

The SCLK signal synchronizes data in and out of the device via the SDOA, SDOB, and SDI signals. A minimum of 16 SCLKs are required for a write to or read from a register. The minimum number of SCLK pulses for a conversion read is dependent on the resolution of the device and the configuration settings.

The ADC conversion operation is driven internally by an on-board oscillator and is independent of the SCLK signal.

The AD4684/AD4685 have two serial output signals, SDOA and SDOB. To achieve the highest throughput, use both SDOA and SDOB, 2-wire mode, to read the conversion results. If a reduced throughput is required or oversampling is used, it is possible to use 1-wire mode, SDOA signal only, for reading conversion results. Programming the SDO bit in the CONFIGURATION2 register configures 2-wire or 1-wire mode.

Configuring a cyclic redundancy check (CRC) operation for SPI reads, SPI writes, and oversampling modes alters the operation of the interface. The relevant CRC Read, CRC Write, and CRC Polynomial sections of this data sheet must be consulted to ensure correct operation.

READING CONVERSION RESULTS

The CS signal initiates the conversion process. A high to low transition on the CS signal initiates a simultaneous conversion of both ADCs, ADC A and ADC B. The AD4684/AD4685 have a one-cycle readback latency. Therefore, the conversion results are available on the next SPI access. Then, take the CS signal low, and the conversion result clocks out on the SDOA and SDOB/ALERT pin. The next conversion is also initiated at this point. The conversion result is shifted out of the device as a 16-bit word for the AD4684/AD4685. The MSB of the conversion result is shifted out on the CS falling edge. The remaining data is shifted out of the device under the control of the serial clock (SCLK) input. The data is shifted out on the rising edge of SCLK, and the data bits are valid on both the falling edge and the rising edge. After the final SCLK falling edge, take CS high again to return the SDOA and SDOB/ALERT pins to a high impedance state.

The number of SCLK cycles to propagate the conversion results on the SDOA and SDOB/ALERT pins is dependent on the serial mode of operation configured and if resolution boost is enabled (see Figure 42 and Table 10 for details). If CRC reading is enabled, additional SCLK pulses are required to propagate the CRC information (see the CRC section for more details). As the CS signal initiates a conversion, as well as framing the data, access must be completed within a single frame.

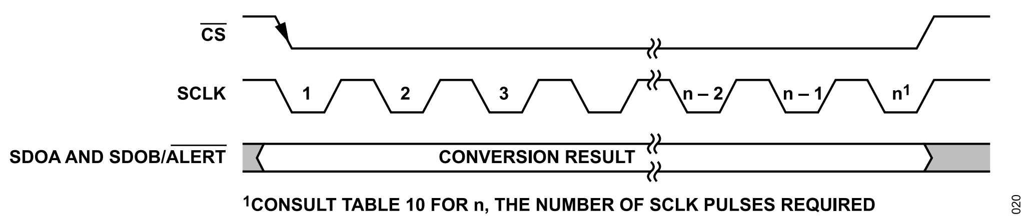


Figure 42. Reading Conversion Results

Table 10. Number of SCLKs, n, Required for Reading Conversion Results

Interface Configuration	Resolution Boost Mode	CRC Read	Number of SCLK Pulses
2-Wire	Disabled	Disabled	16
		Enabled	24
	Enabled	Disabled	18
		Enabled	26
1-Wire	Disabled	Disabled	32
		Enabled	40
	Enabled	Disabled	36
		Enabled	44

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Serial 2-Wire Mode

Configure 2-wire mode by setting the SDO bit in the CONFIGURATION2 register to 0. In 2-wire mode, the conversion result for ADC A is output on the SDOA pin, and the conversion result for ADC B is output on the SDOB/$\overline{\text{ALERT}}$ pin. See Figure 43 for more information.

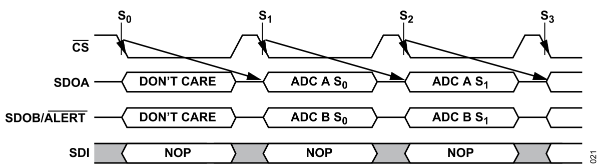

Figure 43. Reading Conversion Results for 2-Wire Mode

Serial 1-Wire Mode

In applications where slower throughput rates are acceptable, the serial interface can be configured to operate in 1-wire mode. In 1-wire mode, the conversion results from ADC A and ADC B are output on the serial output, SDOA. Additional SCLK cycles are required to propagate all the data. ADC A data is output first, followed by the ADC B conversion results. See Figure 44 for more information.

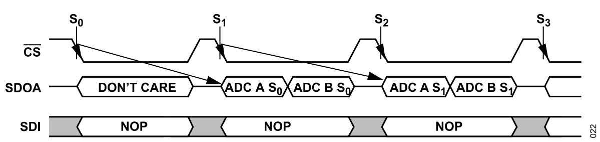

Figure 44. Reading Conversion Results for 1-Wire Mode

Resolution Boost Mode

The default resolution and output data size are 16 bits for the AD4684/AD4685. Enabling the on-chip oversampling function reduces noise and improves the device performance. To accommodate the performance boost, it is possible to enable an additional two bits of resolution in the conversion output data. If the RES bit in the CONFIGURATION1 register is set to Logic 1 and the AD4684/AD4685 are in a valid oversampling mode, the conversion result size is 18 bits. When the resolution boost mode is enabled, 18 SCLK cycles are required to propagate the data.

LOW LATENCY READBACK

The interface on the AD4684/AD4685 has a one-cycle latency, as shown in Figure 45. For applications that operate at lower throughput rates, the latency of reading the conversion result can be reduced. After the conversion time elapses, a second $\overline{\text{CS}}$ pulse after the initial $\overline{\text{CS}}$ pulse that initiated the conversion can be used to read back the conversion result. This operation is shown in Figure 45.

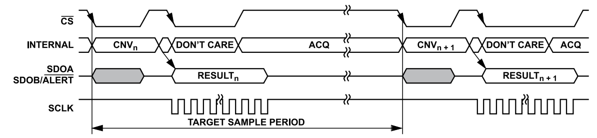

Figure 45. Low Throughput Low Latency

READING FROM DEVICE REGISTERS

All the registers in the devices can be read over the serial interface. A register read is performed by issuing a register read command followed by an additional SPI command that can be either a valid command or a no operation (NOP) command. The format for a read command is shown in Table 13. Bit D15 must be set to 0 to select a read command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0] are ignored. Figure 46 shows the timing details on reading the AD4684/AD4685 registers.

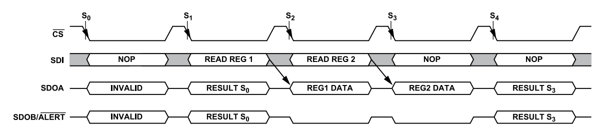

Figure 46. Register Read

WRITING TO DEVICE REGISTERS

All the read and write registers in the AD4684/AD4685 can be written to over the SPI. The length of an SPI write access is determined by the CRC write function. An SPI access is 16 bits if the CRC write is disabled and 24 bits when the CRC write is enabled. The format for a write command is shown in Table 13. Bit D15 must be set to 1 to select a write command. Bits[D14:D12] contain the register address. The subsequent 12 bits, Bits[D11:D0], contain the data to be written to the selected register. Figure 47 shows the timing details on writing to the AD4684/AD4685 registers.

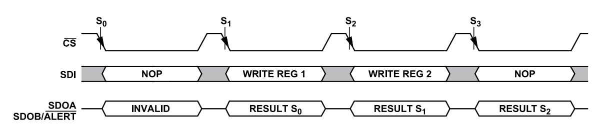

Figure 47. Register Write

CRC

The AD4684/AD4685 have CRC checksum modes that can be used to improve interface robustness by detecting errors in data transmissions. The CRC feature is independently selectable for SPI reads and SPI writes. For example, enable the CRC function for SPI writes to prevent unexpected changes to the device configuration but do not enable it on SPI reads, thus maintaining a higher throughput rate. The CRC feature is controlled by programming the CRC_W bit and CRC_R bit in the CONFIGURATION1 register.

CRC Read

If enabled, a CRC is appended to the conversion result or register read and consists of an 8-bit word. The CRC is calculated in the

INTERFACE

conversion result for ADC A and ADC B and is output on SDOA. A CRC is also calculated and appended to register read outputs.

The CRC read function can be used in 2-wire SPI mode, 1-wire SPI mode, and resolution boost mode.

CRC Write

To enable the CRC write function, the CRC_W bit in the CONFIGURATION1 register must be set to 1. To set the CRC_W bit to 1 to enable the CRC feature, the request frame must have a valid CRC appended to the frame.

After the CRC feature is enabled, all register write requests are ignored unless accompanied by a valid CRC command, requiring a valid CRC to both enable and disable the CRC write feature.

CRC Polynomial

For CRC checksum calculations, the following polynomial is always used:

$x^8 + x^2 + x + 1$

To generate the checksum, the 16-bit data conversion results of the two channels are combined, which produces a 32-bit data. The eight MSBs of the 32-bit data are inverted and then shift by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned such that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned such that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process repeats until the original data is reduced to a value less than the polynomial, the 8-bit checksum. For example, the polynomial is 100000111.

Let the original data of two channels be 0xAAAA and 0x5555, that is, 1010 1010 1010 1010 and 0101 0101 0101 0101. The data of the two channels is then appended, including eight 0s on the right. The data then becomes 1010 1010 1010 1010 0101 0101 0101 0101 0000 0000.

Table 11 shows the CRC calculation of 16-bit, 2-channel data. In the final XOR operation, the reduced data is less than the polynomial. Thus, the remainder is the CRC for the assumed data.

Figure 48 shows the CRC operation.

Table 11. Example CRC Calculation for 2-Channel, 16-Bit Data

Data	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]
Process Data	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0
		1	0	0	0	0	0	1	1	1																														
				1	0	1	0	0	0	1	1	0																												
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																														1	0	0	1	0	0	0	0	0		
																														1	0	0	0	0	0	1	1	1		
CRC																																	1	0	0	1	1	1	0	0

[1] X = don't care.

INTERFACE

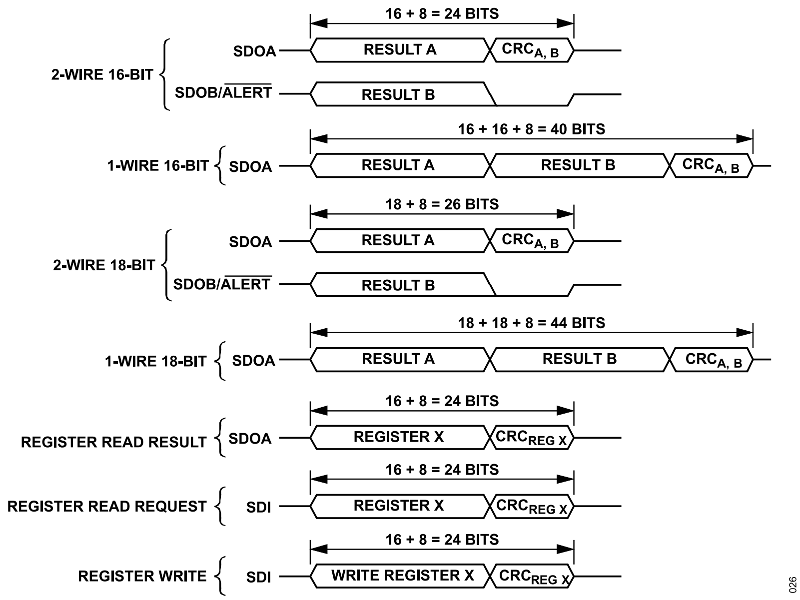

Figure 48. CRC Operation

REGISTERS

The AD4684/AD4685 have user-programmable on-chip registers for configuring the device. Table 12 shows a complete overview of the registers available on the AD4684/AD4685. The registers are either read/write (R/W) or read only (R). Any read request to a write only register is ignored. Any write to a read only register is ignored.

Writes to any other register address are considered a NOP and are ignored. Any read request to a register address, other than those listed in Table 12, are considered an NOP, and the data transmitted in the next SPI frame are the conversion results.

Table 12. Register Description

Reg	Name	Bits	Bit 15 Bit 7	Bit 14 Bit 6	Bit 13 Bit 5	Bit 12 Bit 4	Bit 11 Bit 3	Bit 10 Bit 2	Bit 9 Bit 1	Bit 8 Bit 0	Reset	R/W
0x1	CONFIGURATION1	[15:8]	ADDRESSING				CH	SEQ	OS_MODE	OSR[2]	0x0000	R/W
		[7:0]	OSR[1:0]		CRC_W	CRC_R	ALERT_EN	RES	REFSEL	PMODE		
0x2	CONFIGURATION2	[15:8]	ADDRESSING				RESERVED			SDO	0x0000	R/W
		[7:0]	RESET									
0x3	ALERT	[15:8]	ADDRESSING				RESERVED		CRCW_F	SETUP_F	0x0000	R
		[7:0]	RESERVED		AL_B_HIGH	AL_B_LOW	RESERVED		AL_A_HIGH	AL_A_LOW		
0x4	ALERT_LOW_THRESHOLD	[15:8]	ADDRESSING				ALERT_LOW[11:8]				0x0000	R/W
		[7:0]	ALERT_LOW[7:0]									
0x5	ALERT_HIGH_THRESHOLD	[15:8]	ADDRESSING				ALERT_HIGH[11:8]				0x0FFF	R/W

REGISTERS

ADDRESSING REGISTERS

A serial register transfer on the AD4684/AD4685 consists of 16 SCLK cycles. The four MSBs written to the device are decoded to determine which register is addressed. The four MSBs consist of the register address (REGADDR), Bits[2:0], and the read/write bit (WR). The register address bits determine which on-chip register is selected. The read/write bit determines if the remaining 12 bits of data on the SDI input are loaded into the addressed register if the addressed register is a valid write register. If the WR bit is 1, the bits load into the register addressed by the register select bits. If the WR bit is 0, the command is seen as a read request. The addressed register data is available to be read during the next read operation.

Table 13. Addressing Register Format

MSB															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WR	REGADDR			[D11:D0]											

Table 14. Bit Descriptions for Addressing Registers

Bit	Mnemonic	Description
D15	WR	If a 1 is written to this bit, Bits[D11:D0] of this register are written to the register specified by the REGADDR bits if it is a valid address. Alternatively, if a 0 is written, the next data sent out on the SDOA pin is a read from the designated register if it is a valid address.
D14 to D12	REGADDR	When WR = 1, the contents of the REGADDR bits determine the register for selection as outlined in Table 12. When WR = 0, and the REGADDR bits contain a valid register address, the contents on the requested register are output on the SDOA pin during the next interface access. When WR = 0, and the REGADDR bits contain 0x0, 0x6, or 0x7, the contents on the SDI line are ignored. The next interface access results in the conversion results being read back.
D11 to D0	[D11:D0]	These bits are written into the corresponding register specified by the REGADDR bits when the WR bit is equal to 1 and the REGADDR bits contain a valid address.

CONFIGURATION1 REGISTER

Address: 0x1, Reset: 0x0000, Name: CONFIGURATION1

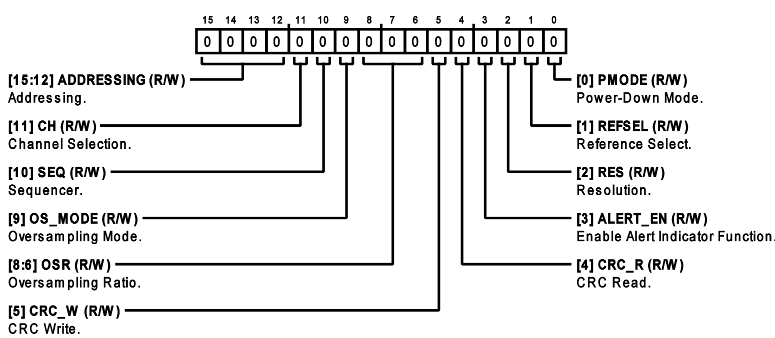

Table 15. Bit Descriptions for CONFIGURATION1

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
11	CH	Channel Selection. Selects the channels to be converted. 0: Channel 0s. Selects Channel 0s of the ADC, $A_{IN}A0$ and $A_{IN}B0$. 1: Channel 1s. Selects Channel 1s of the ADC, $A_{IN}A1$ and $A_{IN}B1$.	0x0	R/W
10	SEQ	Sequencer. Cycles through the $A_{IN}x0$ and $A_{IN}x1$ channels of the ADC for conversion. 0: sequencer disabled. 1: sequencer enabled.	0x0	R/W
9	OS_MODE	Oversampling Mode. Enables the rolling average oversampling mode of the ADC. 0: disable. 1: enable.	0x0	R/W

REGISTERS

Table 15. Bit Descriptions for CONFIGURATION1 (Continued)

Bits	Bit Name	Description	Reset	Access
[8:6]	OSR	Oversampling Ratio. Sets the oversampling ratio for all the ADCs in the rolling average mode. Rolling average mode supports oversampling ratios of ×2, ×4, and ×8. 000: disabled. 001: ×2. 010: ×4. 011: ×8. 100: disabled. 101: disabled 110: disabled. 111: disabled.	0x0	R/W
5	CRC_W	CRC Write. Controls the CRC functionality for the SDI interface. When setting this bit from a 0 to a 1, the command must be followed by a valid CRC to set this configuration bit. If a valid CRC is not received, the entire frame is ignored. If the bit is set to 1, it requires a CRC to clear it to 0. 0: no CRC function. 1: CRC function.	0x0	R/W
4	CRC_R	CRC Read. Controls the CRC functionality for the SDOA and SDOB/$\overline{\text{ALERT}}$ interface. 0: no CRC function. 1: CRC function.	0x0	R/W
3	ALERT_EN	Enable Alert Indicator Function. This register functions when the SDO bit = 1. Otherwise, the ALERT_EN bit is ignored. 0: SDOB. 1: $\overline{\text{ALERT}}$.	0x0	R/W
2	RES	Resolution. Sets the size of the conversion result data. If OSR = 0, these bits are ignored and the resolution is set to default resolution. 0: normal resolution. 1: 2-bit higher resolution.	0x0	R/W
1	REFSEL	Reference Select. Selects the ADC reference source. 0: selects internal reference. 1: selects external reference.	0x0	R/W
0	PMODE	Power-Down Mode. Sets the power modes. 0: normal mode. 1: power-down mode.	0x0	R/W

CONFIGURATION2 REGISTER

Address: 0x2, Reset: 0x0000, Name: CONFIGURATION2

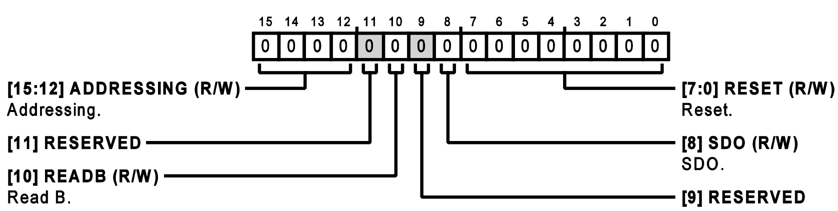

Table 16. Bit Descriptions for CONFIGURATION2

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:9]	RESERVED	Reserved.	0x0	R

REGISTERS

Table 16. Bit Descriptions for CONFIGURATION2 (Continued)

Bits	Bit Name	Description	Reset	Access
8	SDO	SDO. Conversion results serial data output. 0: 2-wire—conversion data are output on both SDOA and SDOB/ALERT pins. 1: 1-wire—conversion data are output on SDOA pin only.	0x0	R/W
[7:0]	RESET	Reset. 0x3C—performs a soft reset. Refreshes some blocks. Register contents remain unchanged. Clears the alert register and flushes any oversampling stored variables or active state machine. 0xFF—performs a hard reset. Resets all possible blocks in the device. Register contents are set to defaults. All other values are ignored.	0x0	R/W

ALERT REGISTER

Address: 0x3, Reset: 0x0000, Name: Alert

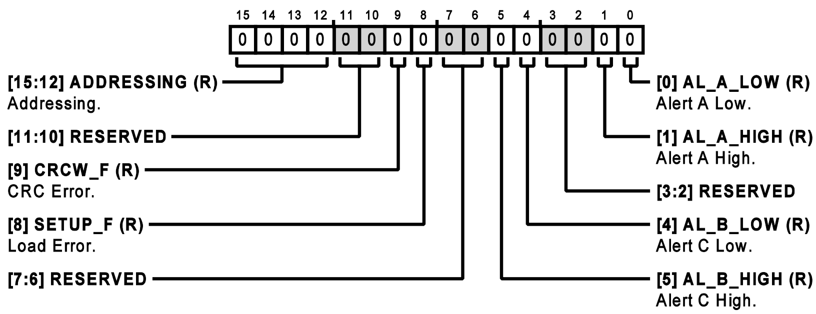

Table 17. Bit Descriptions for Alert

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R
[11:10]	RESERVED	Reserved.	0x0	R
9	CRCW_F	CRC Error. Indicates that a register write command failed due to a CRC error. This fault bit is sticky and remains set until the register is read. 0: no CRC error. 1: CRC error.	0x0	R
8	SETUP_F	Load Error. The SETUP_F bit indicates that the device configuration data did not load correctly on startup. This bit does not clear on an alert register read. A hard reset via the CONFIGURATION2 register is required to clear this bit and restart the device setup again. 0: no setup error. 1: setup error.	0x0	R
[7:6]	RESERVED	Reserved.	0x0	R
5	AL_B_HIGH	Alert B High. The alert indication high bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
4	AL_B_LOW	Alert B Low. The alert indication low bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R
[3:2]	RESERVED	Reserved.	0x0	R

REGISTERS

Table 17. Bit Descriptions for Alert (Continued)

Bits	Bit Name	Description	Reset	Access
1	AL_A_HIGH	Alert A High. The alert indication high bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_HIGH_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 0: no alert indication. 1: alert indication.	0x0	R
0	AL_A_LOW	Alert A Low. The alert indication low bits indicate if a conversion result for the respective input channel exceeds the value set in the ALERT_LOW_THRESHOLD register. This fault bit is sticky and remains set until the register is read. 1: alert indication. 0: no alert indication.	0x0	R

ALERT_LOW_THRESHOLD REGISTER

Address: 0x4, Reset: 0x0000, Name: ALERT_LOW_THRESHOLD

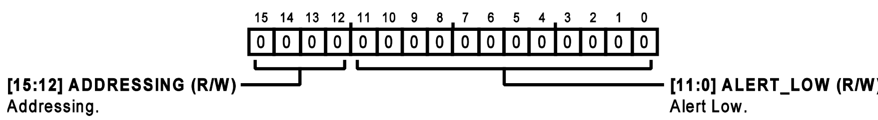

Table 18. Bit Descriptions for ALERT_LOW_THRESHOLD

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_LOW	Alert Low. Data Bits[D11:D0] are the MSBs of the 16-bit internal alert low register. The remaining 4 bits are fixed at 0x0, which sets an alert when the conversion result is below the ALERT_LOW_THRESHOLD and disables when the conversion result is above the ALERT_LOW_THRESHOLD.	0x0	R/W

ALERT_HIGH_THRESHOLD REGISTER

Address: 0x5, Reset: 0x0FFF, Name: ALERT_HIGH_THRESHOLD

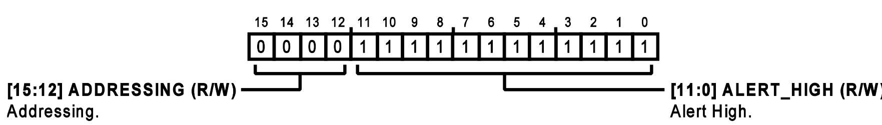

Table 19. Bit Descriptions for ALERT_HIGH_THRESHOLD

Bits	Bit Name	Description	Reset	Access
[15:12]	ADDRESSING	Addressing. Bits[15:12] define the address of the relevant register. See the Addressing Registers section for further details.	0x0	R/W
[11:0]	ALERT_HIGH	Alert High. Data Bits[D11:D0] are the MSBs of the 16-bit internal alert high register. The remaining 4 bits are fixed at 0xF, which sets an alert when the conversion result is above the ALERT_HIGH_THRESHOLD and disables when the conversion result is below the ALERT_HIGH_THRESHOLD.	0xFFF	R/W

OUTLINE DIMENSIONS

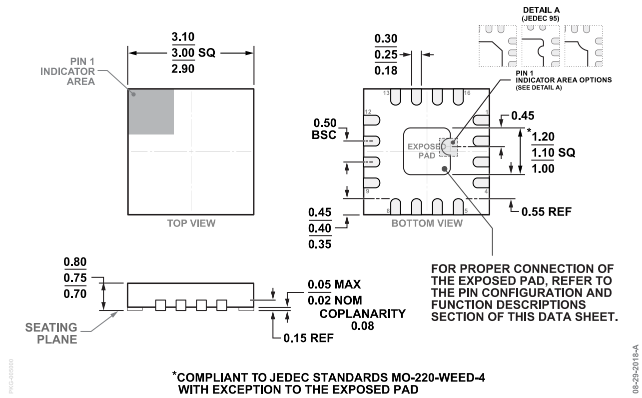

Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-16-45)
Dimensions shown in millimeters

Updated: May 17, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code
AD4684BCPZ-R2	-40°C to +125°C	16-Lead LFCSP (3mm x 3mm x 0.75mm w/ EP)	Reel, 250	CP-16-45	CAQ
AD4684BCPZ-RL	-40°C to +125°C	16-Lead LFCSP (3mm x 3mm x 0.75mm w/ EP)	Reel, 5000	CP-16-45	CAQ
AD4684BCPZ-RL7	-40°C to +125°C	16-Lead LFCSP (3mm x 3mm x 0.75mm w/ EP)	Reel, 1500	CP-16-45	CAQ
AD4685BCPZ-RL	-40°C to +125°C	16-Lead LFCSP (3mm x 3mm x 0.75mm w/ EP)	Reel, 5000	CP-16-45	CAR
AD4685BCPZ-RL7	-40°C to +125°C	16-Lead LFCSP (3mm x 3mm x 0.75mm w/ EP)	Reel, 1500	CP-16-45	CAR

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1, 2]	Description
EVAL-AD7386FMCZ	AD7386 Evaluation Board

[1] Z = RoHS Compliant Part.

[2] Use the EVAL-AD7386FMCZ to evaluate the AD4684 and the AD4683.