CMOS 12-Bit Multiplying D/A Converter "With Memory"

DAC-8012

FEATURES

- **Data Readback Capability for System Self Check**
- **Fast TTL/CMOS Compatible Data Register**
- **±1/2 LSB Max Linearity Error Over the Full Operating Temperature Range**
- **±1 LSB Max Gain Error — No User Adjustment Required**
- **Less Than 0.04 LSB Max Zero Scale Error (10nA)**
- **Single +5V to +15V Supply**
- **Small 20-Pin 0.3" Wide DIP**
- **Improved ESD Resistance**
- **Latch-Up Resistant**
- **Adds Data Readback Feature to PM-7545 Pinout**
- **Available in Die Form**

GENERAL DESCRIPTION

The DAC-8012 is a monolithic 12-bit CMOS multiplying DAC with internal data latches and three-state data readback buffers. The latches and readback buffers perform like a "memory" location. Data loads into the latches as a single 12-bit wide word allowing direct connection to 12-bit and 16-bit busses.

Four-quadrant multiplying capability and 12-bit linearity simplifies wide-bandwidth, low-distortion, digitally-controlled precision attenuator and filter applications.

The powerful data readback function allows users to perform data path verification between the controlling processor and the DAC-8012. System self check results after writing a data word to the DAC-8012, then reading it back to the processor, verifying no change in data takes place. The readback function simplifies the design of automatic test equipment, industrial automation, robotics, and processor-controlled instrumentation. Reduction of software coding results with processors using direct memory execution instructions. In remote systems, data set-points are held in the DAC register which can be interrogated upon system fault recovery.

ORDERING INFORMATION †

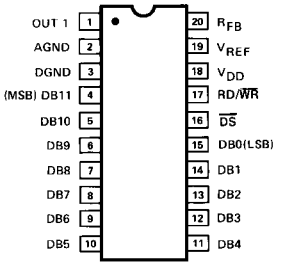
	PACKAGE: 20-PIN			
RELATIVE ACCURACY	MAXIMUM GAIN ERROR T_A = +25°C V_{DD} = +5V	MILITARY* TEMPERATURE –55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE –40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1/2 LSB	±1 LSB	DAC8012AR	DAC8012ER	DAC8012GP
±1 LSB	±3 LSB	DAC8012BR	DAC8012FR	DAC8012HP
±1 LSB	±3 LSB	–	DAC8012FP	–
±1 LSB	±3 LSB	–	DAC8012FPC	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

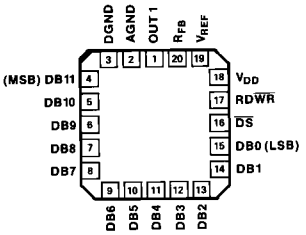
†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

PIN CONNECTIONS



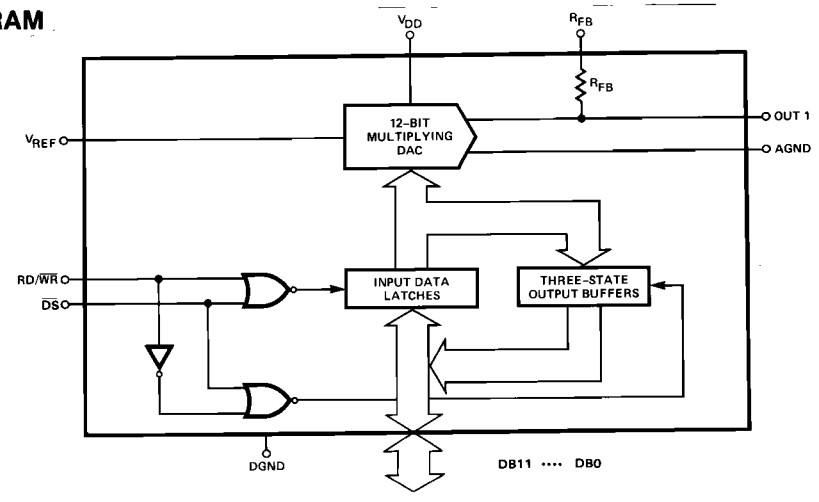
20-PIN EPOXY DIP (P-Suffix)

20-PIN HERMETIC DIP (R-Suffix)



20-LEAD PLCC (PC-Suffix)

FUNCTIONAL DIAGRAM



REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... –0.3V, +17V
Digital Input Voltage to DGND ..... –0.3V, V_{DD}
AGND to DGND ..... –0.3, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... –0.3V, V_{DD}
Operating Temperature Range
  Military (AR, BR) Grades ..... –55°C to +125°C
  Industrial (ER, FR, FP, FPC) Grades ..... –40°C to +85°C
  Commercial (GP, HP) Grades ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings " may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, $V_{OUT\ 1}$ = 0V, AGND = DGND = 0V, T_A = –55°C to +125°C apply for DAC-8012AR/BR, T_A = –40°C to +85°C apply for DAC-8012ER/FR/FP/FPC, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G MIN	TYP	MAX	DAC-8012B/F/H MIN	TYP	MAX	UNITS
STATIC ACCURACY									
Resolution			12	—	—	12	—	—	Bits
Relative Accuracy	INL	T_A = Full Temp. Range	—	—	±1/2	—	—	±1	LSB
Differential Nonlinearity (Note 1)	DNL	T_A = Full Temp. Range	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C	—	—	±1	—	—	±3	LSB
		T_A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature (Notes 4, 5)	TCG_{FS}		—	—	±5	—	—	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD} (Note 4)	PSR	T_A = +25°C (ΔV_{DD} = ±5%)	—	—	0.002	—	—	0.002	%/%
		T_A = Full Temp. Range (ΔV_{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT 1	I_{LKG}	T_A = +25°C, RD/$\overline{WR}$ = $\overline{DS}$ = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T_A = Full Temp. Range							
		A/B Versions	—	—	200	—	—	200	
		E/F/G/H Versions	—	—	25	—	—	25	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 6, & 7)	t_{pD}	T_A = +25°C (OUT 1 Load = 100Ω, C_{EXT} = 13pF)	—	—	300	—	—	300	ns
Current Settling Time (Notes 4, 7)	t_s	T_A = Full Temp. Range (To 1/2 LSB) $I_{OUT\ 1}$ Load = 100Ω	—	—	1	—	—	1	μs
Glitch Energy (Note 4)	Q	T_A = +25°C	—	—	400	—	—	400	nVs
		T_A = Full Temp. Range V_{REF} = AGND	—	—	500	—	—	500	
AC Feedthrough at $I_{OUT\ 1}$ (Note 4)	FT	T_A = Full Temp. Range V_{REF} = ±10V, f = 10kHz	—	—	5	—	—	5	mV_{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	T_A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V, T_A = –55°C to +125°C apply for DAC-8012AR/BR, T_A = –40°C to +85°C apply for DAC-8012ER/FR/FP/FPC, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

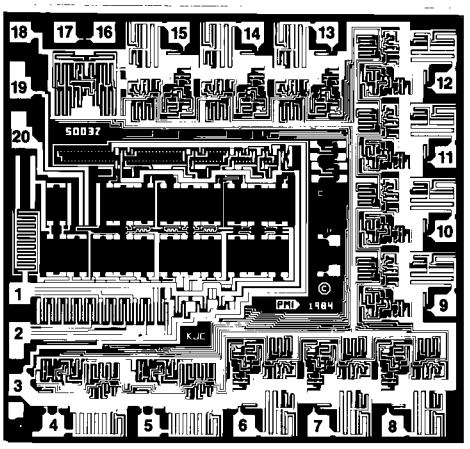
PARAMETER	SYMBOL	CONDITIONS	DAC-8012A/E/G MIN	TYP	MAX	DAC-8012B/F/H MIN	TYP	MAX	UNITS
ANALOG OUTPUTS									
Output Capacitance (Note 4) $C_{OUT\,1}$	C_{OUT}	V_{DD} = +5V or +15V, T_A = Full Temp. Range, DB0-DB11 = 0V, RD/$\overline{WR}$ = $\overline{DS}$ = 0V	—	—	70	—	—	70	pF
		DB0-DB11 = V_{DD}, RD/$\overline{WR}$ = $\overline{DS}$ = 0V	—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	µA
		T_A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0-DB11 (Note 4)	C_{IN}	T_A = Full Temp. Range	—	—	12	—	—	12	pF
Input Capacitance RD/$\overline{WR}$, $\overline{DS}$ (Note 4)			—	—	6	—	—	6	
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	I_O = 400µA	4.0	—	—	4.0	—	—	V
Output Low Voltage	V_{OL}	I_O = –1.6mA	—	—	0.4	—	—	0.4	V
Three-State Output Leakage Current			—	—	10	—	—	10	µA
SWITCHING CHARACTERISTICS (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Write Hold Time	t_{WH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Read to Data Strobe Setup Time	t_{RSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Read Hold Time	t_{RH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Write Mode Data Strobe Width	t_{WRS}	T_A = +25°C	180	—	—	180	—	—	ns
		T_A = Full Temp. Range	250	—	—	250	—	—	
Read Mode Data Strobe Width	t_{RDS}	T_A = +25°C	220	—	—	220	—	—	ns
		T_A = Full Temp. Range	290	—	—	290	—	—	
Data Setup Time	t_{DSU}	T_A = +25°C	210	—	—	210	—	—	ns
		T_A = Full Temp. Range	250	—	—	250	—	—	
Data Hold Time	t_{DH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Data Valid Time (Notes 4, 9)	t_{CO}	T_A = +25°C	—	—	300	—	—	300	ns
		T_A = Full Temp. Range	—	—	400	—	—	400	
Output Active Time from Deselection (Notes 4, 9)	t_{OTD}	T_A = +25°C	—	—	215	—	—	215	ns
		T_A = Full Temp. Range	—	—	375	—	—	375	
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	µA

ELECTRICAL CHARACTERISTICS at V_{DD} = ±15V, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND = 0V, T_A = –55°C to +125°C apply for DAC-8012AR/BR, T_A = –40°C to +85°C apply for DAC-8012ER/FR/FP/FPC, T_A = 0°C to +70°C apply for DAC-8012GP/HP, unless otherwise noted.

			DAC-8012A/E/G			DAC-8012B/F/H			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range	13.5	—	—	13.5	—	—	V
Input Low Voltage	V_{INL}		—	—	1.5	—	—	1.5	
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	µA
		T_A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0-DB11	C_{IN}	T_A = Full Temp. Range	—	—	12	—	—	12	pF
RD/$\overline{WR}$, $\overline{DS}$ (Note 4)			—	—	10	—	—	10	
DIGITAL OUTPUTS									
Output High Voltage	V_{OH}	I_O = 3mA	13.5	—	—	13.5	—	—	V
Output Low Voltage	V_{OL}	I_O = -3mA	—	—	1.5	—	—	1.5	V
Three-State Output Leakage Current			—	—	10	—	—	10	µA
SWITCHING CHARACTERISTICS (Note 8)		See Timing Diagram							
Write to Data Strobe Setup Time	t_{WSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Write Hold Time	t_{WH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Read to Data Strobe Setup Time	t_{RSU}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Read Hold Time	t_{RH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Write Mode Data Strobe Width	t_{WRS}	T_A = +25°C	100	—	—	100	—	—	ns
		T_A = Full Temp. Range	120	—	—	120	—	—	
Read Mode Data Strobe Width	t_{RDS}	T_A = +25°C	110	—	—	110	—	—	ns
		T_A = Full Temp. Range	150	—	—	150	—	—	
Data Setup Time	t_{DSU}	T_A = +25°C	90	—	—	90	—	—	ns
		T_A = Full Temp. Range	120	—	—	120	—	—	
Data Hold Time	t_{DH}	T_A = +25°C	0	—	—	0	—	—	ns
		T_A = Full Temp. Range	0	—	—	0	—	—	
Data Strobe to Output Valid Time (Note 9)	t_{CO}	T_A = +25°C	—	—	180	—	—	180	ns
		T_A = Full Temp. Range	—	—	220	—	—	220	
Output Active Time for Deselection (Note 9)	t_{OTD}	T_A = +25°C	—	—	180	—	—	180	ns
		T_A = Full Temp. Range	—	—	250	—	—	250	
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	10	100	—	10	100	µA

NOTES:
1. 12-bit monotonic over full temperature range.
2. Includes the effects of 5ppm max. gain T.C.
3. Using internal R_{FB}. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
4. GUARANTEED but NOT TESTED.
5. Typical value is 2ppm/°C for V_{DD} = +5V.
6. From digital input change to 90% of final analog output.
7. All digital inputs = 0V to V_{DD}, or V_{DD} to 0V.
8. Sample tested at +25°C to ensure compliance.
9. See load circuits for switching tests.

DICE CHARACTERISTICS



DIE SIZE 0.121 × 0.112 inch, 13,552 sq. mils
(3.07 × 2.85 mm, 8.75 sq. mm)

1. OUT 1
2. AGND
3. DGND
4. DB11 (MSB)
5. DB10
6. DB9
7. DB8
8. DB7
9. DB6
10. DB5
11. DB4
12. DB3
13. DB2
14. DB1
15. DB0 (LSB)
16. $\overline{DS}$
17. RD/$\overline{WR}$
18. V_{DD}
19. V_{REF}
20. R_{FB}

WAFER TEST LIMITS at V_{DD} = +5V or +15V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V, AGND = DGND = 0V, T_A = 25°C, unless otherwise noted.

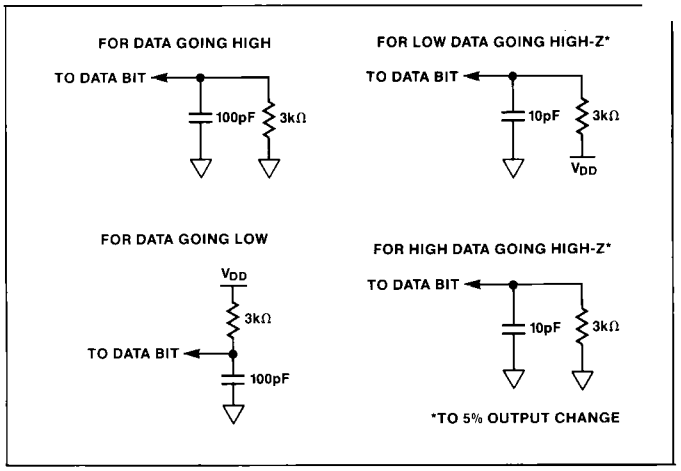
PARAMETER	SYMBOL	CONDITIONS	DAC-8012G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111 1111	±3	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R_{REF}	Pad 19	6/15	kΩ MIN/ kΩ MAX
Output High Voltage	V_{OH}	V_{DD} = 5V, I_O = 400μA	4.0	V MIN
Output Low Voltage	V_{OL}	V_{DD} = 5V, I_O = −1.6mA	0.4	V MAX
Digital Input High	V_{INH}	V_{DD} = 5V V_{DD} = 15V	2.4 13.5	V MIN
Digital Input Low	V_{INL}	V_{DD} = 5V V_{DD} = 15V	0.8 1.5	V MAX
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSRR	V_{DD} = ±5%	0.004	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, V_{REF} = +10V, $V_{OUT\,1}$ = 0V; T_A = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-8012G TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		12	pF
Output Capacitance	$C_{OUT\,1}$	DAC Latches Loaded with 0000 0000 0000	70	pF
	$C_{OUT\,1}$	DAC Latches Loaded with 1111 1111 1111	150	pF
Propagation Delay	t_{pD}	V_{DD} = 15V V_{DD} = 5V	300	ns

LOAD CIRCUITS FOR SWITCHING TESTS



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ±1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will not decrease for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT1 to AGND.

PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

FEEDTHROUGH GLITCH ENERGY

This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with V_{REF} = AGND.

LOGIC INFORMATION

D/A CONVERTER SECTION

Figure 1 shows a simplified circuit of the D/A Converter section of the DAC-8012, and Figure 2 gives an approximate equivalent switch circuit. R is typically 11kΩ.

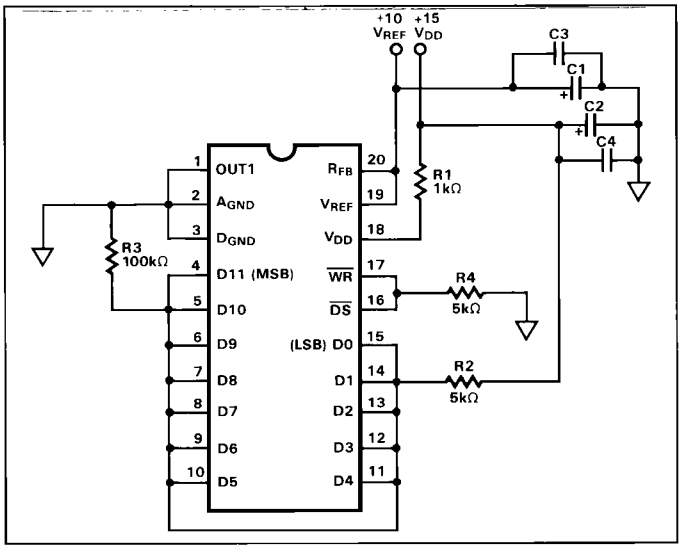
The binary-weighted currents are switched between OUT 1 and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT 1 terminal, $C_{OUT\ 1}$, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT 1). One of the current switches is shown in Figure 2.

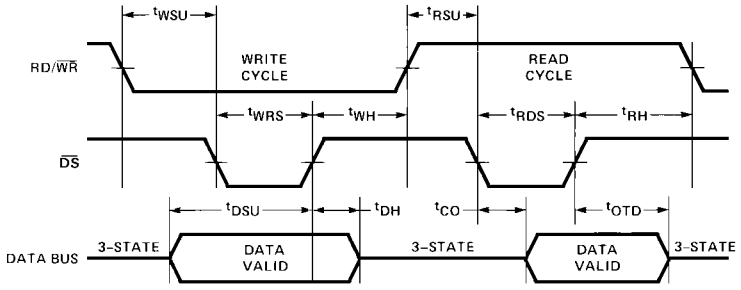
The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however, when the circuit is not powered up the switch assumes an open state.

BURN-IN CIRCUIT



TIMING DIAGRAM



NOTES:
V_{DD} = +5V; $t_r = t_F$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}
TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

FIGURE 1: Simplified D/A Circuit of DAC-8012

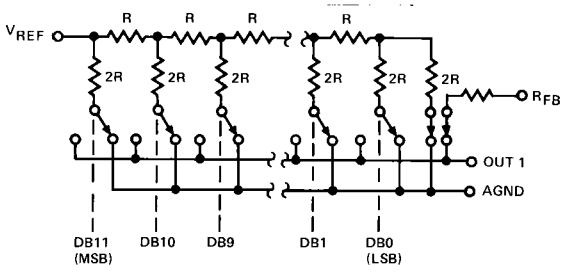


FIGURE 2: N-Channel Current Steering Switch

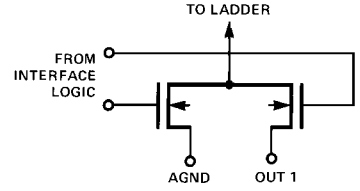
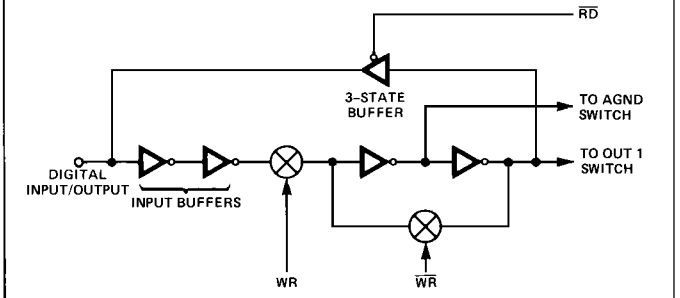


FIGURE 3: Digital Input/Output Structure



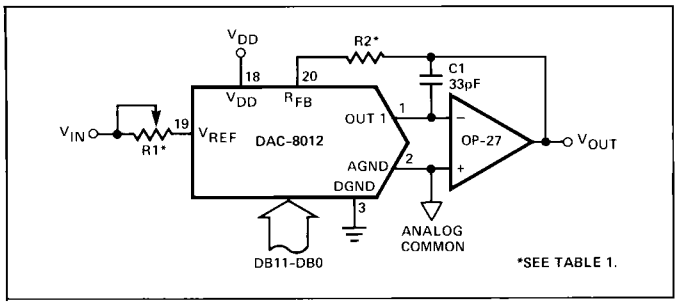
DIGITAL SECTION

Figure 3 shows the digital I/O structure for one bit. When the data strobe ($\overline{DS}$) and the RD/$\overline{WR}$ lines are held low, data at the digital input is fed through the input buffers and the data latches which control the DAC current output switches are transparent. Data is latched when either $\overline{DS}$ or RD/$\overline{WR}$ go high. When the data strobe $\overline{DS}$ is held low and the RD/$\overline{WR}$ line is held high, the three-state buffer becomes active and the data from the latches is fed through the three-state buffers to the digital input/output lines. This is known as the Read Cycle, or data readback.

The input buffers are simple CMOS inverters designed such that when the DAC-8012 is operated with V_{DD} = +5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0V to 3.0V, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and D_{GND}) as is practically possible. The DAC-8012 may be operated with any supply voltage in the range 5V $\leq V_{DD} \leq$ 15V. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

The three-state output buffers, in the active mode, provide TTL-compatible digital outputs with a fan-out of one TTL load when the DAC-8012 is operated with +5V power supply. When powered from +15V, the output buffers provide output logic levels of 1.5V and 13.5V. Three-state output leakage is typically 10nA.

FIGURE 4: Unipolar Binary Operation



BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the DAC-8012. Resistor R1 is used to trim for full scale. The following versions: DAC-8012AR, DAC-8012ER, DAC-8012GP, have a guaranteed maximum gain error of ±1 LSB at +25°C and V_{DD} = +5V, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20V \leq V_{IN} \leq +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table II shows the code relationship for the circuit of Figure 4.

Figure 5 and Table III illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code, and inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software, using an exclusive OR instruction.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	HP/FR/BR	GP/ER/AR
R1	100Ω	20Ω
R2	33Ω	6.8Ω

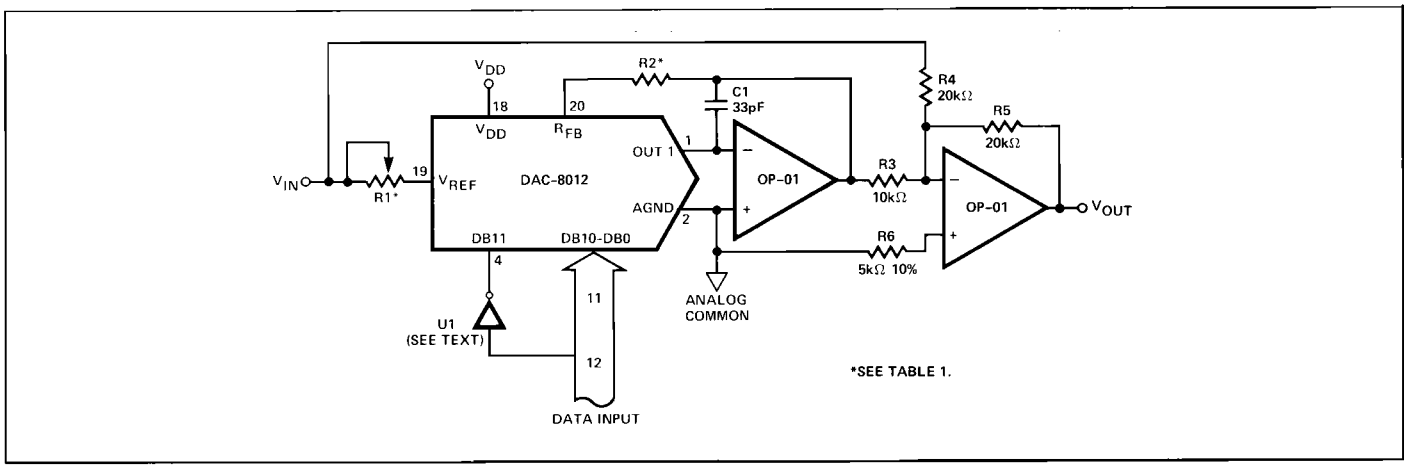
TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER	ANALOG OUTPUT
1111 1111 1111	$-V_{IN} \cdot \left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{IN} \cdot \left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000 0000 0001	$-V_{IN} \cdot \left(\frac{1}{4096}\right)$
0000 0000 0000	0 Volts

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT	ANALOG OUTPUT
0111 1111 1111	$+V_{IN} \cdot \left(\frac{2047}{2048}\right)$
0000 0000 0001	$+V_{IN} \cdot \left(\frac{1}{2048}\right)$
0000 0000 0000	0 Volts
1111 1111 1111	$-V_{IN} \cdot \left(\frac{1}{2048}\right)$
1000 0000 0000	$-V_{IN} \cdot \left(\frac{2048}{2048}\right)$

FIGURE 5: Bipolar Operation (2's Complement Code)



APPLICATIONS HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the DAC-8012. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When RD/$\overline{WR}$ and $\overline{DS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which RD/$\overline{WR}$ is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse RD/$\overline{WR}$, so that it only occurs when data is valid, will eliminate the problem.

INTERFACING THE DAC-8012 TO MICROPROCESSORS

Figure 6 shows the interface configuration for the 68000 16-bit microprocessor. No external logic is required to write data into the DAC or to readback data from the DAC-8012 latches. Analog circuitry has been removed for clarity.

FIGURE 6: 68000 16-Bit Microprocessor to DAC-8012 Interface

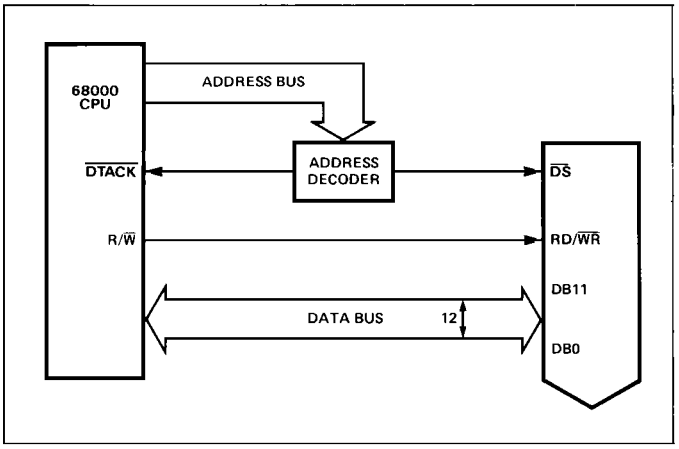


FIGURE 7: 8-Bit Processor to DAC-8012 Interface