MAXIM

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

General Description

The MAX154/MAX158 and AD7824/AD7828 are high speed multi-channel A/D converters. The MAX154 and AD7824 have 4 analog input channels while the MAX158 and AD7828 have 8 channels. Conversion time for all devices is 2.5μs. The MAX154/MAX158 also features a 2.5V on-chip reference, forming a complete high speed data acquisition system.

All converters include a built-in track-and-hold, eliminating the need for an external track-and-hold with many input signals. The analog input range is 0V to +5V although the A/D operates from a single +5V supply.

Microprocessor interface's are simplified by the ADC's ability to appear as a memory location or I/O port without the need for external logic. The data outputs use latched, three-state buffer circuitry to allow direct connection to a microprocessor data bus or system input port.

The AD7824 and AD7828 are pin compatible with Analog Devices' AD7824 and AD7828. The MAX154 and MAX158, which feature internal references, are also compatible with these products.

Applications

Digital Signal Processing
High Speed Data Acquisition
Telecommunications
High Speed Servo Control
Audio Instrumentation

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Features

- **One-Chip Data Acquisition System**
- **4 or 8 Analog Input Channels**
- **2.5μs Per Channel Conversion Time**
- **Internal 2.5V Reference (MAX154/MAX158 only)**
- **Built In Track/Hold Function**
- **½ LSB Error Specification**
- **Single +5V Supply Operation**
- **No External Clock**

Ordering Information

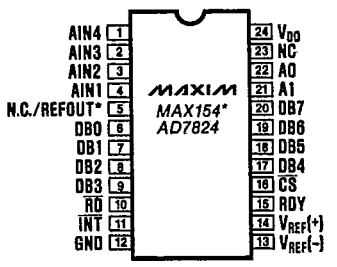
PART	TEMP RANGE	PACKAGE*	ERROR
MAX154ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX154BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX154BC/D	0°C to +70°C	Dice	±1 LSB
MAX154ACWG	0°C to +70°C	Small Outline	±½ LSB
MAX154BCWG	0°C to +70°C	Small Outline	±1 LSB
MAX154AENG	-40°C to +85°C	Plastic DIP	±½ LSB
MAX154BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX154AEWG	-40°C to +85°C	Small Outline	±½ LSB
MAX154BEWG	-40°C to +85°C	Small Outline	±1 LSB
MAX154AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX154BMRG	-55°C to +125°C	CERDIP	±1 LSB

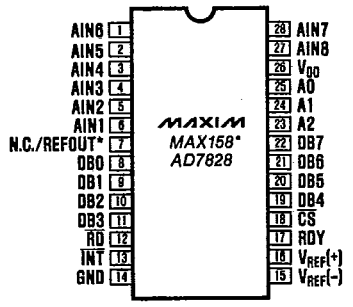
* *MAX154/AD7824 — 24 lead package,*
MAX158/AD7828 — 28 lead package

Ordering Information continued on last page.

Pin Configurations

Top View





*REFOUT on MAX154/MAX158 only

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} to GND ..... 0V, +10V
Voltage at any other pins ..... GND - 0.3V, V_{DD} +0.3V
Output current (REF_{OUT}) 30mA
Power Dissipation (Any Package) to 75°C 450mW
Derate Above +25°C by ..... 6mW/°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Operating Temperature Ranges
MAX154, MAX158
XCXX ..... 0°C to +70°C
XEXX ..... -40°C to +85°C
XMXX ..... -55°C to +125°C
AD7824, AD7828
KN/LN/KCWX/LCWX ..... 0°C to +70°C
BQ/CQ ..... -25°C to +85°C
TQ/UQ ..... -55°C to +125°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, MODE 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
ACCURACY						
Resolution			8			bits
Total Unadjusted Error (Note 1)		MAX15XA, AD782XL/C/U MAX15XB, AD782XK/B/T			±1/2 ±1	LSB
No Missing Codes Resolution			8			bits
Channel to Channel Mismatch					±1/4	LSB
REFERENCE INPUT						
Reference Resistance		T_A = T_{MIN} to T_{MAX}	1		4	kΩ
V_{REF}^+ Input Voltage Range			V_{REF}^-		V_{DD}	V
V_{REF}^- Input Voltage Range			GND		V_{REF}^+	V
REFERENCE OUTPUT — MAX154/MAX158 ONLY (NOTE 2)						
Output Voltage	**REF OUT**	**T_A = +25°C**	**2.47**	**2.50**	**2.53**	**V**
Load Regulation		**I_L = 0 to 10mA T_A = +25°C**		**-6**	**-10**	**mV**
Power Supply Sensitivity		**V_{DD} ±5% T_A = +25°C**		**±1**	**±3**	**mV**
Temperature Drift (Note 3)		**MAX15XXC T_A = 0°C to +70°C MAX15XXE T_A = -40°C to +85°C MAX15XXM T_A = -55°C to +125°C**		**40 40 60**	**70 70 100**	**ppm/°C**
Output Noise	**e_N**			**200**		**μV/rms**
Capacitive Load					**0.01**	**μF**
ANALOG INPUT						
Analog Input Voltage Range	A_{INR}		V_{REF}^-		V_{REF}^+	V
Analog Input Capacitance	C_{AIN}			45		pF
Analog Input Current	I_{AIN}	Any Channel, AIN = 0V to +5V			±3	μA
Slew Rate, Tracking (Note 4)	SR			0.7	0.157	V/μs
LOGIC INPUTS ($\overline{RD}$, $\overline{CS}$, A0, A1, A2)						
Input HIGH Voltage	V_{INH}		2.4			V
Input LOW Voltage	V_{INL}				0.8	V
Input High Current	I_{INH}				1	μA
Input Low Current	I_{INL}				-1	μA
Input Capacitance (Note 8)	C_{IN}			5	8	pF

Note 1: Total unadjusted error includes offset, full-scale and linearity errors.
Note 2: Specified with no external load unless otherwise noted.
Note 3: Temperature drift is defined as change in output voltage from +25°C to T_{MIN} or T_{MAX} divided by (25 - T_{MIN}) or (T_{MAX} -25).
Note 4: Sample tested at +25°C by Quality Assurance to ensure compliance.

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, MODE 0, T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
LOGIC OUTPUTS						
Output HIGH Voltage	V_{OH}	DB0–DB7, $\overline{INT}$; I_{OUT} = -360µA	4.0			V
Output LOW Voltage	V_{OL}	DB0–DB7, $\overline{INT}$; I_{OUT} = 1.6mA RDY; I_{OUT} = 2.6mA			0.4 0.4	V
Three-state Output Current		DB0–DB7, RDY; V_{OUT} = 0V to V_{DD}			±3	µA
Output Capacitance (Note 8)	C_{OUT}			5	8	pF
POWER SUPPLY						
Supply Voltage	V_{DD}	5V ±5% for Specified Performance	+4.75		+5.25	V
Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = +2.4V			15	mA
Power Dissipation				25	75	mW
Power Supply Sensitivity	PSS	V_{DD} = ±5%		±1/16	±1/4	LSB

TIMING CHARACTERISTICS (Note 4, 5)

(V_{DD} = +5V, V_{REF}^+ = +5V, V_{REF}^- = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX15XC/E AD782XK/L/B/C		MAX15XM AD782XT/U		UNITS
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
$\overline{CS}$ to $\overline{RD}$, Setup Time	t_{CSS}		0			0		0		ns
$\overline{CS}$ to $\overline{RD}$, Hold Time	t_{CSH}		0			0		0		ns
Multiplexer Address Setup Time	t_{AS}		0			0		0		ns
Multiplexer Address Hold Time	t_{AH}		30			35		40		ns
$\overline{CS}$ to RDY Delay	t_{RDY}	C_L = 50pF, R = 5kΩ		30	40		60		60	ns
Conversion Time (Mode 0)	t_{CRD}			1.6	2.0		2.4		2.8	µs
Data Access Time After RD	t_{ACC1}	(Note 6)			85		110		120	ns
Data Access Time After INT, Mode 0	t_{ACC2}	(Note 6)		20	50		60		70	ns
$\overline{RD}$ to $\overline{INT}$ Delay (Mode 1)	t_{INTH}	C_L = 50pF		40	75		100		100	ns
Data Hold Time	t_{DH}	(Note 7)			60		70		70	ns
Delay Time Between Conversions	t_P				500		500		600	ns
$\overline{RD}$ Pulse Width (Mode 1)	t_{RD}		60		600	80	500	80	400	ns

Note 5: All input control signals are specified with t_R = t_F = 20ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
Note 6: Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4 V.
Note 7: Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Note 8: Guaranteed by design.

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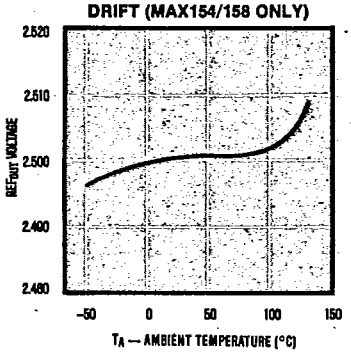
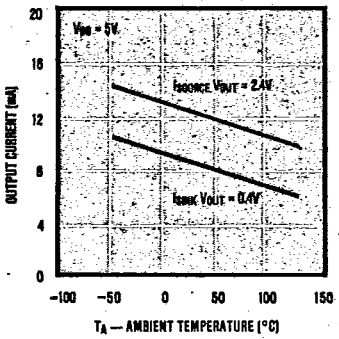
Typical Operating Characteristics

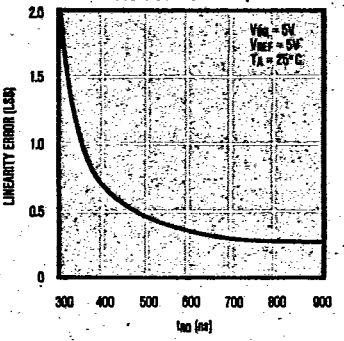
REFERENCE TEMPERATURE DRIFT (MAX154/158 ONLY)



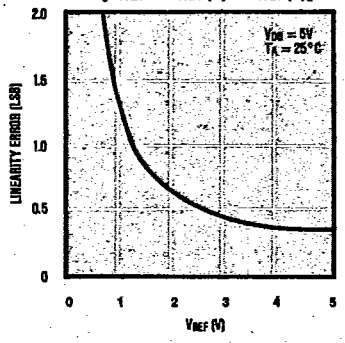
OUTPUT CURRENT vs. TEMPERATURE



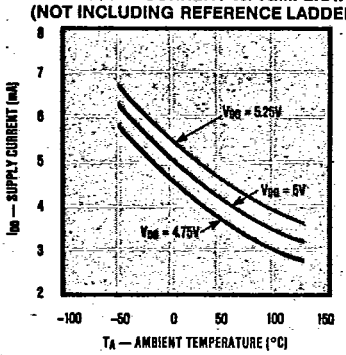
ACCURACY vs. tp



ACCURACY vs. VREF [VREF = VREF(+) - VREF(-)]



POWER SUPPLY CURRENT vs. TEMPERATURE (NOT INCLUDING REFERENCE LADDER)



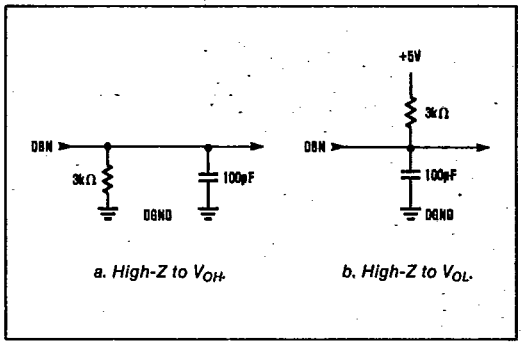


Figure 1. Load Circuits for Data Access Time Test

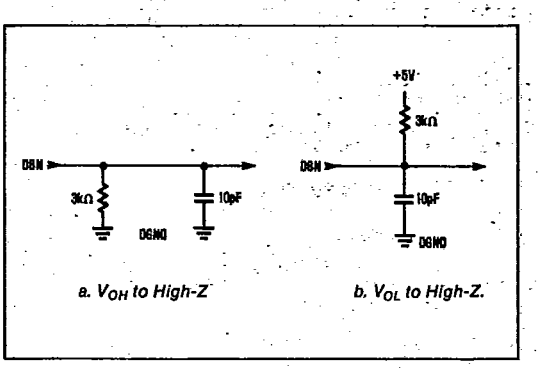


Figure 2. Load Circuits for Data Hold Time Test

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MAX154/AD7824 Pin Description

PIN	NAME	FUNCTION
1	AIN4	Analog input channel 4
2	AIN3	Analog input channel 3
3	AIN2	Analog input channel 2
4	AIN1	Analog input channel 1
5	REFOUT N.C.	Reference output (2.5V) for MAX154 No Connect for AD7824
6	DB0	Three-state data output, bit 0 (LSB)
7	DB1	Three-state data output, bit 1
8	DB2	Three-state data output, bit 2
9	DB3	Three-state data output, bit 3
10	$\overline{RD}$	READ input. $\overline{RD}$ controls conversions and data access. See Digital Interface section.
11	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
12	GND	Ground
13	$V_{REF}(-)$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF}(+)$
14	$V_{REF}(+)$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF}(-)$ to V_{DD}.
15	RDY	READY Output. Open drain output with no active pull-up device. Goes low when $\overline{CS}$ goes low and high impedance at the end of a conversion.
16	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to be selected.
17	DB4	Three-state data output, bit 4
18	DB5	Three-state data output, bit 5
19	DB6	Three-state data output, bit 6
20	DB7	Three-state data output, bit 7 (MSB)
21	A1	Channel Address 1 Input
22	A0	Channel Address 0 Input
23	NC	No Connect
24	V_{DD}	Power supply voltage, +5V

MAX158/AD7828 Pin Description

PIN	NAME	FUNCTION
1	AIN6	Analog input channel 6
2	AIN5	Analog input channel 5
3	AIN4	Analog input channel 4
4	AIN3	Analog input channel 3
5	AIN2	Analog input channel 2
6	AIN1	Analog input channel 1
7	REFOUT N.C.	Reference output (2.5V) for MAX158 No Connect for AD7828
8	DB0	Three-state data output, bit 0 (LSB)
9	DB1	Three-state data output, bit 1
10	DB2	Three-state data output, bit 2
11	DB3	Three-state data output, bit 3
12	$\overline{RD}$	READ input. $\overline{RD}$ controls conversions and data access. See Digital Interface section.
13	$\overline{INT}$	INTERRUPT output. $\overline{INT}$ going low indicates the completion of a conversion. See Digital Interface section.
14	GND	Ground
15	$V_{REF}(-)$	Lower limit of reference span. Sets the zero code voltage. Range: GND to $V_{REF}(+)$
16	$V_{REF}(+)$	Upper limit of reference span. Sets the Full Scale input voltage. Range: $V_{REF}(-)$ to V_{DD}.
17	RDY	READY Output. Open drain output with no active pull-up device. Goes low when $\overline{CS}$ goes low and high impedance at the end of a conversion.
18	$\overline{CS}$	CHIP-SELECT input. $\overline{CS}$ must be low for the device to be selected.
19	DB4	Three-state data output, bit 4
20	DB5	Three-state data output, bit 5
21	DB6	Three-state data output, bit 6
22	DB7	Three-state data output, bit 7 (MSB)
23	A2	Channel Address 2 Input
24	A1	Channel Address 1 Input
25	A0	Channel Address 0 Input
26	V_{DD}	Power supply voltage, +5V
27	AIN8	Analog input channel 8
28	AIN7	Analog input channel 7

CMOS High Speed 8-Bit A/D Converter with Multiplexer and Reference

Detailed Description

Converter Operation

The MAX154/MAX158/AD7824/AD7828 uses what is commonly called a "half-flash" conversion technique (see Figure 3). Two 4-bit flash A/D converter sections are used to achieve an 8-bit result. Using 15 comparators, the upper four bit MS (most significant) flash A/D compares the unknown input voltage to the reference ladder and provides the upper four data bits.

An internal DAC uses the MS bits to generate an analog signal from the first flash conversion. A residue voltage representing the difference between the unknown input and the DAC voltage is then compared to the reference ladder by 15 LS (least significant) flash comparators to obtain the lower four output bits.

Operating Sequence

The operating sequence is shown in Figure 4. A conversion is initiated by a falling edge of RD and CS. The comparator inputs track the analog input voltage for approximately 1μs. After this first cycle the MS flash result is latched into the output buffers and the LS conversion begins. INT goes low approximately 600ns later, indicating the end of the conversion, and that the lower 4 bits are latched into the output buffers. The data can then be accessed using the CS and RD inputs.

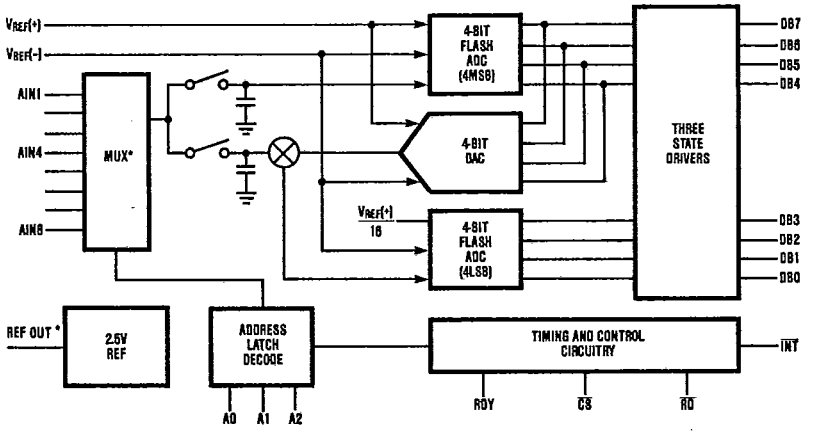
Digital Interface

The MAX154/MAX158 and AD7824/AD7828 use only Chip Select (CS) and Read (RD) as control inputs. A READ operation, taking CS and RD low, latches the multiplexer address inputs and starts a conversion (See Table 1).

Table 1.
Truth Table For Input Channel Selection

MAX154/AD7824 A1	MAX154/AD7824 A0	MAX158/AD7828 A2	MAX158/AD7828 A1	MAX158/AD7828 A0	SELECTED CHANNEL
0	0	0	0	0	AIN1
0	1	0	0	1	AIN2
1	0	0	1	0	AIN3
1	1	0	1	1	AIN4
		1	0	0	AIN5
		1	0	1	AIN6
		1	1	0	AIN7
		1	1	1	AIN8

There are two interface modes which are determined by the length of the RD input. Mode 0, implemented by keeping RD low until the conversion ends, is designed for microprocessors that can be forced into a WAIT state. In this mode, a conversion is started with a READ operation (taking CS and RD low) and data is read when the conversion ends. Mode 1 on the other hand does not require microprocessor WAIT states. A READ operation simultaneously initiates a conversion and reads the previous conversion result.



*MAX154/AD7824 — 4 Channel Mux
MAX158/AD7828 — 8 Channel Mux
REFOUT on MAX154/MAX158 only

Figure 3. Functional Diagram

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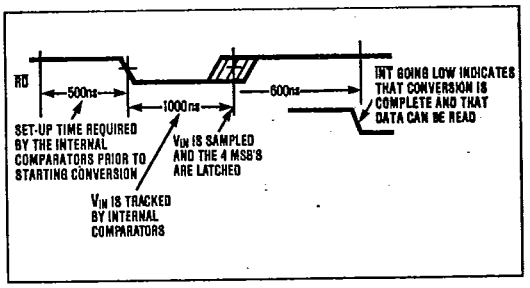

Figure 4. Operating Sequence

Interface Mode 0

Figure 5 shows the timing diagram for Mode 0 operation. This is used with microprocessors that have WAIT state capability, whereby a READ instruction is extended to accomodate slow memory devices. Taking $\overline{CS}$ and $\overline{RD}$ low latches the analog multiplexer address and starts a conversion. Data outputs DB0-DB7 remain in the high impedance condition until the conversion is complete.

There are two status outputs, Interrupt ($\overline{INT}$) and Ready (RDY). RDY, an open drain output (no internal pull-up device), is connected to the processor's READY/$\overline{WAIT}$ input. RDY goes low on the falling edge of $\overline{CS}$ and goes high impedance at the end of the conversion, when the conversion result appears on the data outputs. If the RDY output is not required, its external pull-up resistor can be omitted. $\overline{INT}$ goes low when the conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

Interface Mode 1

Mode 1 is designed for applications where the microprocessor is not forced into a WAIT state. Taking $\overline{CS}$ and $\overline{RD}$ low latches the multiplexer address and starts a conversion (See Figure 6). Data from the previous conversion is immediately read from the outputs (DB0-DB7).

$\overline{INT}$ goes high at the rising edge of $\overline{CS}$ or $\overline{RD}$ and goes low at the end of the conversion. A second READ operation is required to read the result of this conversion. The second READ latches a new multiplexer address and starts another conversion. A delay of 2.5μs must be allowed between READ operations. RDY goes low on the falling edge of $\overline{CS}$ and goes high impedance at the rising edge of $\overline{CS}$. If RDY is not needed, its external pull-up resistor can be omitted.

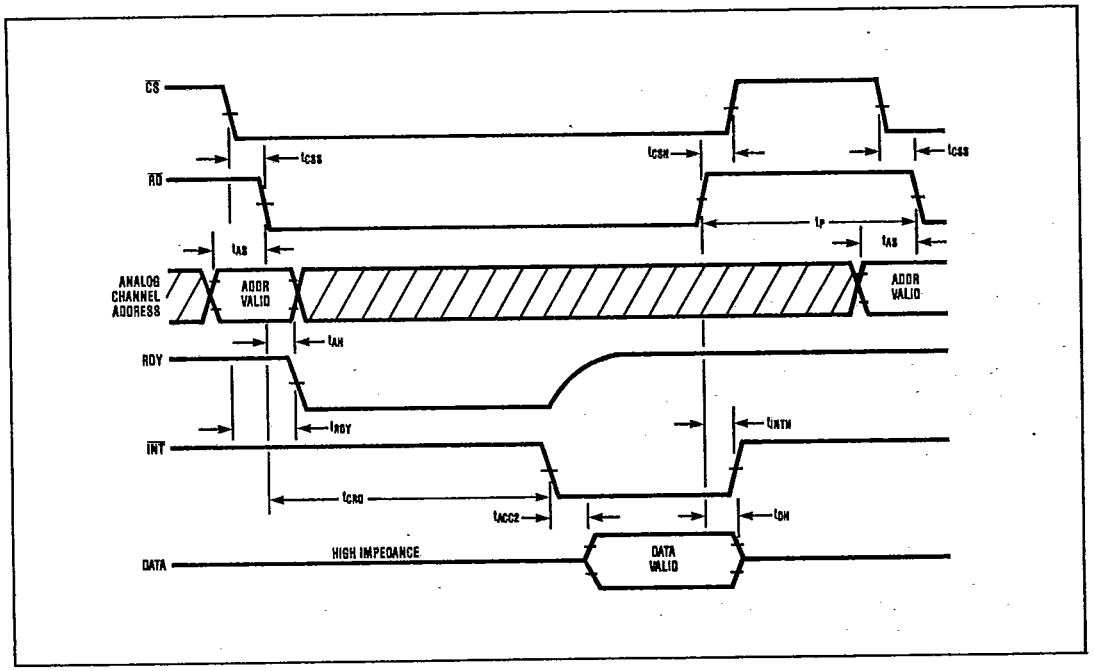

Figure 5. Mode 0 Timing Diagram

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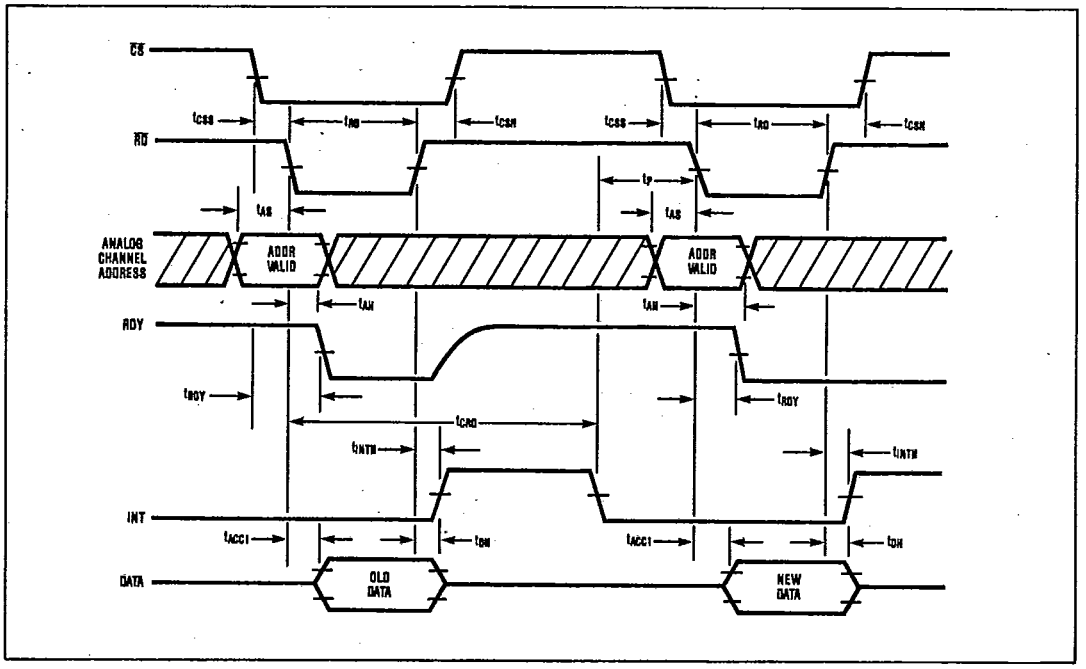

Figure 6. Mode 1 Timing Diagram

Analog Considerations

Reference and Input

The $V_{REF}(+)$ and $V_{REF}(-)$ inputs of the converter define the zero and the full-scale of the ADC. In other words, the voltage at $V_{REF}(-)$ is equal to the input voltage which produces an output code of all zeroes and the voltage at $V_{REF}(+)$ is equal to input voltage which produces an output code of all ones (see Figure 7).

Figure 8 shows some possible reference configurations. For the MAX154/MAX158, a 0.01μF bypass capacitor to GND should be used to reduce the high frequency output impedance of the internal reference. Larger capacitors should not be used as this degrades the stability of the reference buffer. The 2.5V reference output is with respect to the GND pin.

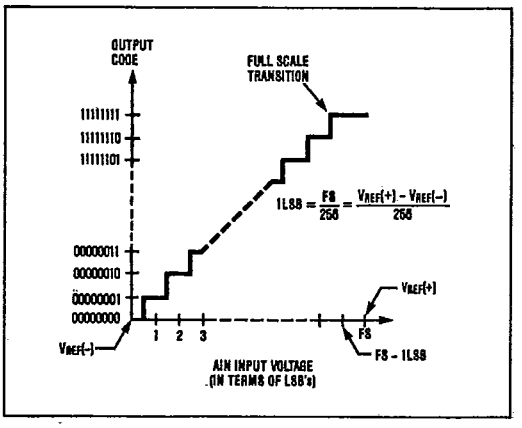

Figure 7. Transfer Function

Bypassing

A 47μF electrolytic and 0.1μF ceramic capacitor should be used to bypass the V_{DD} pin to GND. These capacitors must have minimum lead length since excess lead length may contribute to conversion errors and instability. If the reference inputs are driven by long lines, they should be bypassed to GND with 0.1μF capacitors at the reference input pins.

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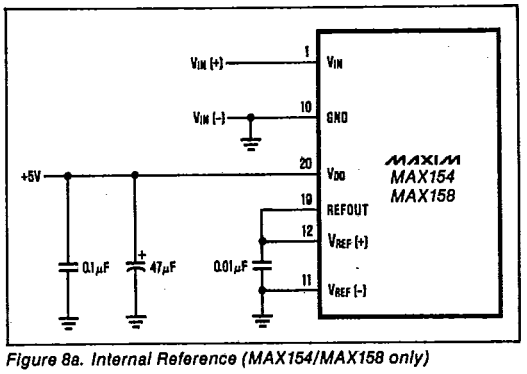

Figure 8a. Internal Reference (MAX154/MAX158 only)

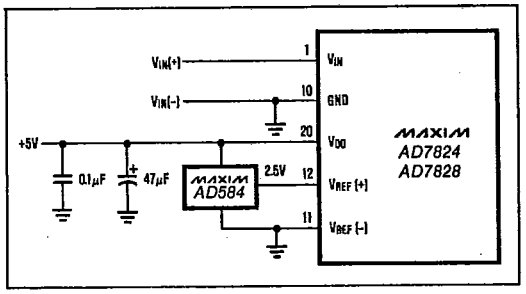

Figure 8b. External Reference +2.5V Full-Scale

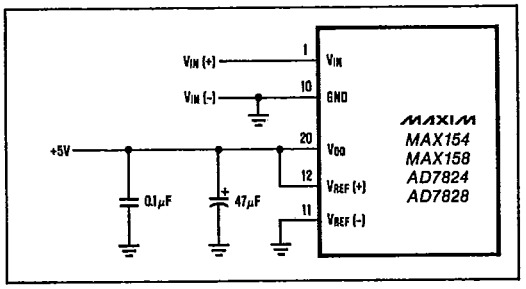

Figure 8c. Power Supply as Reference

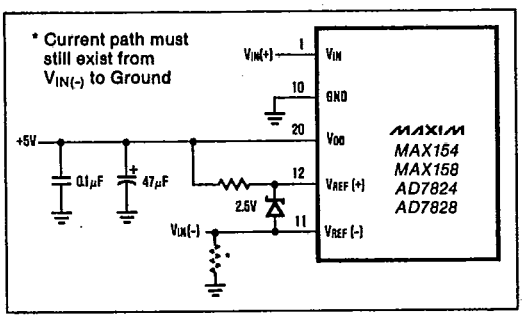

Figure 8d. Inputs Not Referenced to GND

Input Current

The converters' analog inputs behave somewhat differently from conventional ADCs. The sampled data comparators take varying amounts of current from the input depending on the cycle they are in. The equivalent circuit of the converter is shown in Figure 9a. When the conversion starts AIN(n) is connected to the MS and LS comparators. Thus, AIN(n) is connected to thirty-one 1pF capacitors.

To acquire the input signal in approximately 1µs, the input capacitors must charge to the input voltage through the on resistance of the multiplexer (about 600Ω) and the comparator's analog switches (2kΩ to 5kΩ per comparator). In addition, about 12pF of stray capacitance must be charged. The input can be modelled as an equivalent RC network shown in Figure 9b. As R_S (source impedance) increases, the capacitors take longer to charge.

Since the length of the input acquisition time is internally set, large source resistances (greater than 100Ω) will cause settling errors. The output impedance of an op-amp is its open loop output impedance divided by the loop gain at the frequency of interest. It is important that the amplifier driving the converter input have sufficient loop gain at approximately 1MHz to maintain low output impedance.

Input Filtering

The transients in the analog input caused by the sampled data comparators do not degrade the converter's performance since the A/D does not "look" at the input when these transients occur. The comparator's outputs track the input during the first 1µs of the conversion, and are then latched. Therefore, at least 1µs will be provided to charge the ADC's input capacitance. It is not necessary to filter these transients with an external capacitor on the AIN terminals.

Sinusoidal Inputs

The MAX154/MAX158 and AD7824/AD7828 can measure input signals with slew rates as high as 157mV/µs to the rated specifications. This means that the analog input frequency can be as high as 10kHz without the aid of an external track-and-hold. The maximum sampling rate is limited by the conversion time (typical t_{CRD} = 2µs) plus the time required between conversions (t_P = 500ns). It is calculated as:

$$f_{MAX} = \frac{1}{t_{CRD} + t_P} = \frac{1}{(2.0 + 0.5)\ \mu s} = 400kHz$$

f_{MAX} permits a maximum sampling rate of 50kHz per channel when using the MAX158/AD7828 and 100kHz per channel when using the MAX154/AD7824. These rates are well above the Nyquist requirement of 20kHz sampling rate for a 10kHz input bandwidth.

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Bipolar Input Operation

The circuit in Figure 10a. can be used for bipolar input operation. The input voltage is scaled by an amplifier so that only positive voltages appear at the ADC's inputs. An external reference should be used for the AD7824/AD7828 but is not needed with the MAX154/MAX158. The analog input range is ±4V and the output code is complementary offset binary. The ideal input/output characteristic is shown in Figure 10b.

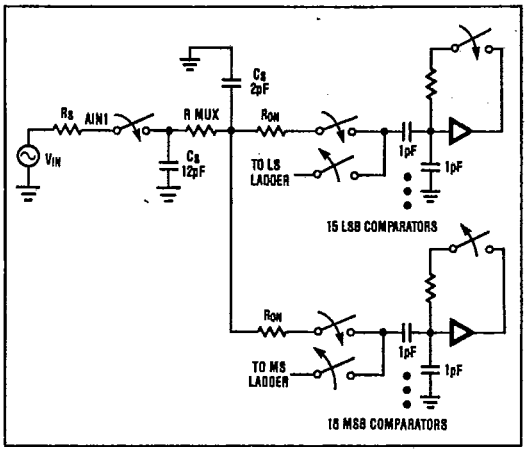

Figure 9a. Equivalent Input Circuit

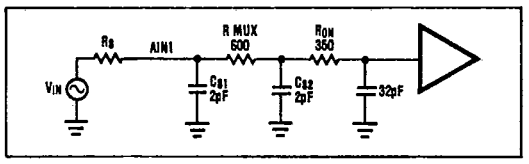

Figure 9b. RC Network Model

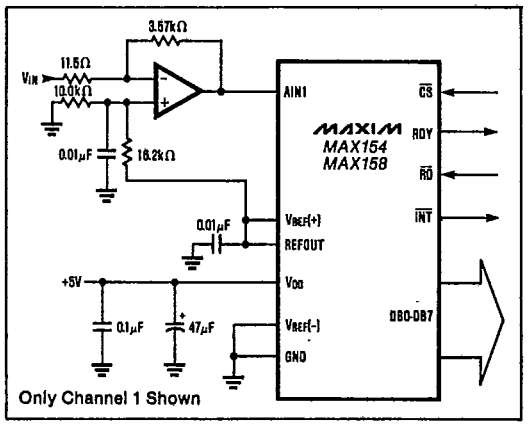

Figure 10a. Bipolar ±4V Input Operation

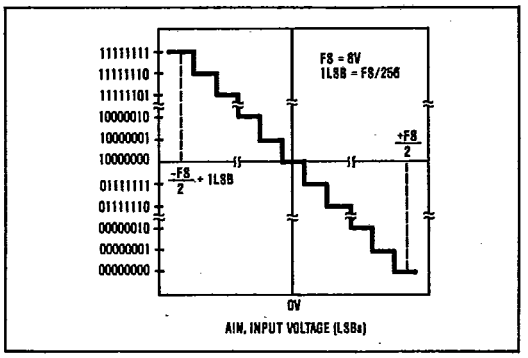

Figure 10b. Transfer Function for ±4V Input Operation

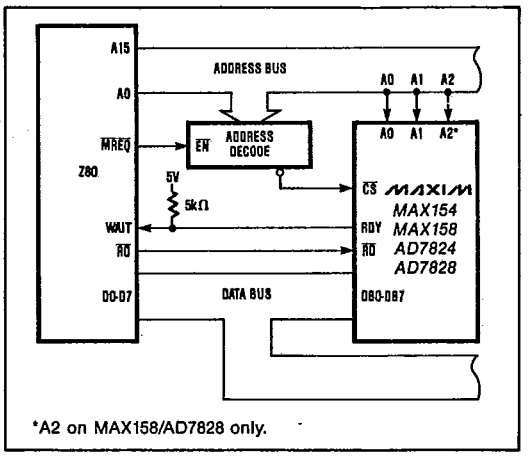

Figure 11. Simple Mode 0 Interface

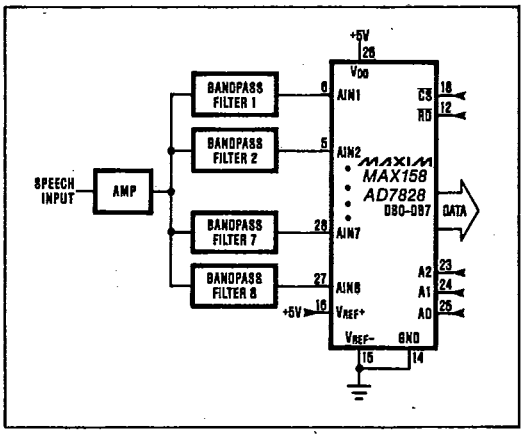

Figure 12. Speech Analysis Using Real Time Filtering

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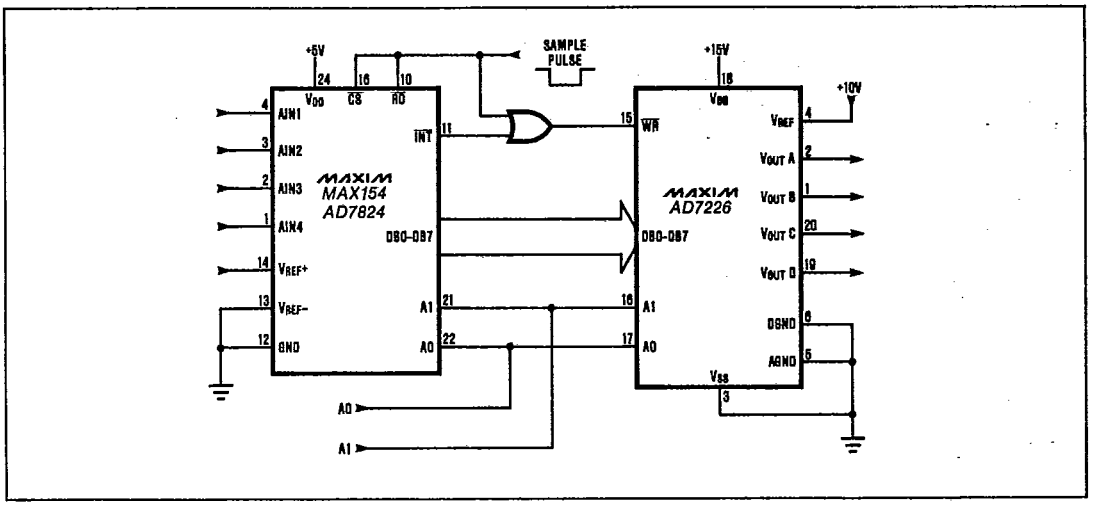
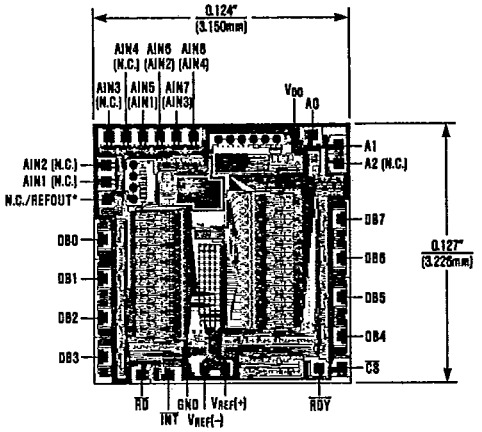


Figure 13. 4-Channel Fast Sample and Infinite Hold

Chip Topography



Note: Connections in parentheses ( ) are for MAX154/AD7824
* REFOUT on MAX154/MAX158 only

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Ordering Information (continued)

PART	TEMP RANGE	PACKAGE*	ERROR
MAX158ACPI	0° C to +70° C	Plastic DIP	±½ LSB
MAX158BCPI	0° C to +70° C	Plastic DIP	±1 LSB
MAX158BC/D	0° C to +70° C	Dice	±1 LSB
MAX158ACWI	0° C to +70° C	Small Outline	±½ LSB
MAX158BCWI	0° C to +70° C	Small Outline	±1 LSB
MAX158AEPI	-40° C to +85° C	Plastic DIP	±½ LSB
MAX158BEPI	-40° C to +85° C	Plastic DIP	±1 LSB
MAX158AEWI	-40° C to +85° C	Small Outline	±½ LSB
MAX158BEWI	-40° C to +85° C	Small Outline	±1 LSB
MAX158AMDI	-55° C to +125° C	CERDIP	±½ LSB
MAX158BMDI	-55° C to +125° C	CERDIP	±1 LSB
AD7824LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7824KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7824LCWG	0° C to +70° C	Small Outline	±1 LSB
AD7824KCWG	0° C to +70° C	Small Outline	±½ LSB
AD7824CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7824BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7824UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7824TQ	-55° C to +125° C	CERDIP	±1 LSB
AD7828LN	0° C to +70° C	Plastic DIP	±½ LSB
AD7828KN	0° C to +70° C	Plastic DIP	±1 LSB
AD7828LCWI	0° C to +70° C	Small Outline	±1 LSB
AD7828KCWI	0° C to +70° C	Small Outline	±½ LSB
AD7828CQ	-25° C to +85° C	CERDIP	±½ LSB
AD7828BQ	-25° C to +85° C	CERDIP	±1 LSB
AD7828UQ	-55° C to +125° C	CERDIP	±½ LSB
AD7828TQ	-55° C to +125° C	CERDIP	±1 LSB

* *MAX154/AD7824 — 24 lead package,*
MAX158/AD7828 — 28 lead package