ANALOG DEVICES

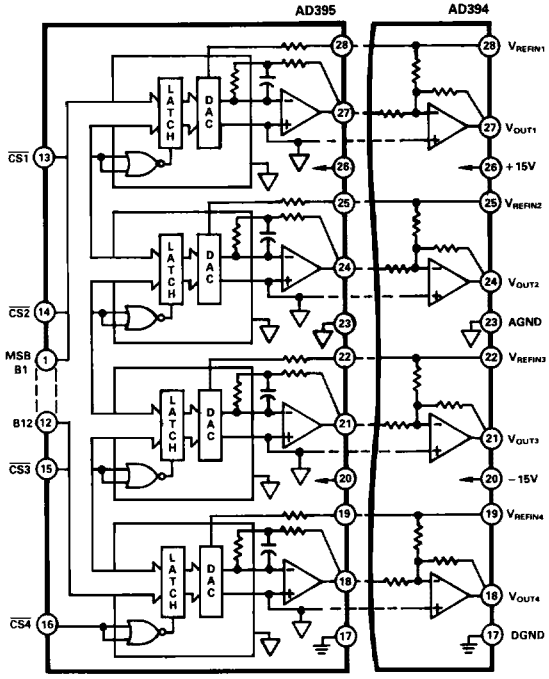
μP-Compatible Multiplying Quad 12-Bit D/A Converters

AD394/AD395

FEATURES

- Four Complete 12-Bit CMOS DACs with Buffer Registers
- Linearity Error ±1/2LSB T_{min}-T_{max} (AD394, AD395K,T)
- Factory-Trimmed Gain and Offset
- Precision Output Amplifiers for V_{OUT}
- Full Four Quadrant Multiplication per DAC
- Monotonicity Guaranteed Over Full Temperature Range
- Fast Settling: 15μs Max to ±1/2LSB
- Available to MIL-STD-883 (See ADI Military Catalog)

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT DESCRIPTION

The AD394 and AD395 contain four 12-bit, high-speed, low power, voltage output multiplying digital-to-analog converters in a compact 28-pin hybrid package. The design is based on a proprietary latched 12-bit CMOS DAC chip which reduces chip count and provides high reliability. The AD394 and AD395 both are ideal for systems requiring digital control of many analog voltages where board space is at a premium and low power consumption a necessity. Such applications include automatic test equipment, process controllers, and vector stroke displays.

Both the AD394 and the AD395 are laser-trimmed to ±1/2LSB max differential and integral linearity (AD394, AD395K,T) and full scale accuracy of ±0.05 percent at 25°C. The high initial accuracy is made possible by the use of precision laser trimmed thin-film scaling resistors.

The individual DAC registers are accessed by the $\overline{CS1}$ through $\overline{CS4}$ control pins. These control signals allow any combination of the DAC select matrix to occur (see Table III). Once selected, the DAC is loaded with a single 12-bit wide word. The 12-bit parallel digital input interfaces to most 12- and 16-bit bus systems.

The AD394 outputs (V_{REFIN} = +10V) provide a ±10V bipolar output range with positive-true offset binary input coding. The AD395 outputs (V_{REFIN} = −10V) provide a 0V to +10V unipolar output range with straight binary input coding.

Both the AD394 and the AD395 are packaged in a 28-lead ceramic package and are available for operation over the 0 to +70°C and −55°C to +125°C temperature range.

PRODUCT HIGHLIGHTS

1. The AD394, AD395 offer a dramatic reduction in printed circuit board space in systems using multiple DACs.
2. The use of CMOS DACs provides low power consumption.
3. Each DAC is independently addressable, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level-triggered.
4. The output voltage is trimmed to a full scale accuracy of ±0.05%. Settling time to ±1/2LSB is 15 microseconds maximum.
5. Maximum gain TC of 5ppm/°C is achievable by both the AD394 and the AD395.
6. The monolithic CMOS DAC chips provide excellent linearity and guaranteed monotonicity over the full operating temperature range.
7. The 28-pin double-width hybrid package provides extremely high functional density.
8. Two or four quadrant multiplication can be achieved simply by applying the appropriate input voltage signal to the selected DAC's reference (V_{REFIN}).
9. Both the AD394S,TD and AD395S,TD feature guaranteed accuracy and linearity over the −55°C to +125°C temperature range.

AD394/AD395—SPECIFICATIONS (T_A = +25°C, V_{REFIN} = 10V, V_S = ±15V unless otherwise specified)

Model	AD394JD/SD[1] AD395JD/SD MIN	TYP	MAX	AD394KD/TD[1] AD395KD/TD MIN	TYP	MAX	UNITS
DATA INPUTS (Pins 1-16)[2]							
TTL or 5 Volt CMOS Compatible							
Input Voltage							
Bit ON (Logic "1")	+2.4		+5.5	+2.4		+5.5	V
Bit OFF (Logic "0")	0		+0.8	0		+0.8	V
Input Current		±4	±40		±4	±40	μA
RESOLUTION			12			12	Bits
OUTPUT							
Voltage Range[3]							
AD394		$\pm V_{REFIN}$			$\pm V_{REFIN}$		V
AD395		0V to $-(V_{REFIN})$			0V to $-(V_{REFIN})$		V
Current	5			5			mA
STATIC ACCURACY							
Gain Error		±0.05	±0.1		±0.025	±0.05	% of FSR[4]
Offset		±0.025	±0.05		±0.012	±0.025	% of FSR
Bipolar Zero (AD394)		±0.025			±0.012		% of FSR
Integral Linearity Error[5]		±1/4	±3/4		±1/8	±1/2	LSB
Differential Linearity Error		±1/2	±3/4		±1/4	±1/2	LSB
TEMPERATURE PERFORMANCE							
Gain Drift			±10			±5	ppm FSR/°C
Offset Drift			±10			±5	ppm FSR/°C
Integral Linearity Error[5]							
T_{min} to T_{max}		±1/2	±3/4		±1/4	±1/2	LSB
Differential Linearity Error	MONOTONICITY GUARANTEED OVER FULL TEMPERATURE RANGE						
REFERENCE INPUTS							
Input Resistance	5		25	5		25	kΩ
Voltage Range	−11		+11	−11		+11	V
DYNAMIC PERFORMANCE							
Settling Time (to ±1/2LSB)							
V_{REFIN} = +10V, Change All Digital							
Inputs from +5.0V to 0V		10	15		10	15	μs
V_{REFIN} = 0 to 5V Step,							
All Digital Inputs = 0V		10	15		10	15	μs
Reference Feedthrough Error[6]							
AD395		5			5		mV p-p
AD394		See Figure 1			See Figure 1		
Digital-to-Analog Glitch Impulse[7]		250			250		nV·sec
Crosstalk							
Digital Input (Static)[8]		0.1			0.1		LSB
Reference[9]		2.0			2.0		mV p-p
POWER REQUIREMENTS							
Supply Voltage[10]	±13.5		±16.5	±13.5		±16.5	V
Current (All Digital Inputs 0V or +5V)							
$+V_S$		20	28		20	28	mA
$-V_S$		18	22		18	22	mA
Power Dissipation		570	750		570	750	mW
POWER SUPPLY GAIN SENSITIVITY							
$+V_S$		0.002	0.006		0.002	0.006	%FS/%
$-V_S$		0.0025	0.006		0.0025	0.006	%FS/%
TEMPERATURE RANGE							
Operating (Full Specifications) J, K	0		+70	0		+70	°C
S, T	−55		+125	−55		+125	°C
Storage	−65		+150	−65		+150	°C

NOTES
[1]AD394 and AD395 S and T grades are available to MIL-STD-883, Method 5008, Class B. See Analog Devices Military Catalog for proper part number and detail specification.
[2]Timing specifications appear in Table IV and Figure 5.
[3]Code tables and graphs appear on Theory of Operation page.
[4]FSR means Full Scale Range and is equal to 20V for a ±10V bipolar range and 10V for 0 to 10V unipolar range.
[5]Integral nonlinearity is a measure of the maximum deviation from a straight line passing though the endpoints of the DAC transfer function.
[6]For AD395 (unipolar), DAC register loaded with 0000 0000 0000, V_{REFIN} = 20V p-p, 10kHz sinewave. For AD394 (bipolar), V_{REFIN} = 20V p-p, 60 and 400Hz.
[7]This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nVs and is measured with V_{REFIN} = AGND.
[8]Digital crosstalk is defined as the change in any one output's steady state value as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} into a 2kΩ load by means of varying the digital input code.
[9]Reference crosstalk is defined as the change in any one output as a result of any other output being driven from V_{OUTMIN} to V_{OUTMAX} @10kHz into a 2kΩ load by means of varying the amplitude of the reference signal.
[10]The AD394 and the AD395 can be used with supply voltages as low as ±11.4V, Figure 10.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

$+V_S$ to DGND	−0.3V to +17V
$-V_S$ to DGND	+0.3V to −17V
Digital Inputs (Pins 1-16) to DGND	−0.3V to +7V
V_{REFIN} to DGND	±25V
AGND to DGND	±0.6V
Analog Outputs (Pins 18, 21, 24, 27)	Indefinite Short to AGND or DGND; Momentary Short to $\pm V_S$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

2

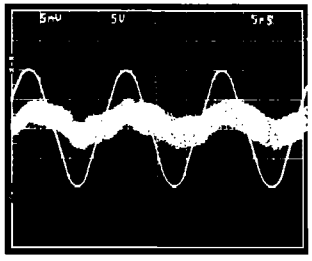


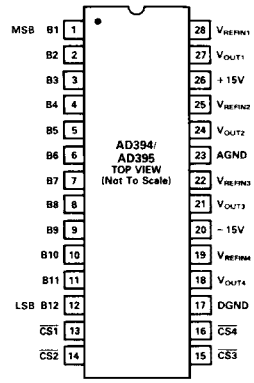
Figure 1. AD394 Feedthrough V_{REFIN} = 60Hz (top photo) and 400Hz (bottom photo) Sinewave. Digital code is set at 1000 000 0000.
SCALE: Reference Input 5V/DIV (Thin Trace)
Feedthrough Output 5mV/DIV
TIME: Top Photo 5ms/DIV
Bottom Photo 500µs DIV

MIL-STD-883

The rigors of the military/aerospace environment, temperature extremes, humidity, mechanical stress, etc., demand the utmost in electronic circuits. The AD394, AD395, with the inherent reliability of integrated circuit construction, were designed with these applications in mind. The hermetically-sealed, low profile DIP package takes up a fraction of the space required by equivalent modular designs and protect the chips from hazardous environments. To further insure reliability, the AD394, AD395 are both fully compliant to MIL-STD-883 Class B, Method 5008.

Consult Analog Devices Military Catalog for proper ordering part number and detail specification.

PIN CONFIGURATION



ORDERING GUIDE

Model	Temperature Range	Gain Error	Linearity Error T_{min}-T_{max}	Package Option*
AD394JD	0 to +70°C	±4LSB	±3/4LSB	DH-28A
AD395JD	0 to +70°C	±4LSB	±3/4LSB	DH-28A
AD394KD	0 to +70°C	±2LSB	±1/2LSB	DH-28A
AD395KD	0 to +70°C	±2LSB	±1/2LSB	DH-28A
AD394SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28A
AD395SD	−55°C to +125°C	±4LSB	±3/4LSB	DH-28A
AD394TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28A
AD395TD	−55°C to +125°C	±2LSB	±1/2LSB	DH-28A

*DH-28A = Ceramic DIP. For outline information see Package Information section.

AD394/AD395—Theory of Operation

The AD394 quad DAC provides four-quadrant multiplication. It is a hybrid IC comprised of four monolithic 12-bit CMOS multiplying DACs and eight precision output amplifiers. Each of the four independent-buffered channels has an independent reference input capable of accepting a separate dc or an ac signal for multiplying or for function generation applications. The CMOS DACs act as digitally programmable attenuators when used with a varying input signal or, if used with a fixed dc reference, the DAC would act as a standard bipolar output DAC. In addition, each DAC has a 12-bit wide data latch to buffer the converter when connected to a microprocessor data bus.

The AD395 quad DAC provides two-quadrant multiplication and is comprised of four 12-bit CMOS multiplying DACs and four precision output amplifiers. The two-quadrant-multiplication function arises from a straight-binary digital input multiplied by a bipolar analog input which results in two-quadrant multiplication. The AD395 can also operate as a standard unipolar DAC when a fixed dc reference is applied to V_{REFIN}.

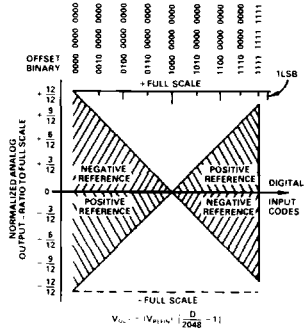


Figure 2. AD394 as a Four-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$+1\times(V_{REFIN})\left\{\frac{2047}{2048}\right\}$	+9.9951V	+FULL SCALE – 1LSB
1100	0000	0000	$+1\times(V_{REFIN})\left\{\frac{1024}{2048}\right\}$	+5.000V	+1/2 SCALE
1000	0000	0001	$+1\times(V_{REFIN})\left\{\frac{1}{2048}\right\}$	+4.88mV	+1LSB
1000	0000	0000	$+1\times(V_{REFIN})\left\{\frac{0}{2048}\right\}$	+0.000V	ZERO
0111	1111	1111	$-1\times(V_{REFIN})\left\{\frac{1}{2048}\right\}$	-4.88mV	-1LSB
0100	0000	0000	$-1\times(V_{REFIN})\left\{\frac{1024}{2048}\right\}$	-5.000V	-1/2 SCALE
0000	0000	0000	$-1\times(V_{REFIN})\left\{\frac{2048}{2048}\right\}$	-10.000V	-FULL SCALE

Table I. AD394 Bipolar Code Table

MULTIPLYING MODE

The figures below show the transfer function for each model. The diagrams indicate an area over which many different combinations of the reference input and digital input can result in a particular analog output voltage. The highlighted transfer line in each diagram indicates the transfer function if a fixed reference is at the input. The digital codes above each diagram indicate the mid and endpoints of each function. The relationship between the reference input (V_{REFIN}) the digital input code and the analog output is given in Tables I and II below. Note that the reference input signal sets the slope of the transfer function (and determines the full scale output at code 111 . . 111) while the digital input selects the horizontal position in each diagram.

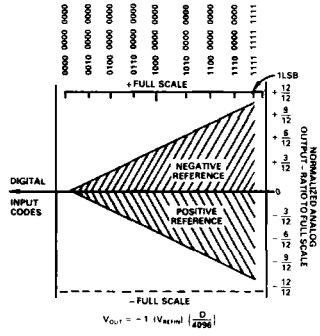


Figure 3. AD395 as a Two-Quadrant Multiplier of Reference Input and Digital Input

DATA INPUT			ANALOG OUTPUT	ANALOG OUTPUT VOLTAGE V_{REFIN} = +10 VOLTS	
1111	1111	1111	$-1\times(V_{REFIN})\left\{\frac{4095}{4096}\right\}$	-9.9976V	-FULL SCALE – 1LSB
1000	0000	0000	$-1\times(V_{REFIN})\left\{\frac{2048}{4096}\right\}$	-5.000V	-1/2 SCALE
0000	0000	0001	$-1\times(V_{REFIN})\left\{\frac{1}{4096}\right\}$	-2.44mV	-1LSB
0000	0000	0000	$-1\times(V_{REFIN})\left\{\frac{0}{4096}\right\}$	0.000V	ZERO

Table II. AD395 Unipolar Code Table

DATA AND CONTROL SIGNAL FORMAT

The AD394 and AD395 accept 12-bit parallel data in response to control signals $\overline{CS1}$-$\overline{CS4}$. As detailed in Table III, the four chip select lines are used to address the DAC register of interest. It is permissible to have more than one chip select active at any time. If $\overline{CS1}$-$\overline{CS4}$ are all brought low coincident, all four DAC outputs will be updated to the value located on the data bus. All control inputs are level-triggered and may be hard-wired low to render any register (or group of registers) transparent.

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	Operation
1	1	1	1	All DACs Latched
0	1	1	1	Load DAC 1 From Data Bus
1	0	1	1	Load DAC 2 From Data Bus
1	1	0	1	Load DAC 3 From Data Bus
1	1	1	0	Load DAC 4 From Data Bus
0	0	0	0	All DACs Simultaneously Loaded

Table III. DAC Select Matrix

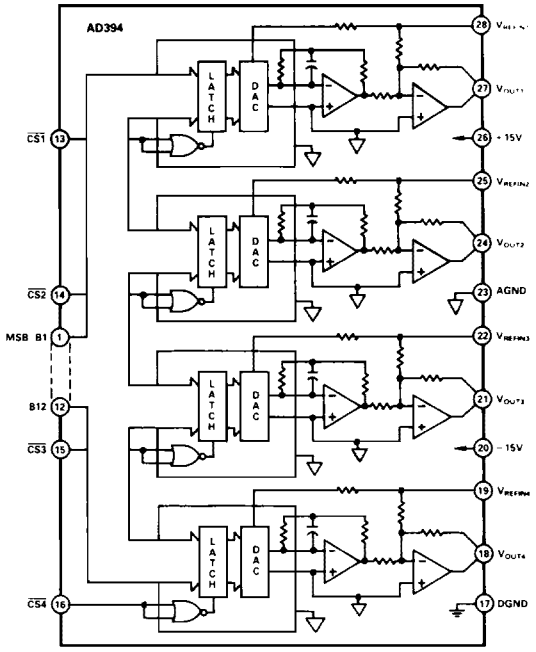


Figure 4. AD394 (Bipolar) Functional Block Diagram

TIMING

The AD394, AD395 control signal timing is very straightforward. $\overline{CS1}$-$\overline{CS4}$ must maintain a minimum pulsewidth of at least 170ns for a desired operation to occur. When loading data from a bus into a 12-bit wide data latch, the data must be stable for at least 150ns before returning CS to a high state. When the $\overline{CS}$ is low, the data latch is transparent allowing the data at the input to propagate through to the DAC. Data can change immediately after the chip select returns high. DAC settling time is measured from the falling edge of the active chip select.

Symbol	Parameter	T_{min} to T_{max}	Units
t_{CS}	Chip Select Pulse Width	170	ns min
t_{DA}	Data Access Time	0	ns min
t_{DS}	Data Set-Up Time	150	ns min
t_{DH}	Data Hold Time	5	ns min

Table IV. AD394, AD395 Timing Specifications

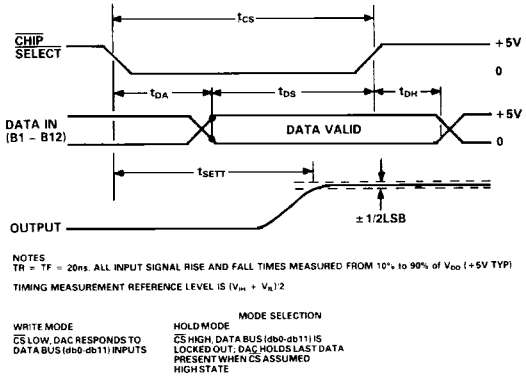


Figure 5. Timing Diagram

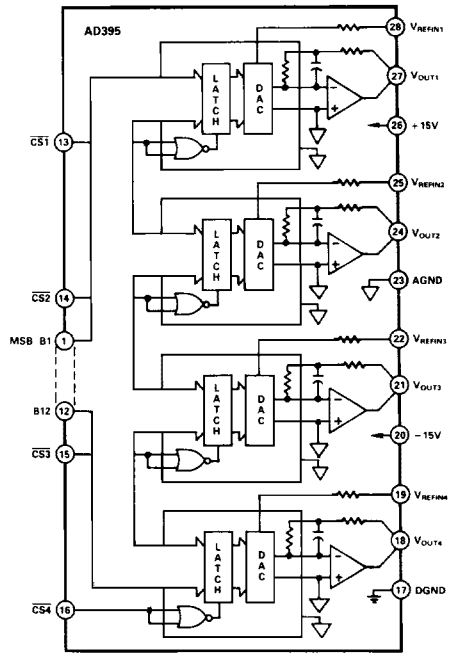


Figure 6. AD395 (Unipolar) Functional Block Diagram

AD394/AD395—Analog Circuit Details

GROUNDING RULES

The AD394 and AD395 include two ground connections in order to minimize system accuracy degradation arising from grounding errors. The two ground pins are designated DGND (pin 17) and AGND (pin 23). The DGND pin is the return for the supply currents of the AD394, AD395 and serves as the reference point for the digital input thresholds. Thus DGND should be connected to the same ground as the circuitry which drives the digital inputs.

Pin 23, AGND, is the high-quality analog ground connection. This pin should serve as the reference point for all analog circuitry associated with the AD394, AD395. It is recommended that any analog signal path carrying significant currents have its own return connection to pin 23 as shown in Figure 7.

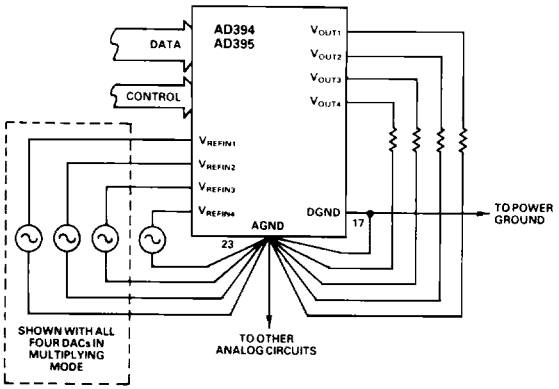


Figure 7. Recommended Ground Connections

Several complications arise in practical systems, particularly if the load is referred to a remote ground. These complications include dc gain errors due to wiring resistance between DAC and load, noise due to currents from other circuits flowing in power ground return impedances, and offsets due to multiple load currents sharing the same signal ground returns. While the DAC outputs are accurately developed between the output pin and pin 23 (AGND), delivering these signals to remote loads

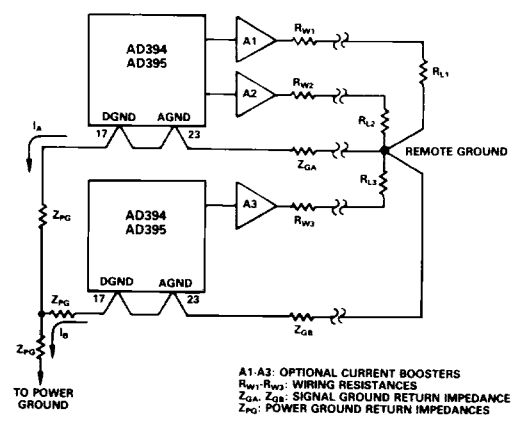


Figure 8. Grounding Errors in Multiple-AD394, AD395 Systems

can be a problem. These problems are compounded if a current booster stage is used, or if multiple AD394, AD395 packages are used. Figure 8 illustrates the parasitic impedances which influence output accuracy.

An output buffer configured as a subtractor as shown in Figure 9 can greatly reduce these errors. First, the effects of voltage drops in wiring resistances is eliminated by sensing the voltage directly at the load with R4. The voltage drops caused by currents flowing through Z_{GA} are eliminated by sensing the remote ground directly with R3. Resistors R1 through R4 should be well matched in order to achieve maximum rejection of the voltage appearing across Z_{GA}. Resistors matched to within one percent (including the effects of R_{W2} and R_{W3}) will reduce ground interaction errors by a factor of 100.

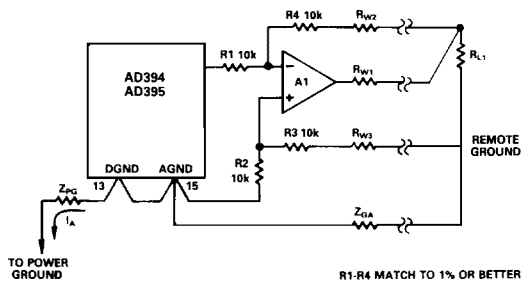


Figure 9. Use of Subtractor Amplifier to Preserve Accuracy

OPERATION FROM ±12 VOLT SUPPLIES

The AD394, AD395 may be used with ±12 volt ±5% power supplies if certain conditions are met. The most important limitation is the output swing available from the output op amps. These amplifiers are capable of swinging only as far as 3 volts from either supply. Thus, the normal ±10 volt output range cannot be used. Changing the output scale is accomplished by changing the reference voltage. With a supply of ±11.4 volts (5% less than ±12V), the output range is restricted to a maximum ±8.4V swing. It may be useful to scale the output at ±8.192 volts (yielding a scale factor of 4 millivolts per LSB).

Figure 10 shows a suggested circuit to set up a ±8.192V output range. To help prevent poor gain drift due to possible mismatch between R_{IN} and $R_{THEVENIN}$ of divider network it is recommended to buffer the potentiometer wiper voltage with an OP-07.

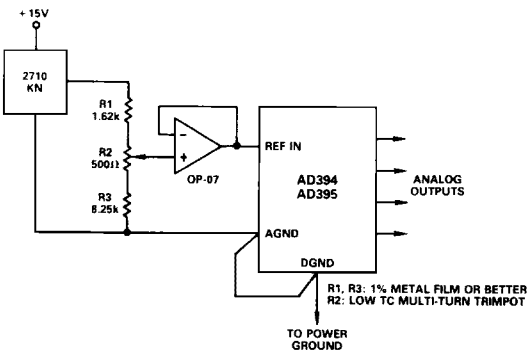


Figure 10. Connections for ±8.192V Full Scale (Recommended for ±12V Power Supplies)

POWER SUPPLY DECOUPLING

The power supplies used with the AD394, AD395 should be well filtered and regulated. Local supply decoupling consisting of a 10μF tantalum capacitor in parallel with 0.1μF ceramic is suggested. The decoupling capacitors should be connected between the AD394 supply pins and the AGND pin. If an output booster is used, its supplies should also be decoupled to the load ground.

IMPROVING FULL-SCALE STABILITY

In large systems using multiple DACs, it may be desirable for all devices to share a common reference. A precision reference can greatly improve system accuracy and temperature stability.

The AD2710 is a suitable reference source for such systems. It features a guaranteed maximum temperature coefficient of ±1ppm/°C. The combination of the AD2710LN and AD394, AD395 shown in Figure 11 will yield a multiple-DAC system with maximum full-scale drift of ±6ppm/°C and excellent tracking.

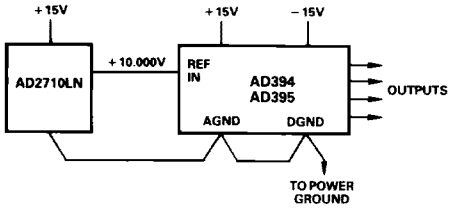


Figure 11. Low Drift AD394, AD395 Configuration

Applications

INTERFACING THE AD394, AD395 TO MICROPROCESSORS

The AD394, AD395 control logic provides simple interface to microprocessors. The individual latches allow for multi-DAC interfacing to a single data bus.

16-BIT PROCESSORS

The AD394, AD395 are 12-bit resolution DAC systems and are easily interfaced to 16-bit wide data buses. Several possible addressing configurations exist.

In the circuit of Figure 12, a system write signal is used to control the decoded address lines and a 74LS139 decoder driven from the least significant address bits provides the active-low $\overline{CS1}$ through $\overline{CS4}$ signals. In the circuit of Figure 12, address lines A0 and A1 each select a single DAC of the four contained in the AD394 or AD395. The use of a separate address line for each DAC allows several DACs to be accessed simultaneously. The address lines are gated by the simultaneous occurrence of a system $\overline{WR}$ and the appropriately decoded base address.

In the addressing scheme shown, A0 represents the least significant word address bit. Data may reside in either the 12MSBs (left-justified) or the 12LSBs (right-justified). Left justification is useful when the data word represents a binary fraction of full scale, while right-justified data usually represents an integer value between 0 and 4095.

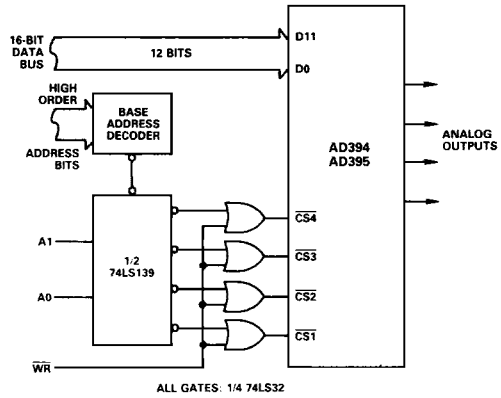
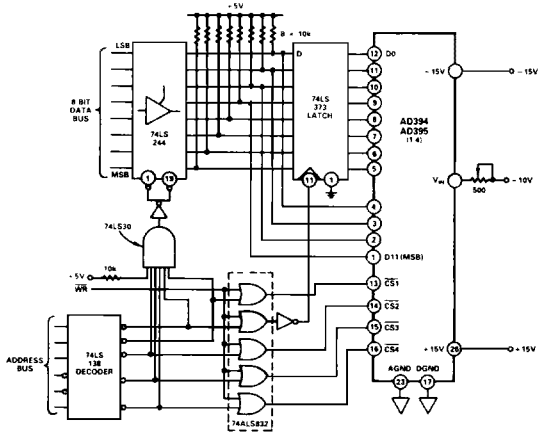


Figure 12. AD394, AD395 16-Bit Bus Interface

8-BIT PROCESSORS

The circuit of Figure 13 shows the general principles for connecting the AD394 or the AD395 to an 8-bit data bus. The 74LS244 buffers the data bus; its outputs are enabled when the DAC address appears on the address bus. The first byte sent to the DAC is loaded to the 74LS373 octal latch and, when the second byte is sent to the DAC, it is combined with the first byte to create a 12-bit word. The connections shown are for right-hand justified data. $\overline{CS}$ and $\overline{WR}$ inputs to the DAC are also gated, and when active, the DAC is loaded. Pull-up resistors at the output of the 74LS244 buffer ensure that the inputs to the DAC do not float at an ill-defined level when the DAC is not being addressed. This method of connecting 12-bit DACs to an 8-bit data bus is most cost effective when multiple DACs are utilized for 8-bit data bus applications.



NOTE:
UNUSED HEX INVERTER INPUTS SHOULD BE TIED LOW. ALL OTHER GATE INPUTS SHOWN SHOULD BE TIED HIGH TO +5V THROUGH A 10kΩ RESISTOR.

Figure 13. AD394, AD395 8-Bit Data Bus Interface

AD394/AD395 — Applications

The functional density of the AD394 and AD395 permits complex analog functions to be produced under digital control, where board space requirements would otherwise be prohibitive. Multiple-output plotters, multi-channel displays and complex waveform generation and multiple programmable voltage sources can all be implemented with the AD394 or AD395 in a fraction of the space which would be needed if separate DACs were used.

USING THE AD394 FOR ANALOG-TO-DIGITAL CONVERSION

Many systems require both analog output and analog input capability. While complete integrated circuit analog-to-digital converters (such as the AD574A) are readily available, the AD394 can be used as the precision analog section of an ADC if some external logic is available. Several types of analog-to-digital converters can be built with a DAC, comparator, and control logic, including staircase, tracking, and successive-approximation types. In systems which include a microprocessor, only a comparator must be added to the AD394 to accomplish the ADC function since the processor can perform the required digital operations under software control. A suitable circuit is shown in Figure 14. The AD311 comparator compares the unknown input voltage to one of the AD394 outputs for the analog-to-digital conversion, while the other three outputs are used as normal DACs. The diode clamp shown limits the voltage swing at the

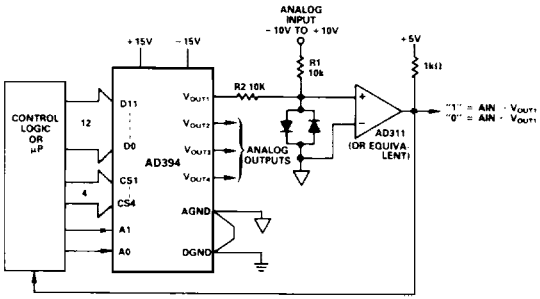


Figure 14. Using One AD394 Output for A D Conversion

comparator input and improves conversion speed. With careful layout, a new comparison can be performed in less than 15 microseconds, resulting in 12-bit successive approximation conversion in under 180 microseconds. The benefit of the AD394 in this application is that one ADC and three DACs can be implemented with only two IC packages (the AD394 and the comparator).

PROGRAMMABLE WINDOW COMPARATOR

The AD395 can be used to perform limit testing of responses to digitally-controlled input signals. For example, two DACs may be used to generate software-controlled test conditions for a component or circuit. The response to these input conditions can either be completely converted from analog to digital or simply tested against high and low limits generated by the two remaining DACs in the AD395.

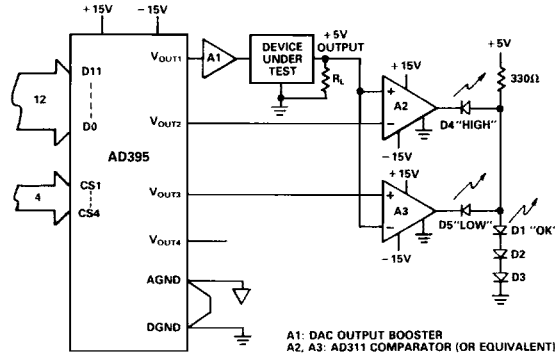


Figure 15. Programmable Window Comparator Used in Power-Supply Testing

In the circuit of Figure 15, two AD311 voltage comparators are used within AD395 to test the output of a 5 volt power-supply regulator. The AD395 V_{OUT1} output (through an appropriate current booster) drives the input to the regulator to simulate variations in input voltage. The output of the regulator is applied to comparators 1 and 2, with their outputs wire-ORed with LED indicators as shown. The test limits for each comparator are programmed by the AD395 V_{OUT2} and V_{OUT3} outputs. When the output of the device under test is within the limits, both comparators are off and D1 lights. If the output is above or below the limits, either D4 or D5 lights.

AD395 AS A MULTIPLIER AND ATTENUATOR

So far, it has been assumed that the reference voltage V_{REFIN} is fixed. In fact, V_{REFIN} can be any voltage within the range ($-11V < V_{REFIN} < +11V$). It can be negative, positive, sinusoidal or whatever the user prefers. This leads to the name "Multiplying D/A Converters" because the output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the V_{REFIN} terminal.

$$V_{OUT} = -1 \cdot (V_{REFIN}) \cdot \frac{D}{(4096)} \qquad (0<D<4095)$$

D is the fractional binary value of the digital word applied to the converter. The AD395 multiplies the digital input value by the analog input voltage at V_{REFIN} for any value of V_{REFIN} up to 22V p-p. This in itself is a powerful tool. Any applications requiring precision multiplication with minimal zero offset and very low distortion should consider the AD395 as a candidate. One popular use for AD395 is as a audio frequency attenuator. The audio signal is applied to the V_{REFIN} input and the attenuation code is applied to the DAC; the output voltage is the product of the two – an attenuated version of the input. The maximum attenuation range obtainable utilizing 12-bits is 4096:1 or 72db.

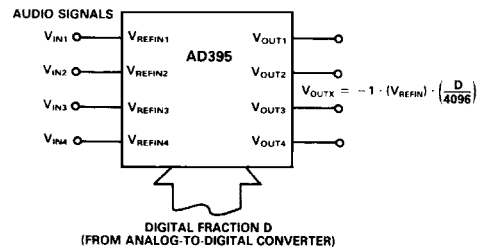


Figure 16. AD395 as a Multiplier or Attenuator