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MAX77541

5.5V_{IN}/6A, Dual-Phase High-Efficiency Buck Converter

General Description

The MAX77541 is a high-efficiency step-down converter with two 3A switching phases for single-cell Li+ battery and 5V_{DC} systems. It uses an adaptive COT (constant on-time) current-mode control architecture and the two 3A switching phases can be configured as either one (2Φ, 6A) or two (1Φ, 3A each) outputs. The output voltages are preset with resistors and are further adjustable through an I^2C compatible interface. With 91% peak efficiency, low quiescent current, and compact solution size, the MAX77541 is ideal for battery powered, space-constraint equipment.

Programmable switching frequency, frequency tracking, and spread-spectrum allow easier system optimization for noise-sensitive applications. Dedicated EN, POK, and FPWM pins provide options for direct hardware control, while more programmable options such as soft-start/stop and ramp-up/down slew-rates are available through I^2C. An array of built-in protections ensures safe operation under abnormal operating conditions.

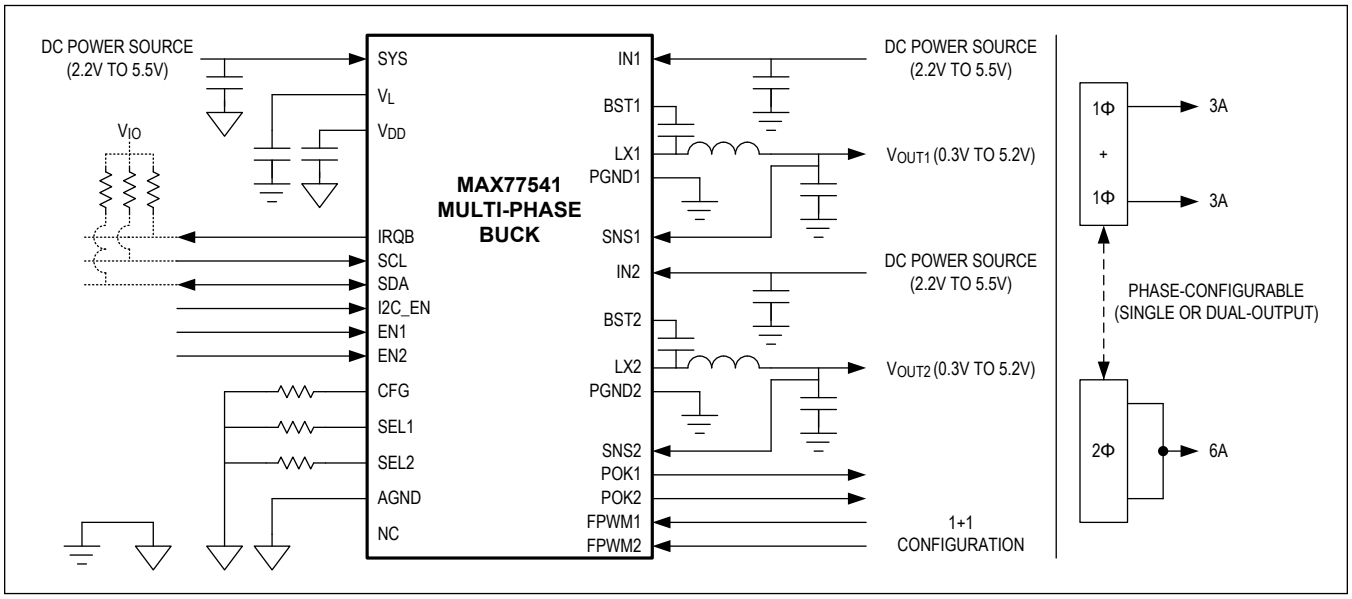
Applications

- Single-Cell Li+ and 5V_{DC} Systems
- Gaming Consoles and VR/AR Headsets
- Microprocessors, FPGAs, DSPs, and ASICs
- Network Switches and Routers

Benefits and Features

- 2.2V to 5.5V Input Voltage Range
- 0.3V to 5.2V Output Voltage Range
- Two 3A Bucks (1Φ) or One 6A Buck (2Φ)
- ±0.5% V_{OUT} Accuracy (Default V_{OUT} at 25°C)
- 91% Peak Efficiency (3.8V_{IN}, 1.1V_{OUT}, 1.6MHz)
- Auto SKIP/PWM Transition and Low-Power Mode
- Drop-Out Operation with 98% of Max. Duty Cycle
- Programmable Soft-Start/Soft-Stop and Ramp-up/Ramp-down Slew-rates
- Prebiased Startup and Active Output Discharge
- Programmable Inductor Peak Current Limits for Solution Size Optimization
- 0.5/1.0/1.6MHz Nominal Switching Frequency
- Spread-Spectrum Modulation for EMI Reduction
- Internal/External Frequency Tracking
- Default V_{OUT} and Phase Configuration Setting by R_{SEL1} and R_{SEL2}
- I^2C Slave ADDR, ILIM, and F_{SW} Preset by R_{CFG}
- Dedicated ENx, POKx and FPWMx for each Buck
- UVLO, Thermal Shutdown, and Short-circuit Protection
- High-Speed I^2C Serial I/F
- Available in 30-WLP (2.51mm x 2.31mm x 0.7mm) and 24-FC2QFN (3mm x 3mm) Packages
- Less than 55mm^2 Total Solution Size with 2520 Inductors

Typical Applications Circuit



***Ordering Information* appears at end of data sheet.**

19-101174; Rev 1; 5/22

TABLE OF CONTENTS

General Description . . . 1
Applications . . . 1
Benefits and Features . . . 1
Typical Applications Circuit . . . 1
Absolute Maximum Ratings . . . 6
Recommended Operating Conditions . . . 6
Package Information . . . 6
30 WLP . . . 6
24 FC2QFN . . . 7
Electrical Characteristics—Top-Level . . . 9
Electrical Characteristics—Dual-Phase Configurable Buck Converter . . . 10
Electrical Characteristics—ADC . . . 13
Electrical Characteristics—I^2C Serial Interface . . . 14
Typical Operating Characteristics . . . 16
Bump Configuration . . . 22
30 WLP . . . 22
24 FC2QFN . . . 23
Bump Descriptions . . . 23
Detailed Description—Top-Level . . . 26
Dedicated Internal Supplies . . . 26
Device Configuration (CFG) . . . 26
Output Enable Control . . . 27
Undervoltage Lock-Out (UVLO) . . . 27
Thermal Warnings and Thermal Shutdown (T_{SHDN}) . . . 27
Interrupt (IRQB) and Mask . . . 28
Register Reset Condition . . . 29
FC2QFN Default Options . . . 29
Detailed Description—Dual-Phase Configurable Buck Converter . . . 29
Buck Converter Control Scheme . . . 29
Buck Operating Modes . . . 30
SKIP Mode . . . 31
Low-Power SKIP (LP-SKIP) Mode . . . 31
Forced-PWM (FPWM) Mode . . . 32
Dropout Mode . . . 32
Switching Frequency . . . 32
Phase Configuration . . . 33
Default Output Voltage Selection (SELx) . . . 33
Output Voltage Setting . . . 35
Soft-Start and Soft-Stop . . . 35

TABLE OF CONTENTS (CONTINUED)

Dynamic Output Voltage Scaling . . . 36
Output Voltage Active Discharge . . . 36
Bootstrap Refresh . . . 37
Frequency Tracking (FTRAK) . . . 37
Spread-Spectrum Modulation . . . 38
Pseudo-Random Pattern . . . 38
Triangular Pattern . . . 39
Inductor Current Limits . . . 40
Power-OK (POK) . . . 40
Fault Protection . . . 41
Detailed Description—ADC . . . 43
ADC Enable and Measurement Options . . . 43
SYS Voltage Measurement . . . 43
Output Voltage Measurement . . . 43
Junction Temperature Measurement . . . 43
Detailed Description—I^2C Serial Interface . . . 44
Slave Address . . . 44
Register Map . . . 45
MAX77541 WLP Package . . . 45
Register Details . . . 46
Applications Information—Dual-Phase Configurable Buck Converter . . . 61
Inductor Selection . . . 61
Input Capacitor Selection . . . 61
Output Capacitor Selection . . . 61
General PCB Layout Guidelines . . . 62
Typical Application Circuits . . . 65
1+1 Phase Configuration—WLP . . . 65
Dual-Phase Configuration—WLP . . . 66
1+1 Phase Configuration—FC2QFN . . . 67
Dual-Phase Configuration—FC2QFN . . . 68
Ordering Information . . . 68
Revision History . . . 69

LIST OF FIGURES

Figure 1. Thermal Warnings and Thermal Shutdown 28
Figure 2. Functional Block Diagram 30
Figure 3. Buck Operating Modes 31
Figure 4. Frequency Tracking 37
Figure 5. Pseudo-Random Modulator Engine 38
Figure 6. 4-Bit Pseudo-Random Modulation Signal Example 39
Figure 7. Triangular Modulator Engine 39
Figure 8. 4-Bit Triangular Modulation Signal Example 40
Figure 9. Fault Protection State Diagram 42
Figure 10. ADC Block Diagram 43
Figure 11. PCB Layout Example—WLP 63
Figure 12. PCB Layout Example—FC2QFN 64

LIST OF TABLES

Table 1. V_{DD} and I^2C Enable Truth Table 26
Table 2. Device Configuration 26
Table 3. Phase Configuration Selection 33
Table 4. Buck Output Voltage Sensing Assignment 33
Table 5. Default V_{OUT1} Selection 33
Table 6. Default V_{OUT2} Selection 34
Table 7. Buck Output Voltage Range 35
Table 8. Mx_FSREN Effect On Buck Behavior 36
Table 9. Bootstrap Refresh Interval Selection 37
Table 10. Mx_FTRAK Enable Truth Table 37
Table 11. Recommended Inductors 61
Table 12. Recommended Minimum Effective Output Capacitance 61

Absolute Maximum Ratings

SYS to AGND ..... -0.3V to +6.0V
V_{DD} to AGND ..... -0.3V to +2.2V
V_L to PGND ..... -0.3V to +2.2V
I2C_EN, EN1, EN2 to AGND ..... -0.3V to +6.0V
IN1 to PGND1 ..... -0.3V to +6.0V
IN2 to PGND2 ..... -0.3V to +6.0V
LX1 to PGND1 ..... -0.3V to +6.0V
LX1 to PGND1 (less than 10ns) ..... (V_{IN} - 11.94)V to +11.94V
LX2 to PGND2 ..... -0.3V to +6.0V
LX2 to PGND2 (less than 10ns) ..... (V_{IN} - 11.94)V to +11.94V
BST1 to LX1 ..... -0.3V to +2.2V
BST2 to LX2 ..... -0.3V to +2.2V
SNS1, SNS2 to AGND ..... -0.3V to +6.0V
FPWM1, FPWM2 to AGND ..... -0.3V to +6.0V
POK1, POK2 to AGND ..... -0.3V to +6.0V
SCL, SDA, IRQB to AGND ..... -0.3V to +6.0V
CFG, SEL1, SEL2 to AGND ..... -0.3V to MIN(V_{DD} + 0.3, +2.2)V
PGND1, PGND2 to AGND ..... -0.3V to +0.3V
Continuous Power Dissipation (JESD51-7, T_A = +70ºC)
30 WLP (Derate 20.25mW/°C above +70°C) 1620mW
24 FC2QFN (Derate 27.29mW/°C above +70°C) 2183mW
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LXx has internal clamp diodes to its corresponding PGNDx and INx. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

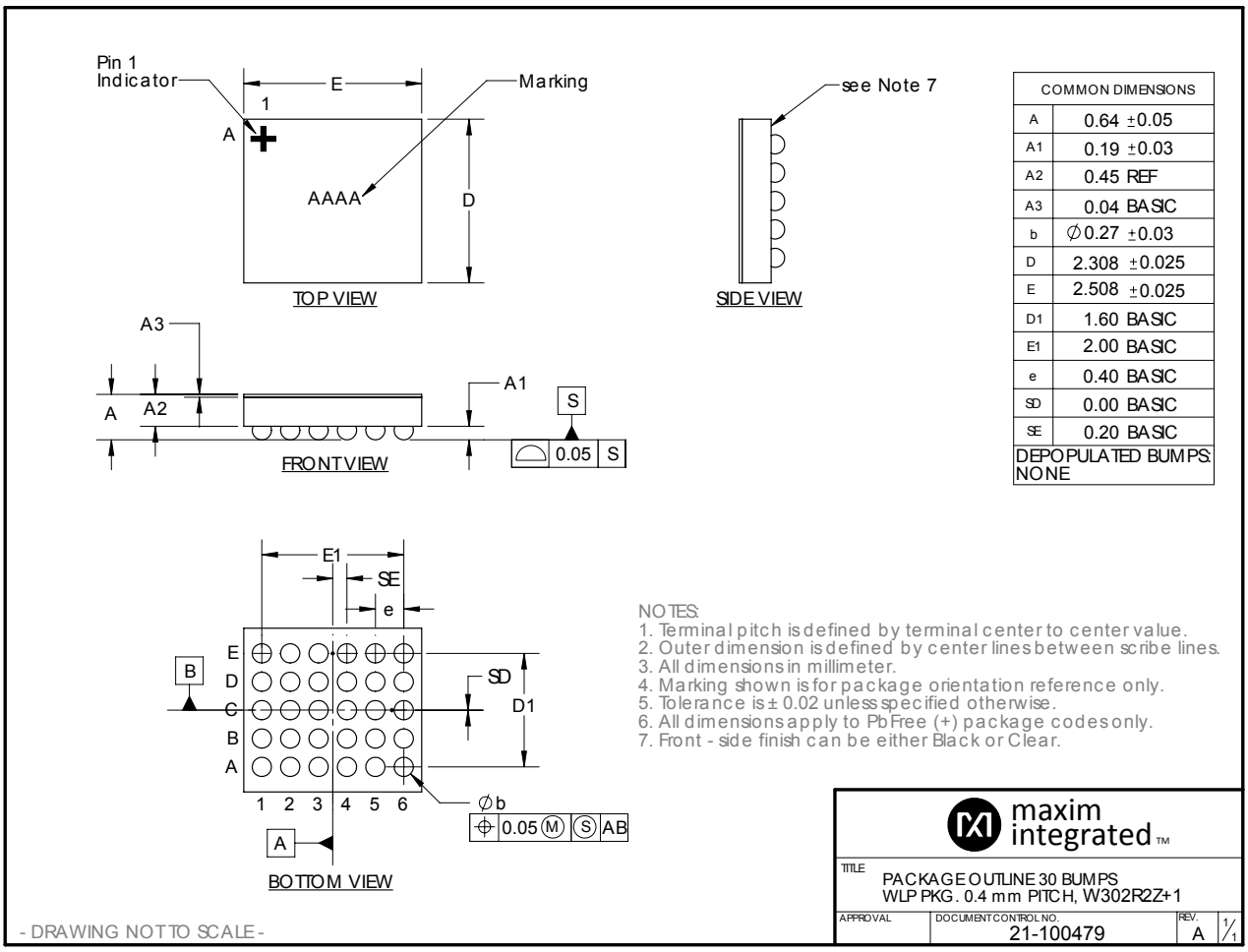
PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Input Voltage Range	V_{IN}		2.2 to 5.5	V
Output Current Range	I_{OUT}	For continuous operation at 3A, the junction temperature (T_J) is limited to +105ºC; if the junction temperature is higher than +105ºC, the expected lifetime at 3A continuous operation is derated	0 to 3	A
Junction Temperature Range	T_J		-40 to +125	ºC

Note: These limits are not guaranteed.

Package Information

30 WLP

Package Code	W302R2Z+1
Outline Number	21-100479
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49.38°C/W



COMMON DIMENSIONS	
A	0.64 ±0.05
A1	0.19 ±0.03
A2	0.45 REF
A3	0.04 BASIC
b	Ø0.27 ±0.03
D	2.308 ±0.025
E	2.508 ±0.025
D1	1.60 BASIC
E1	2.00 BASIC
e	0.40 BASIC
SD	0.00 BASIC
SE	0.20 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

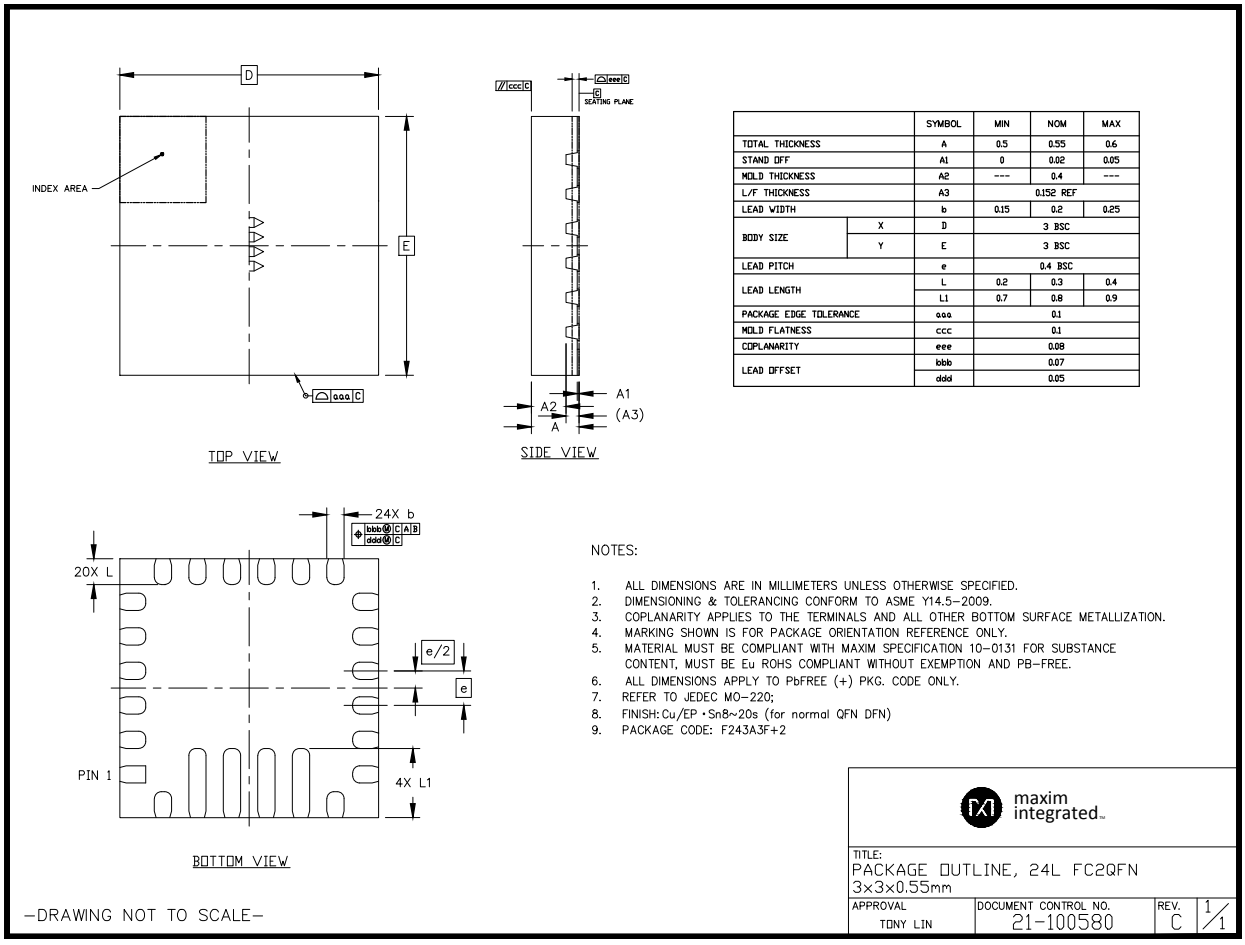
maxim integrated™

TITLE: PACKAGE OUTLINE 30 BUMPS WLP PKG. 0.4 mm PITCH, W302R2Z+1

APPROVAL | DOCUMENT CONTROL NO. 21-100479 | REV. A | 1/1

24 FC2QFN

Package Code	F243A3F+2
Outline Number	21-100580
Land Pattern Number	90-100211
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	36.64°C/W



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.4 BSC	
LEAD LENGTH		L	0.2	0.3	0.4
		L1	0.7	0.8	0.9
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5–2009.
3. COPLANARITY APPLIES TO THE TERMINALS AND ALL OTHER BOTTOM SURFACE METALLIZATION.
4. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
5. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10–0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB–FREE.
6. ALL DIMENSIONS APPLY TO PbFREE (+) PKG. CODE ONLY.
7. REFER TO JEDEC MO–220;
8. FINISH: Cu/EP • Sn8~20s (for normal QFN DFN)
9. PACKAGE CODE: F243A3F+2

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TITLE:
PACKAGE OUTLINE, 24L FC2QFN
3x3x0.55mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
TONY LIN	21-100580	C	1/1

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics—Top-Level

(V_{SYS} = V_{IN1} = V_{IN2} = 3.8V, V_{OUT1} = 0.65V, V_{OUT2} = 1.1V, Single-phase Configuration (1Φ + 1Φ), V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT VOLTAGE AND SUPPLY CURRENT							
SYS Voltage Range	V_{SYS}			2.2		5.5	V
SYS Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{SYS} rising		2.1	2.2	2.3	V
	V_{UVLO_F}	V_{SYS} falling		1.9	2.0	2.1	
Power-On Reset (POR) Threshold (Note 7)	V_{POR}	V_{SYS} falling			1.7		V
Shutdown Supply Current (Note 3)	I_{SHDN}	V_{I2C_EN} = V_{ENx} = 0V	T_J = -40°C to +85°C		1.5	7.5	µA
			T_J = +125°C			35	
Standby Supply Current (Note 3, Note 8)	I_{STBY}	EN_FTMON = 0, all Bucks are disabled	T_J = -40°C to +85°C		25	50	µA
			T_J = +125°C			105	
Quiescent Supply Current in LP-SKIP Mode (Note 3, Note 8)	$I_{Q\_LP-SKIP}$	V_{OUT} > $V_{OUT(TARGET)}$, no load	Only one Buck phase is enabled		215	300	µA
			Both Buck phases are enabled		325	400	
Quiescent Supply Current in SKIP Mode (Note 3)	I_{Q_SKIP}	V_{OUT} > $V_{OUT(TARGET)}$, No Load	Only one Buck phase is enabled		250	330	µA
			Both Buck phases are enabled		390	500	
INTERNAL BIAS SUPPLY							
V_L Regulator Voltage	V_L	(Note 4)			1.8		V
V_{DD} Regulator Voltage	V_{DD}	(Note 4)			1.8		V
V_{DD} Undervoltage Lock out (UVLO)	$V_{DD\_UVLO\_F}$	(Note 4)			1.55		V
THERMAL PROTECTION							
Thermal Warning 1 (Note 8)	T_{J120}	T_J Rising, 15°C hysteresis			+120		°C
Thermal Warning 2 (Note 8)	T_{J140}	T_J Rising, 15°C hysteresis			+140		°C
Thermal Shutdown (T_{SHDN})	T_{SHDN}	T_J Rising, 15°C hysteresis (Note 8)			+165		°C
LOGIC INPUT AND OUTPUT							
FPWMx Input Logic High Threshold	V_{IH_FPWM}			1.44			V
FPWMx Input Logic Low Threshold	V_{IL_FPWM}					0.54	V
I2C_EN, ENx Input Logic High Threshold	V_{IH_EN}			1.1			V
I2C_EN, ENx Input Logic Low Threshold	V_{IL_EN}					0.4	V
IRQB Output Logic Low Threshold (Note 8)	V_{OL_IRQB}	Sinking 2mA				0.4	V

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 3.8V, V_{OUT1} = 0.65V, V_{OUT2} = 1.1V, Single-phase Configuration (1Φ + 1Φ), V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POKx Output Logic Low Threshold	V_{OL_POK}	Sinking 2mA				0.4	V
I2C_EN, ENx Leakage Current	I_{LKG_EN}	V_{SYS} = 5.5V, V_{ENx} = 0V and 5.5V	T_J = +25°C		±0.1		µA
			T_J = +85°C		±0.5		
IRQB Leakage Current (Note 8)	I_{LKG_IRQB}	IRQB set to Hi-Z (i.e., no interrupt pending), V_{IRQB} = 0V and 5.5V		-1		+1	µA
POKx Leakage Current	I_{LKG_POK}	POKx = High (Hi-Z), V_{POKx} = 5.5V, T_J = +85ºC				1	µA

Note 2: The MAX77541 is tested under pulsed load conditions such that $T_J \approx T_A$. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_J = -40°C to +125°C) are guaranteed by design and characterization using statistical process control methods. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

Note 3: Supply Current = I_{SYS} + I_{IN1} + I_{IN2}

Note 4: See the *Dedicated Internal Supplies* section.

Electrical Characteristics—Dual-Phase Configurable Buck Converter

(V_{SYS} = V_{IN1} = V_{IN2} = 3.8V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 0.65V, V_{OUT2} = 1.1V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY							
Input Voltage Range	V_{INx}			2.2		5.5	V
DC OUTPUT VOLTAGE AND ACCURACY							
Output Voltage Range	V_{OUT_RNG}	Low-range (Mx_RNG[1:0] = 0x0)		0.3		1.2	V
		Mid-range (Mx_RNG[1:0] = 0x1)		1		2.4	
		High-range (Mx_RNG[1:0] = 0x2)		2		5.2	
Line Regulation		1Φ, FPWM mode, V_{INx} = 2.2V to 5.5V, V_{OUT} = default, I_{OUT} = 0A		-0.1		+0.1	%/V
Load Regulation		1Φ, FPWM mode, I_{OUT} = 0A to 3A (Note 7)			0.1		%/A
DC Output Voltage Accuracy	V_{OUT_ACC}	1Φ, FPWM mode, V_{INx} = 2.2V to 5.5V, I_{OUT} = 0A	V_{OUT} < 0.5V	-2.5		+2.5	%
			0.5V ≤ V_{OUT} ≤ 1.0V	-1.5		+1.5	
			1.0V < V_{OUT} ≤ 5.2V	-2.0		+2.0	
			V_{OUT} = factory default, T_J = +25°C	-0.5		+0.5	
POWER STAGE							
High-Side MOSFET Peak Current Limit	I_{PLIM}	Mx_ILIM[1:0] = 0x0		1.6	2.2	2.8	A
		Mx_ILIM[1:0] = 0x1		2.8	3.4	4.0	
		Mx_ILIM[1:0] = 0x2		3.4	4.0	4.6	
		Mx_ILIM[1:0] = 0x3		4.0	4.6	5.2	

Electrical Characteristics—Dual-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 3.8V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 0.65V, V_{OUT2} = 1.1V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Side MOSFET Valley Current Limit	I_{VLIM}	Tracks I_{PLIM}			I_{PLIM} - 1		A
Low-Side MOSFET Negative Current Limit	I_{NLIM}	FPWM mode		-3.9	-3.0	-2.4	A
Low-Side MOSFET Zero-Crossing Current Threshold	I_{ZX}	SKIP or LP-SKIP mode			150		mA
High-Side MOSFET On-Resistance	R_{ON_HS}	1Φ, I_{LXx} = 190mA			16	32	mΩ
Low-Side MOSFET On-Resistance	R_{ON_LS}	1Φ, I_{LXx} = -190mA			10	20	mΩ
Nominal Switching Frequency	F_{SW}	FPWM mode, no load, no external clock, T_J = +25°C (Note 5)	Mx_FREQ[1:0] = 0x0		0.5		MHz
			Mx_FREQ[1:0] = 0x1		1		
			Mx_FREQ[1:0] = 0x2		1.6		
Maximum Duty Cycle	D_{MAX}	Drop-out region (V_{OUT} falls below its regulation target)		97	98		%
Output Active Discharge Resistance	R_{AD7}	1Φ, Buck output disabled, active discharge enabled (Mx_ADIS7 = 1), resistance from corresponding SNS_X to PGNDx (Note 8)			7		Ω
	R_{AD100}	1Φ, Buck output disabled, active discharge enabled (Mx_ADIS100 = 1), resistance from corresponding LX_X to PGNDx			100		
LX Leakage Current	I_{LKG_LX}	1Φ, V_{LXx} = 0V and 5.5V	T_J = +25°C		0.1	1	µA
			T_J = -40°C to +85°C		1		
SLEW-RATE AND TIMING							
Soft-Start Slew-Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	SSTRT_SR[2:0] = 0x0			0.15		mV/µs
		SSTRT_SR[2:0] = 0x1			0.625		
		SSTRT_SR[2:0] = 0x2			1.25		
		SSTRT_SR[2:0] = 0x3			2.5		
		SSTRT_SR[2:0] = 0x4			5		
		SSTRT_SR[2:0] = 0x5			10		
		SSTRT_SR[2:0] = 0x6			20		
		SSTRT_SR[2:0] = 0x7			40		

Electrical Characteristics—Dual-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 3.8V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 0.65V, V_{OUT2} = 1.1V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Stop Slew-Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	SSTOP_SR[2:0] = 0x0			-0.15		mV/µs
		SSTOP_SR[2:0] = 0x1			-0.625		
		SSTOP_SR[2:0] = 0x2			-1.25		
		SSTOP_SR[2:0] = 0x3			-2.5		
		SSTOP_SR[2:0] = 0x4			-5		
		SSTOP_SR[2:0] = 0x5			-10		
		SSTOP_SR[2:0] = 0x6			-20		
		SSTOP_SR[2:0] = 0x7			-40		
Ramp-Up Slew-Rate (Note 6, Note 8)	$\Delta V_{OUT}/\Delta t$	Mx_RU_SR[2:0] = 0x0			0.15		mV/µs
		Mx_RU_SR[2:0] = 0x1			0.625		
		Mx_RU_SR[2:0] = 0x2			1.25		
		Mx_RU_SR[2:0] = 0x3			2.5		
		Mx_RU_SR[2:0] = 0x4			5		
		Mx_RU_SR[2:0] = 0x5			10		
		Mx_RU_SR[2:0] = 0x6			20		
		Mx_RU_SR[2:0] = 0x7			40		
Ramp-Down Slew-Rate (Note 6, Note 8)	$\Delta V_{OUT}/\Delta t$	Mx_RD_SR[2:0] = 0x0			-0.15		mV/µs
		Mx_RD_SR[2:0] = 0x1			-0.625		
		Mx_RD_SR[2:0] = 0x2			-1.25		
		Mx_RD_SR[2:0] = 0x3			-2.5		
		Mx_RD_SR[2:0] = 0x4			-5		
		Mx_RD_SR[2:0] = 0x5			-10		
		Mx_RD_SR[2:0] = 0x6			-20		
		Mx_RD_SR[2:0] = 0x7			-40		
Slew-Rate Accuracy		REFDAC Slew-rate accuracy		-5		+5	%
Turn-On Delay	t_{DLY}	Delay from rising edge of ENx signal to V_{OUTx} ramping start-off	V_{DD} is pre-enabled		90	140	µs
Turn-on Delay	t_{DLY}	Delay from rising edge of ENx signal to V_{OUTx} ramping start-off	V_{DD} is not pre-enabled		530	640	µs
FREQUENCY TRACKING							
External Frequency Tracking Lockable Range (Note 6)	F_{FTRAK}	Expressed as a percentage of the nominal frequency set by Mx_FREQ[1:0]		95		105	%

Electrical Characteristics—Dual-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 3.8V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 0.65V, V_{OUT2} = 1.1V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPREAD-SPECTRUM (Note 8)						
Modulation Frequency (Note 6)	F_{SS_MOD}	Mx_SS_FREQ[1:0] = 0x0		1		kHz
		Mx_SS_FREQ[1:0] = 0x1		3		
		Mx_SS_FREQ[1:0] = 0x2		5		
		Mx_SS_FREQ[1:0] = 0x3		7		
Modulation Envelope	ΔF_{SS}	Mx_SS_ENV[1:0] = 0x1		±8		%
		Mx_SS_ENV[1:0] = 0x2		±12		
		Mx_SS_ENV[1:0] = 0x3		±16		
POWER-OK AND SHORT-CIRCUIT PROTECTION						
Power-OK Rising Threshold	V_{POK_R}	Expressed as a percentage of V_{OUT}	77	82	87	%
Power-OK Falling Threshold	V_{POK_F}	Expressed as a percentage of V_{OUT}	73	78	83	%
Power-OK Fault Time-out (Note 6)	t_{POK_TO}	POK_TO[1:0] = 0x1		1		ms
		POK_TO[1:0] = 0x2		5		
		POK_TO[1:0] = 0x3		10		
Short-Circuit Detection Threshold	V_{SCP}	V_{OUT} falling, expressed as a percentage of target V_{OUT}		20		%

Note 5: Switching frequency is not set by a clock oscillator. F_{SW} varies depending on input voltage, output voltage, load, and spread-spectrum settings.

Note 6: Guaranteed by design. Production tested through scan.

Note 7: Not production tested. Design guidance only.

Note 8: Not applicable to FC2QFN package.

Electrical Characteristics—ADC

(V_{SYS} = 3.8V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
READBACK ACCURACY (NOTE 7)							
SYS Input Voltage Readback Accuracy	V_{SYS_ADC}	3.0V ≤ V_{SYS} ≤ 5.5V	T_J = -40°C to +85°C		3		%
			T_J = +125°C		5		
Output Voltage Readback Accuracy	V_{OUT_ADC}	T_J = -40°C to +85°C			3		%
		T_J = +125°C			5		
Junction Temperature Readback Accuracy	T_{J_ADC}	T_J = +85°C to +125°C			5		%
TIMING (NOTE 6)							
Clock Frequency	f_{ADC}				1		MHz
ADC Startup Time	t_{ADC_SU}	One of Buck outputs is enabled			11		µs
		All Buck outputs are disabled			13		

Electrical Characteristics—ADC (continued)

(V_{SYS} = 3.8V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC Sampling Time	t_{SAMPLE}	Per channel	V_{SYS}, V_{OUTx}		9		µs
			T_J		1		ms
Conversion Time	t_{CONV}	Per channel			9		µs
Sampling Interval for Averaging Mode	t_{INT_AVG}	Sampling interval for the same channel in averaging mode			5		ms
Sampling Interval for Continuous Measurement	t_{INT_CONT}	Sampling interval for the same channel during continuous measurement operation			1		s

Electrical Characteristics—I^2C Serial Interface

(V_{SYS} = 3.8V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE (Note 8)						
SCL, SDA Input Logic Low Threshold	V_{IL}				0.54	V
SCL, SDA Input Logic High Threshold	V_{IH}		1.44			V
SCL, SDA Input Hysteresis	V_{HYS}			0.3		V
SDA Output Logic Low Threshold	V_{OL_SDA}	Sinking 20mA			0.4	V
SCL, SDA Input Leakage Current	I_{LKG}	V_{SCL} = V_{SDA} = 0V or 5.5V	-10		+10	µA
SCL, SDA Pin Capacitance		(Note 7)		10		pF
STANDARD, FAST, AND FAST MODE PLUS TIMING (Note 8)						
Clock Frequency	f_{SCL}				1	MHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		260			ns
SCL LOW Period	t_{LOW}		500			ns
SCL HIGH Period	t_{HIGH}		260			ns
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Data Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 7)		50		ns

Electrical Characteristics—I²C Serial Interface (continued)

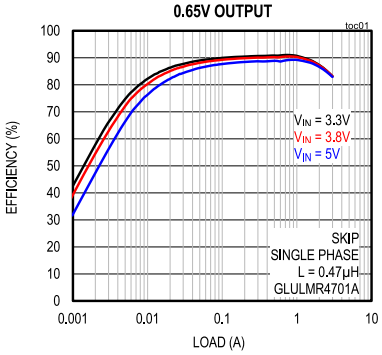
(V_{SYS} = 3.8V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted, limits are 100% production tested at T_A = +25°C. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SPEED MODE TIMING (Note 8)						
Clock Frequency	f_{SCL}	High-speed mode			3.4	MHz
Setup Time REPEATED START Condition	$t_{SU;STA}$		160			ns
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Data Setup Time	$t_{SU;DAT}$		10			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 7)		10		ns

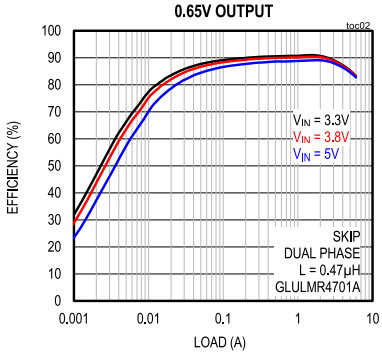
Typical Operating Characteristics

(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

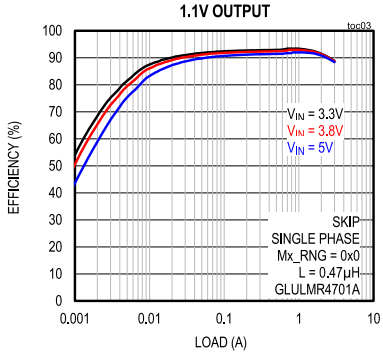
EFFICIENCY vs. LOAD
0.65V OUTPUT



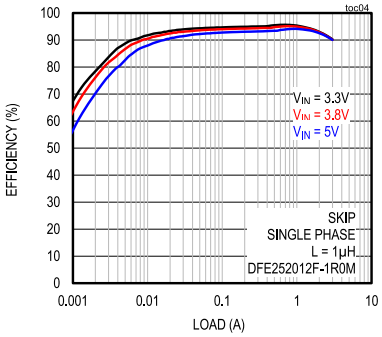
EFFICIENCY vs. LOAD
0.65V OUTPUT



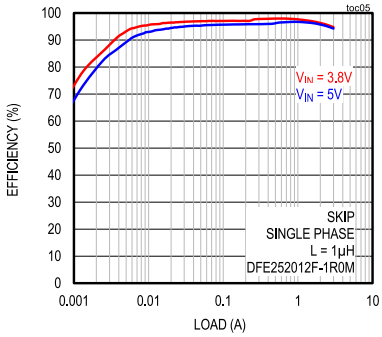
EFFICIENCY vs. LOAD
1.1V OUTPUT



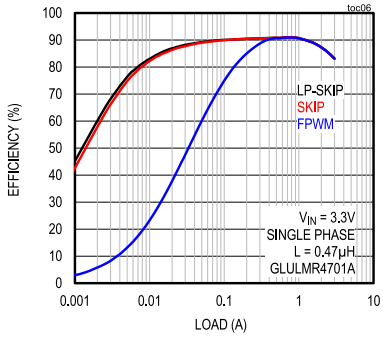
EFFICIENCY vs. LOAD
1.8V OUTPUT



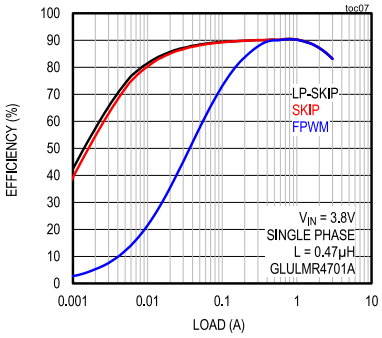
EFFICIENCY vs. LOAD
3.3V OUTPUT



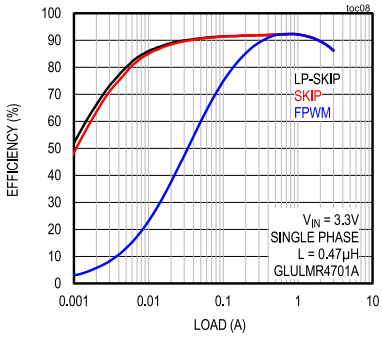
EFFICIENCY vs. LOAD
0.65V OUTPUT



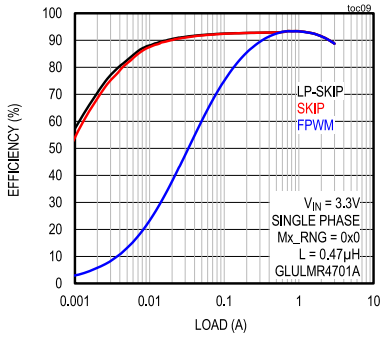
EFFICIENCY vs. LOAD
0.65V OUTPUT



EFFICIENCY vs. LOAD
0.85V OUTPUT



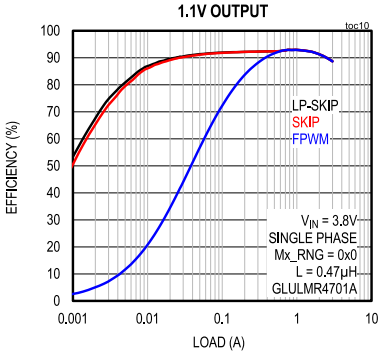
EFFICIENCY vs. LOAD
1.1V OUTPUT



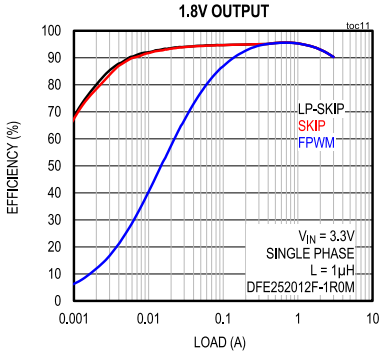
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

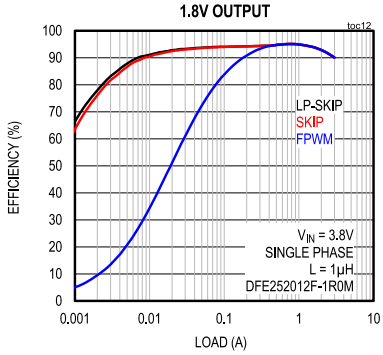
EFFICIENCY vs. LOAD
1.1V OUTPUT



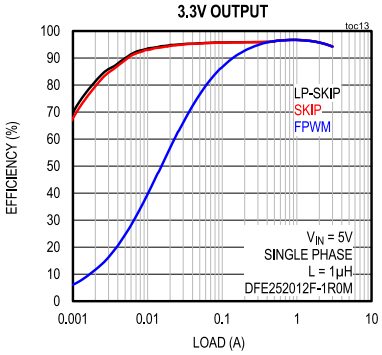
EFFICIENCY vs. LOAD
1.8V OUTPUT



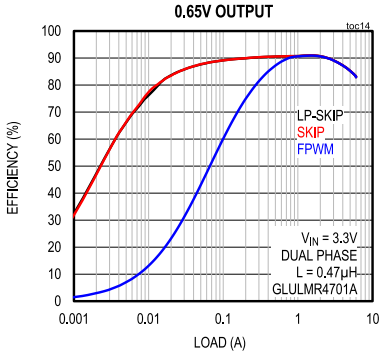
EFFICIENCY vs. LOAD
1.8V OUTPUT



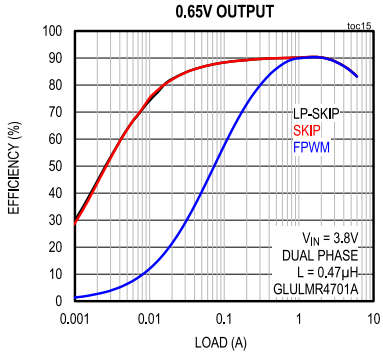
EFFICIENCY vs. LOAD
3.3V OUTPUT



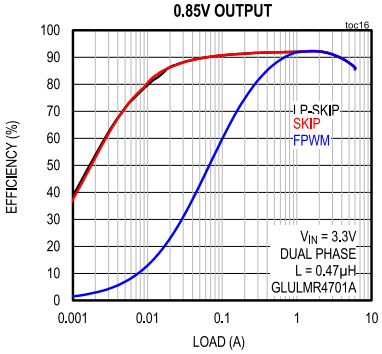
EFFICIENCY vs. LOAD
0.65V OUTPUT



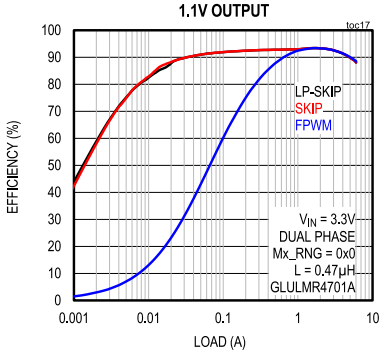
EFFICIENCY vs. LOAD
0.65V OUTPUT



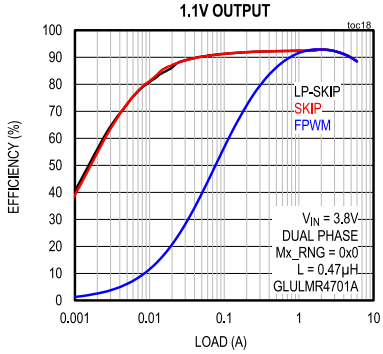
EFFICIENCY vs. LOAD
0.85V OUTPUT



EFFICIENCY vs. LOAD
1.1V OUTPUT



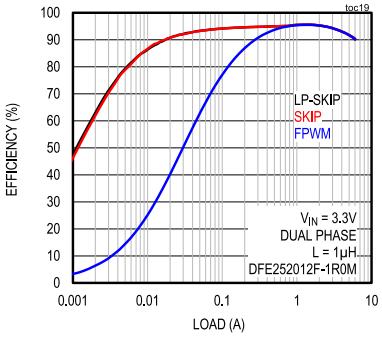
EFFICIENCY vs. LOAD
1.1V OUTPUT



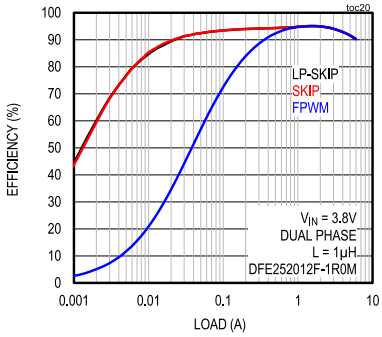
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

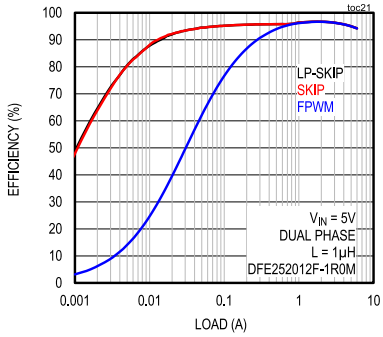
EFFICIENCY vs. LOAD
1.8V OUTPUT



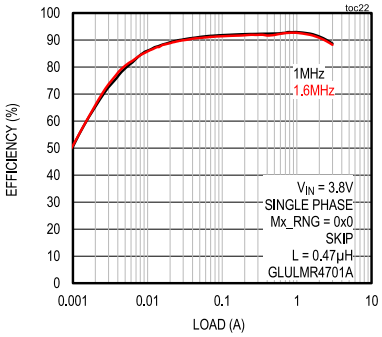
EFFICIENCY vs. LOAD
1.8V OUTPUT



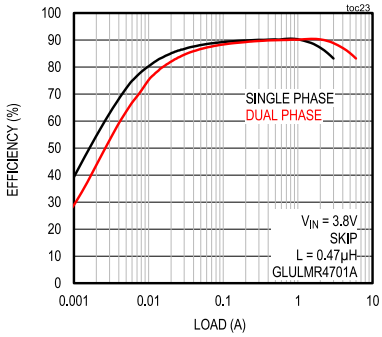
EFFICIENCY vs. LOAD
3.3V OUTPUT



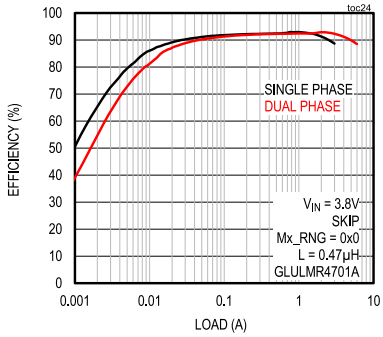
EFFICIENCY vs. LOAD
1.1V OUTPUT



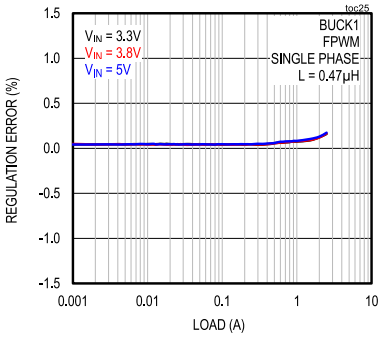
EFFICIENCY vs. LOAD
0.65V OUTPUT



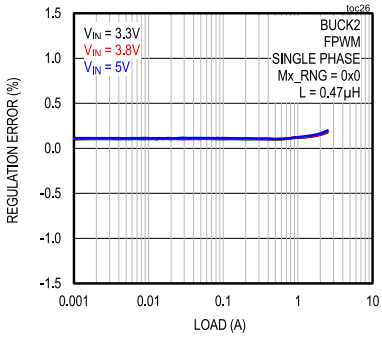
EFFICIENCY vs. LOAD
1.1V OUTPUT



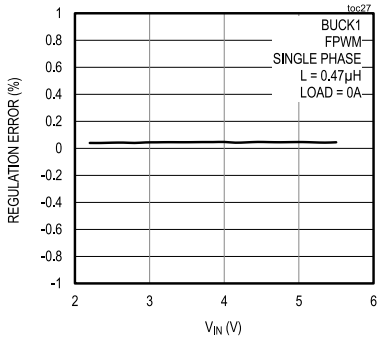
LOAD REGULATION
0.65V OUTPUT



LOAD REGULATION
1.1V OUTPUT

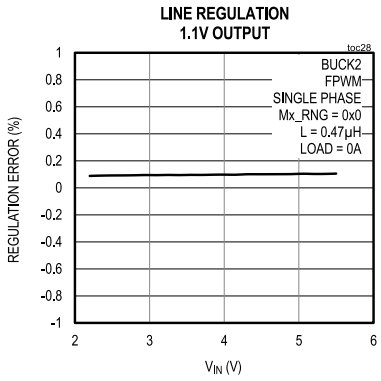


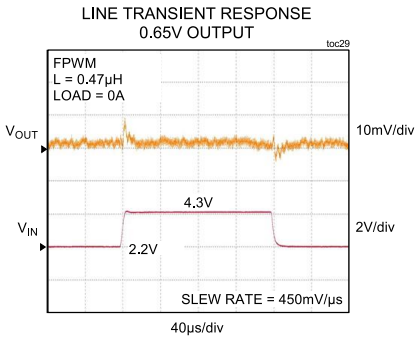
LINE REGULATION
0.65V OUTPUT

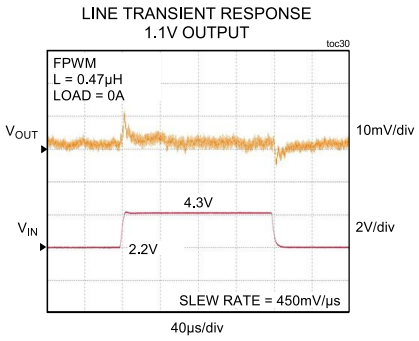


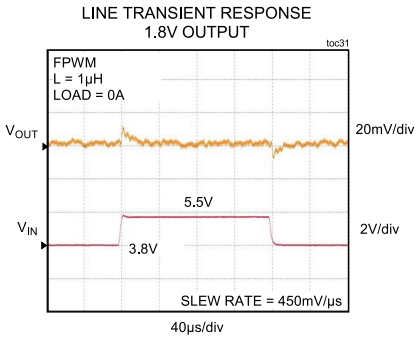
Typical Operating Characteristics (continued)

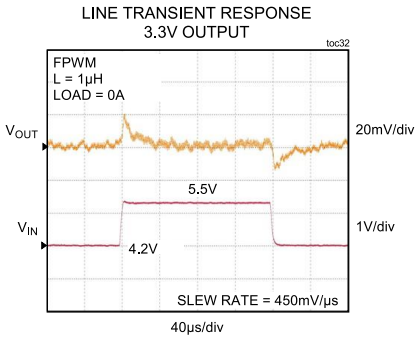
(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

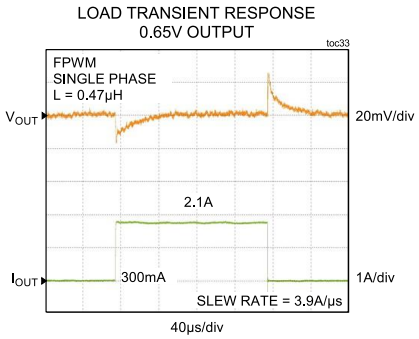


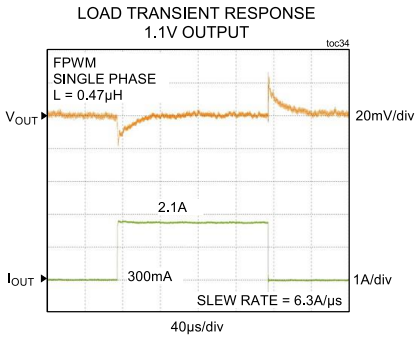


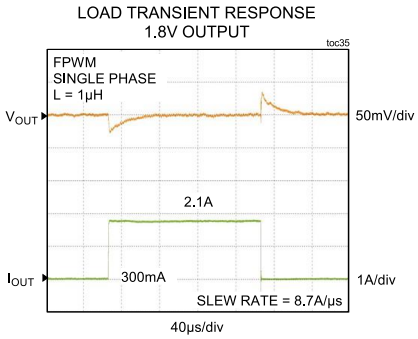


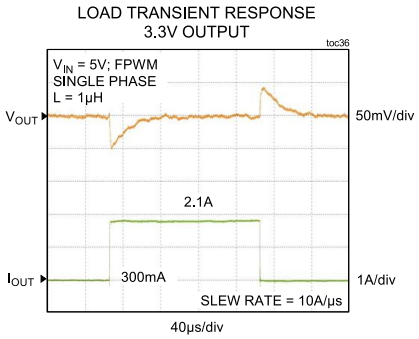








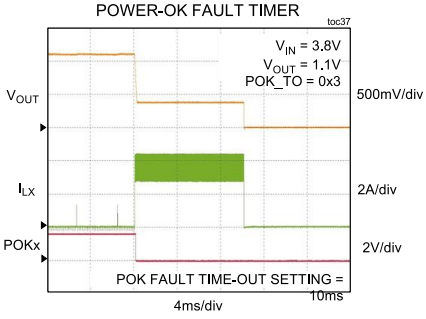




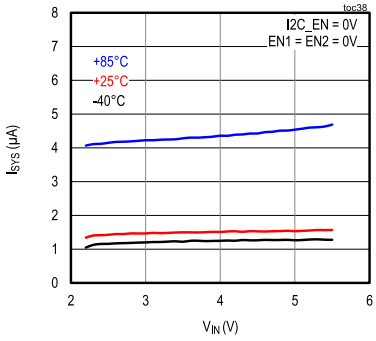
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

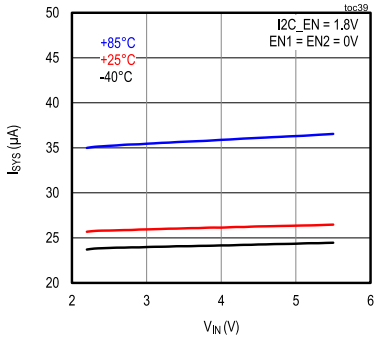
POWER-OK FAULT TIMER



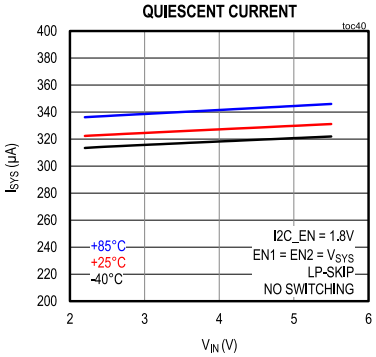
SHUTDOWN CURRENT



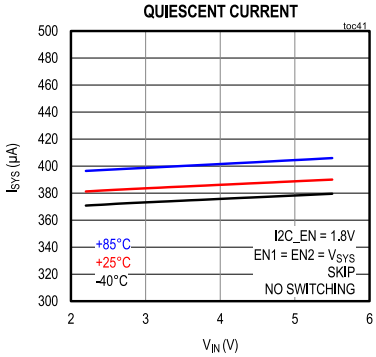
STANDBY CURRENT



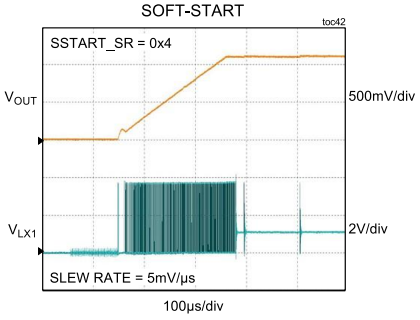
QUIESCENT CURRENT



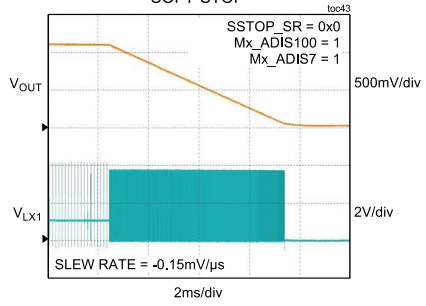
QUIESCENT CURRENT



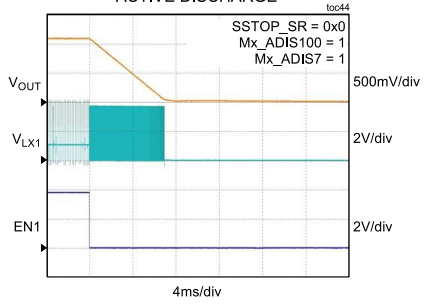
SOFT-START



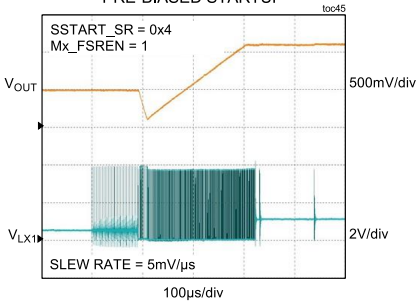
SOFT-STOP



ACTIVE DISCHARGE



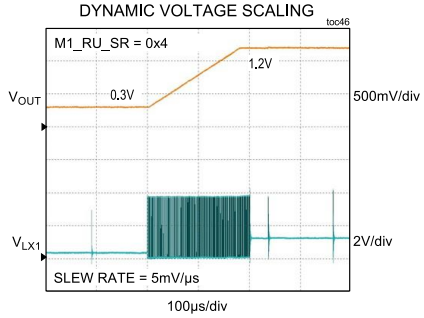
PRE-BIASED STARTUP



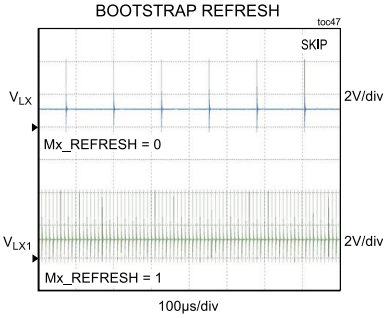
Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

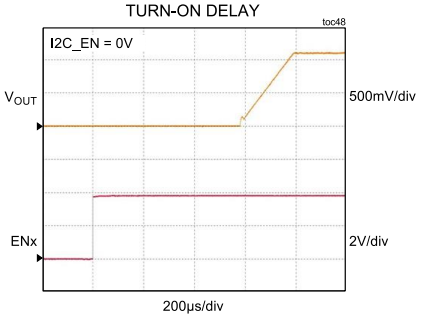
DYNAMIC VOLTAGE SCALING



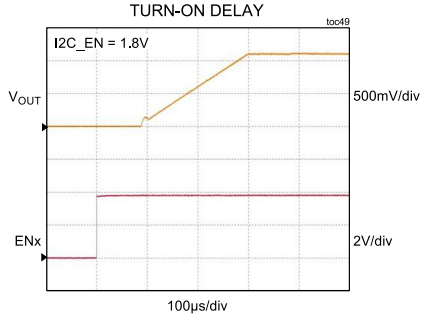
BOOTSTRAP REFRESH



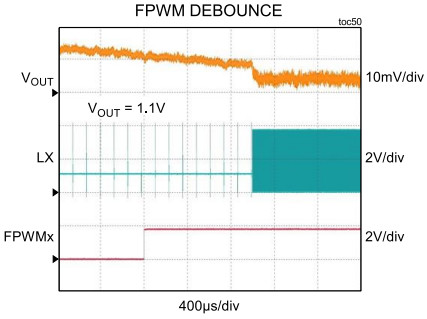
TURN-ON DELAY



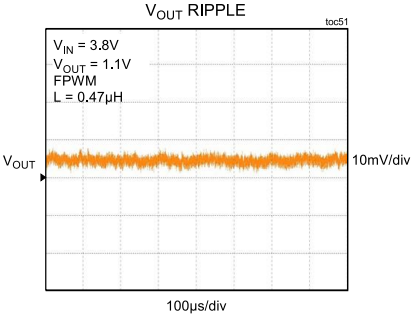
TURN-ON DELAY



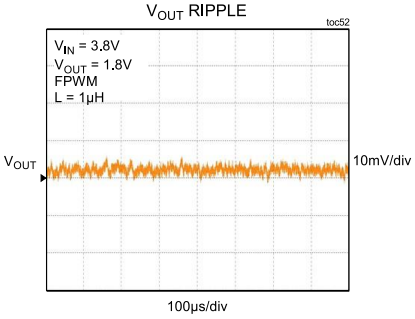
FPWM DEBOUNCE



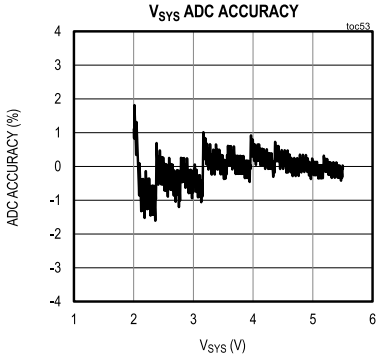
VOUT RIPPLE



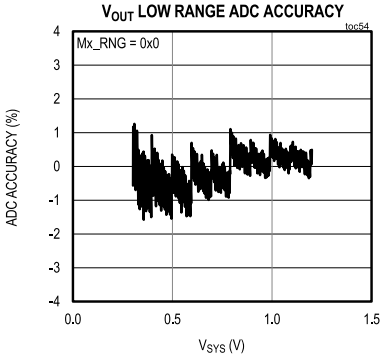
VOUT RIPPLE



VSYS ADC ACCURACY

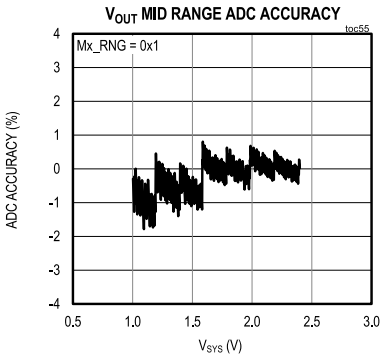


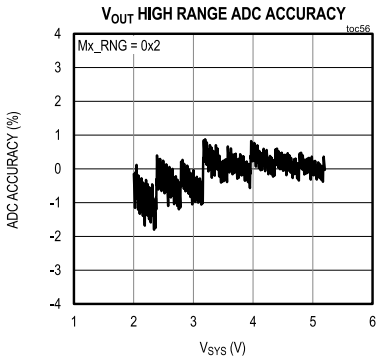
VOUT LOW RANGE ADC ACCURACY

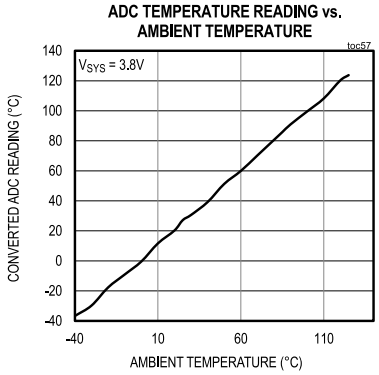


Typical Operating Characteristics (continued)

(V_{IN} = 3.8V, V_{OUT} = 0.65V, L = 0.47µH (Alps GLULMR4701A), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

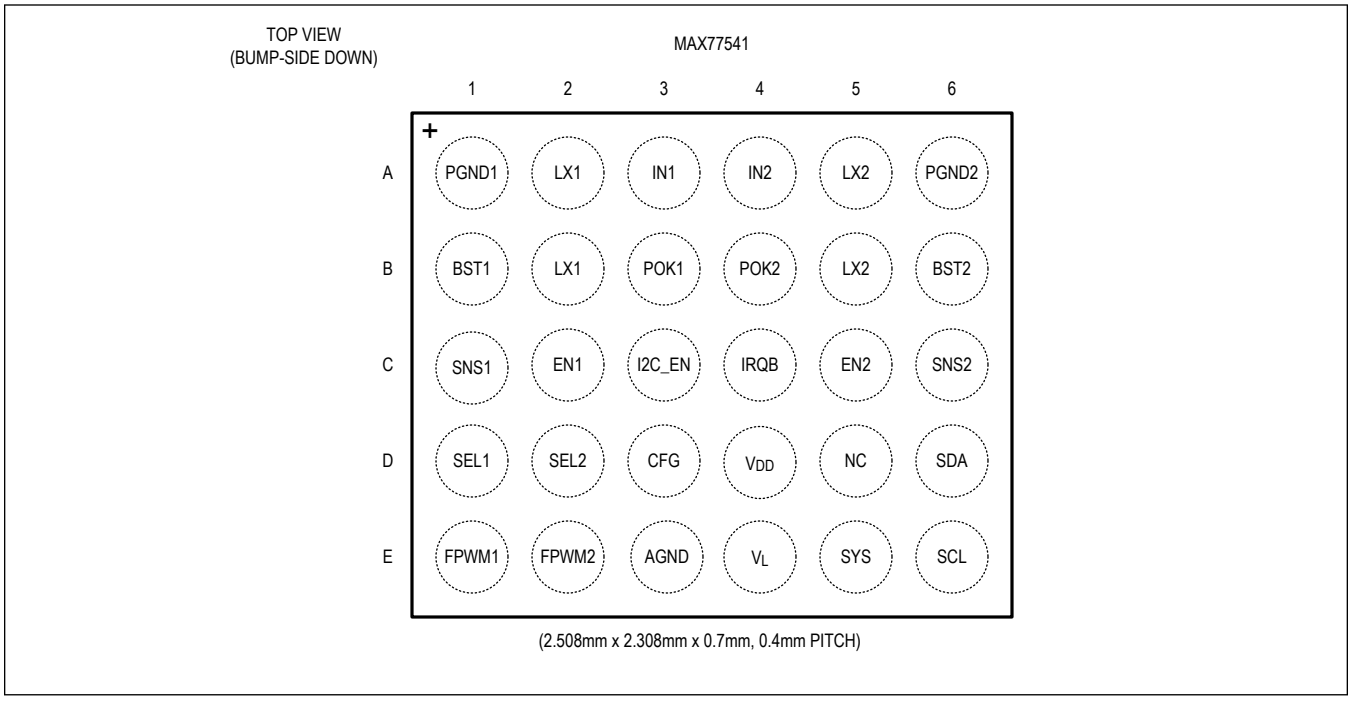




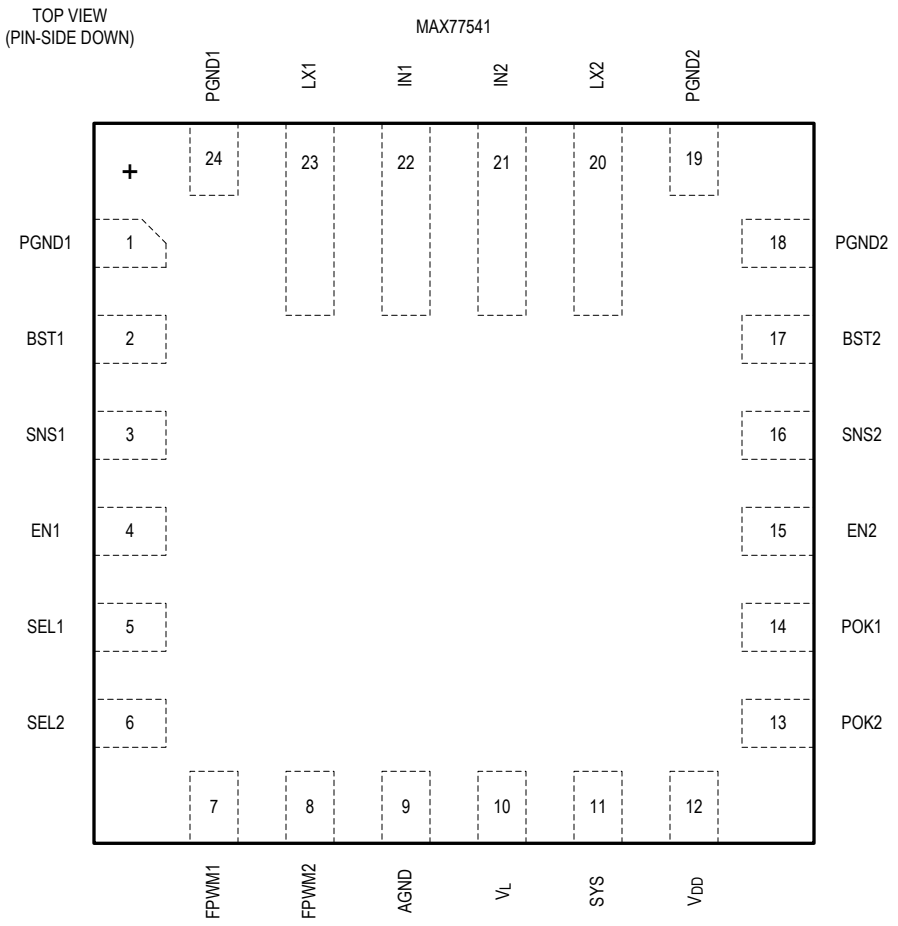


Bump Configuration

30 WLP



24 FC2QFN



Bump Descriptions

PIN		NAME	FUNCTION	TYPE
30 WLP	24 FC2QFN			
BUCK SWITCHING PHASE				
B1	2	BST1	Phase1 High-Side MOSFET Driver Supply. Connect a 0.1µF ceramic capacitor between BST1 and LX1.	Power Input
B6	17	BST2	Phase2 High-Side MOSFET Driver Supply. Connect a 0.1µF ceramic capacitor between BST2 and LX2.	Power Input
A3	22	IN1	Phase1 Input. Bypass to PGND1 with a 10µF ceramic capacitor.	Power Input
A4	21	IN2	Phase2 Input. Bypass to PGND2 with a 10µF ceramic capacitor.	Power Input
A2, B2	23	LX1	Phase1 Switching Node	Power Output
A5, B5	20	LX2	Phase2 Switching Node	Power Output

Bump Descriptions (continued)

PIN		NAME	FUNCTION	TYPE
30 WLP	24 FC2QFN			
A1	1, 24	PGND1	Phase1 Power Ground	Power Ground
A6	18, 19	PGND2	Phase2 Power Ground	Power Ground
C1	3	SNS1	Phase1 Output Voltage Sensing Input. Connect to the output at the point-of-load.	Analog Input
C6	16	SNS2	Phase2 Output Voltage Sensing Input. Connect to the output at the point-of-load. Connect to AGND or leave unconnected (floating) when the phase configuration is set for 2Φ operation.	Analog Input
INTERNAL BIAS SUPPLY				
E3	9	AGND	Analog (Quiet) Ground	Ground
D5	—	NC	No Connection	
E5	11	SYS	System Power Input (Supply to Internal V_L and V_{DD} Linear Regulator). Bypass to AGND with a 2.2µF ceramic capacitor.	Power Input
D4	12	V_{DD}	Internal Bias Supply Output. Powered from SYS. Bypass to AGND with a 1µF ceramic capacitor. Do not load this pin externally.	Power Output
E4	10	V_L	Internal Gate Driver Supply Output. Powered from SYS. Bypass V_L to PGND with a 2.2µF ceramic capacitor. Do not load this pin externally.	Power Output
CONTROL AND SERIAL INTERFACE				
D3	—	CFG	Device Configuration Selection Input. Connect a selection resistor (R_{CFG}) between CFG and AGND to configure I^2C slave address, current limits, and switching frequency. Default settings may be over-written through I^2C. See the *Device Configuration (CFG)* section for more information. In the FC2QFN package option, the CFG pin is left unconnected inside the package.	Analog Input
C2	4	EN1	Buck1 Enable Input (Active-High)	Digital Input
C5	15	EN2	Buck2 Enable Input (Active-High). Connect to AGND for 2Φ operation.	Digital Input
E1	7	FPWM1	Buck1 Forced-PWM Mode Control (Active-High) and External Frequency Tracking Input. Provide an external clock to enable FPWM mode with external frequency stabilization. Connect to AGND if unused. See the *Frequency Tracking (FTRAK)* section for more information.	Digital Input
E2	8	FPWM2	Buck2 Forced-PWM Mode Control (Active-High) and External Frequency Tracking Input. Provide an external clock to enable FPWM mode with external frequency stabilization. Connect to AGND if unused. See the *Frequency Tracking (FTRAK)* section for more information.	Digital Input
C3	—	I2C_EN	I^2C Enable Input (Active-High). Enables I^2C interface and V_L and V_{DD} regulators. See the *Dedicated Internal Supplies* section for more information.	Digital Input
C4	—	IRQB	Interrupt Output (Open-drain, Active Low), This pin requires an external pullup resistor.	Digital Output

Bump Descriptions (continued)

PIN		NAME	FUNCTION	TYPE
30 WLP	24 FC2QFN			
B3	14	POK1	Buck1 Power-OK Output (Open-drain). An external pullup resistor (10kΩ to 100kΩ) is required. Leave this pin unconnected if unused.	Digital Output
B4	13	POK2	Buck2 Power-OK Output (Open-Drain). An external pullup resistor (10kΩ to 100kΩ) is required. Leave this pin unconnected if unused. This pin is pulled low internally when the phase configuration is set for 2Φ operation.	Digital Output
E6	—	SCL	I^2C Serial Interface Clock. Connect to ground if not used.	Digital Input
D6	—	SDA	I^2C Serial Interface Data. Connect to ground if not used.	Digital I/O
D1	5	SEL1	Buck1 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL1}) between SEL1 and AGND to configure the default V_{OUT1} and V_{OUT1} range. Default settings can be overwritten through I^2C. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input
D2	6	SEL2	Buck2 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL2}) between SEL2 and AGND to configure the default target V_{OUT2} and V_{OUT2} range. Default settings can be overwritten through I^2C. When $R_{SEL2} \leq 95.3\Omega$, Buck2 becomes a slave phase of a dual-phase converter. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input

Detailed Description—Top-Level

Dedicated Internal Supplies

The MAX77541 has dedicated internal supplies which are the V_L and the V_{DD}. The V_L provides power to gate drivers for switching MOSFETs, while the V_{DD} provides power for internal logic and control. Those two 1.8V regulators are powered from the SYS input.

When either the I2C_EN or the ENx pin is pulled high, the MAX77541 enables bias circuitry as well as the V_L and the V_{DD} supplies. As soon as the V_{DD} supply becomes stable, the MAX77541 reads the R_{CFG} and the R_{SELx} values to configure the device. While both the V_{SYS} and the V_{DD} are valid, I^2C serial communication is activated. Enabling I^2C by pulling the I2C_EN pin high allows the host processor to modify configuration settings before activating the Buck outputs.

Table 1. V_{DD} and I^2C Enable Truth Table

I2C_EN (PIN)	EN1 OR EN2 (PIN)	V_{DD} and I^2C SERIAL INTERFACE
Low	Low	Disabled
X	High	Enabled
High	X	Enabled

Device Configuration (CFG)

The MAX77541 supports user-selectable device configurations with a 1% tolerance (or better) resistor. The MAX77541 evaluates the resistances between the CFG and the AGND whenever the V_{DD} regulator first turns on (exits shutdown by either the I2C_EN or the ENx pin). The decoded value of the R_{CFG} is latched until the next time the device exits shutdown mode. The CFG_LATCH[4:0] status bits reflect the latched decoded value of the R_{CFG}. See the *Register Map* for more details.

Table 2 decodes the default selection options for I^2C slave address, current limits, and switching frequency. Once latched, the Mx_ILIM[1:0] and the Mx_FREQ[1:0] bits reflect the selected options. The decoded values for R_{CFG} ≥ 75kΩ are programmable at the factory.

Table 2. Device Configuration

R_{CFG} (Ω)	I^2C SLAVE ADDRESS (7-BIT ADDR)	M1_ILIM (A) (1Φ/2Φ)	M2_ILIM (A)	Mx_FREQ (MHz)
≤ 95.3	7'h60 (110 0000)	2.2/3.4	2.2	1.0
200	7'h61 (110 0001)	2.2/3.4	2.2	1.0
309	7'h62 (110 0010)	2.2/3.4	2.2	1.0
422	7'h63 (110 0011)	2.2/3.4	2.2	1.0
536	7'h60 (110 0000)	2.2/3.4	2.2	1.6
649	7'h61 (110 0001)	2.2/3.4	2.2	1.6
768	7'h62 (110 0010)	2.2/3.4	2.2	1.6
909	7'h63 (110 0011)	2.2/3.4	2.2	1.6
1.05k	7'h60 (110 0000)	4.0/4.6	2.2	1.0
1.21k	7'h61 (110 0001)	4.0/4.6	2.2	1.0
1.40k	7'h62 (110 0010)	4.0/4.6	2.2	1.0
1.62k	7'h63 (110 0011)	4.0/4.6	2.2	1.0
1.87k	7'h60 (110 0000)	4.0/4.6	2.2	1.6
2.15k	7'h61 (110 0001)	4.0/4.6	2.2	1.6
2.49k	7'h62 (110 0010)	4.0/4.6	2.2	1.6
2.87k	7'h63 (110 0011)	4.0/4.6	2.2	1.6
3.74k	7'h60 (110 0000)	4.0/4.6	4.0	0.5

Table 2. Device Configuration (continued)

R_{CFG} (Ω)	I^2C SLAVE ADDRESS (7-BIT ADDR)	M1_ILIM (A) (1Φ/2Φ)	M2_ILIM (A)	Mx_FREQ (MHz)
8.06k	7'h61 (110 0001)	4.0/4.6	4.0	0.5
12.4k	7'h62 (110 0010)	4.0/4.6	4.0	0.5
16.9k	7'h63 (110 0011)	4.0/4.6	4.0	0.5
21.5k	7'h60 (110 0000)	4.0/4.6	4.0	1.0
26.1k	7'h61 (110 0001)	4.0/4.6	4.0	1.0
30.9k	7'h62 (110 0010)	4.0/4.6	4.0	1.0
36.5k	7'h63 (110 0011)	4.0/4.6	4.0	1.0
42.2k	7'h60 (110 0000)	4.0/4.6	4.0	1.6
48.7k	7'h61 (110 0001)	4.0/4.6	4.0	1.6
56.2k	7'h62 (110 0010)	4.0/4.6	4.0	1.6
64.9k	7'h63 (110 0011)	4.0/4.6	4.0	1.6
75.0k	7'h60 (110 0000)	Factory Option		
86.6k	7'h61 (110 0001)			
100k	7'h62 (110 0010)			
≥115k	7'h63 (110 0011)			

Output Enable Control

The MAX77541 has dedicated logic input pins (EN1 and EN2) for enabling individual Buck outputs. When the ENx is pulled above the V_{IH} (or tied to SYS), the corresponding Buck output is enabled. In case the MAX77541 exits shutdown mode by the ENx, it takes about 320µs (typ.) to turn on the internal bias circuitry and evaluate the R_{CFG} and the R_{SELx} before propagating the Buck enable signals. To prevent chatter, the ENx pins must be driven either high or low.

The Buck outputs can also be turned on by setting the Mx_EN bits to 1 through the I^2C serial interface. The logical interaction between the enable pins (ENx) and their corresponding I^2C enable bits (Mx_EN) is 'OR'. The serial interface is active whenever the V_{DD} regulator is enabled (See Table 1).

Undervoltage Lock-Out (UVLO)

When the V_{SYS} voltage falls below the V_{UVLO_F} (typ. 2.0V), the MAX77541 disables all individual Buck outputs immediately and resets all Buck configuration registers. See the *Fault Protection* section for more information.

A UVLO event forces the device to a dormant state until the V_{SYS} voltage rises above the UVLO rising threshold (typ. 2.2V). The UVLO falling threshold is programmable through I^2C, but it must be set lower than the UVLO rising threshold to avoid unexpected behaviors. If the V_{SYS} voltage drops down to the POR threshold (typ 1.7V), the V_{DD} supply turns off (all the registers are reset) and the MAX77541 enters shutdown state.

Thermal Warnings and Thermal Shutdown (T_{SHDN})

The MAX77541 has thermal warning to monitor whether the junction temperature rises above +120°C and +140°C. As shown in Figure 1, the device enters thermal shutdown (T_{SHDN}) if the junction temperature exceeds the T_{SHDN} (approximately +165°C typ). A T_{SHDN} event disables all individual Buck outputs immediately and resets all Buck configuration registers. See the *Fault Protection* section for more information. Thermal monitoring is active whenever any of the following conditions are true:

- One of the Buck outputs is enabled
- Force thermal protection enable bit is set (EN_FTMON = 1)
- Thermal protection is enabled (for any reason) and detects $T_J \geq 120°C$ (In this case, thermal monitoring remains active until $T_J \leq 105°C$)

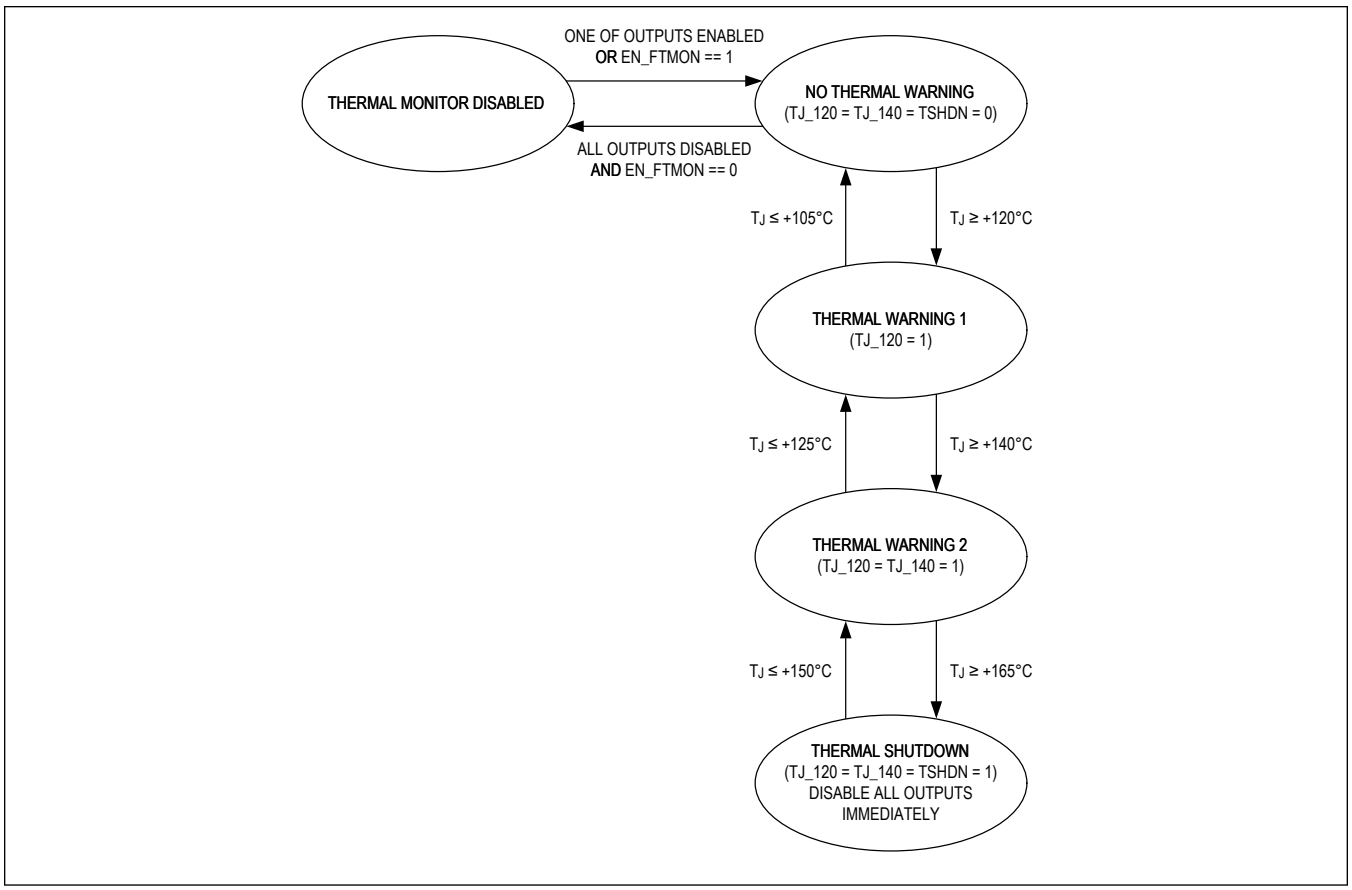


Figure 1. Thermal Warnings and Thermal Shutdown

Interrupt (IRQB) and Mask

The IRQB is an active-low, open-drain output that indicates to the host processor that the status on the MAX77541 has changed. The IRQB is the logical "NOR" of all unmasked interrupt bits. See the *Register Map* for a full list of available status and interrupt bits.

The IRQB output asserts (goes low) anytime an unmasked interrupt bit is triggered. The host processor reads the interrupt source register (ADDR 0x00) and the interrupt registers that are indicated by the interrupt source register to check the cause of the interrupt event. Note that the interrupt source register is cleared when the corresponding interrupt register group is read by the host processor.

All the interrupt events are edge-triggered. Therefore, the same interrupt is not generated repeatedly even though the interrupt condition persists.

Each interrupt register can be read at once and all interrupt bits are "Clear-On-Read" bits. The IRQB output de-asserts (goes high) when all interrupt bits have been cleared. If an interrupt is captured during the read sequence, the IRQB output is held low. When the IRQB output is pulled low by an unmasked interrupt event, the IRQB output stays low until the interrupt bit is cleared by the reading operation of the host processor or the corresponding interrupt mask bit is set to 1 (masked). All interrupts (except UVLO_I) are masked by default. Masked interrupt bits do not cause the IRQB pin to assert.

The MAX77541 has two interrupt mask modes. With MASK_MODE = 0 (default), an interrupt bit is set for an interrupt event regardless of the corresponding mask bit, however the interrupt event does not propagate to the interrupt source register when masked. When the MASK_MODE is set to 1, it prevents the interrupt register bit from asserting for the corresponding interrupt event (gated at the interrupt bit).

Register Reset Condition

All registers are reset to the POR default values specified in the register map section when the MAX77541 enters shutdown mode (I2C_EN = ENx = Low) or the V_{SYS} supply drops below its POR threshold (typ. 1.7V). Whenever the I2C_EN or the ENx pin is pulled high, the MAX77541 updates the default register values of the Mx_VOUT[7:0], the Mx_RNG[1:0], the Mx_ILIM[1:0], and the Mx_FREQ[1:0] bits based on R_{CFG} and R_{SELx} detection, and the updated default values are latched until both the I2C_EN and the ENx pins are pulled low or a POR event occurs.

FC2QFN Default Options

The FC2QFN package has a reduced set of features due to the the lack of SDA and SCL pins for I^2C communication and the ALT_IN pin. The default register settings cannot be changed. The following is a list of features not available in the FC2QFN package:

- The alternative low-voltage input feature is not available.
- Output enable control can only be performed using the hardware ENx pins.
- Thermal warnings are not accessible.
- Interrupt pin and registers are not accessible.
- Low-power SKIP mode is not available (the FPWMx pins can be used to toggle between SKIP and FPWM modes).
- Only V_{OUTx} options available through the R_{SELx} pins can be programmed.
- Configuring F_{SW} and Mx_ILIM through the CFG pin is unavailable.
- F_{SW} is default to 1MHz.
- Mx_ILIM is default to 4.0A.
- Dynamic output voltage scaling is not available.
- The 7Ω active discharge resistor is disabled.
- Spread spectrum modulation cannot be enabled.

Detailed Description—Dual-Phase Configurable Buck Converter

The MAX77541 is a high-efficiency, phase-configurable Buck converter with two 3A phases (Φ). Two output voltage sensing inputs allow up to two regulated outputs. Each Buck converter operates on an input supply between 2.2V and 5.5V. The output voltages are preset using the SELx inputs and further configurable with an I^2C serial interface between 0.3V and 5.2V in 5mV, 10mV, or 20mV steps depending on the Mx_RNG[1:0] registers. See the *Output Voltage Setting* section.

Each switching phase supports 3A and dual-phase (2Φ) configuration supports up to 6A. The phase configuration is user-programmable by tying the SEL2 pin to the AGND on the PCB. See the *Phase Configuration* section.

Buck Converter Control Scheme

The MAX77541 uses Maxim's proprietary adaptive COT (constant on-time) current-mode control scheme. The adaptive COT control provides fast response to load transients, inherent compensation to input voltage variation, and stable performance at low duty cycles. As shown in Figure 2, Buck1 is referenced in the following explanation.

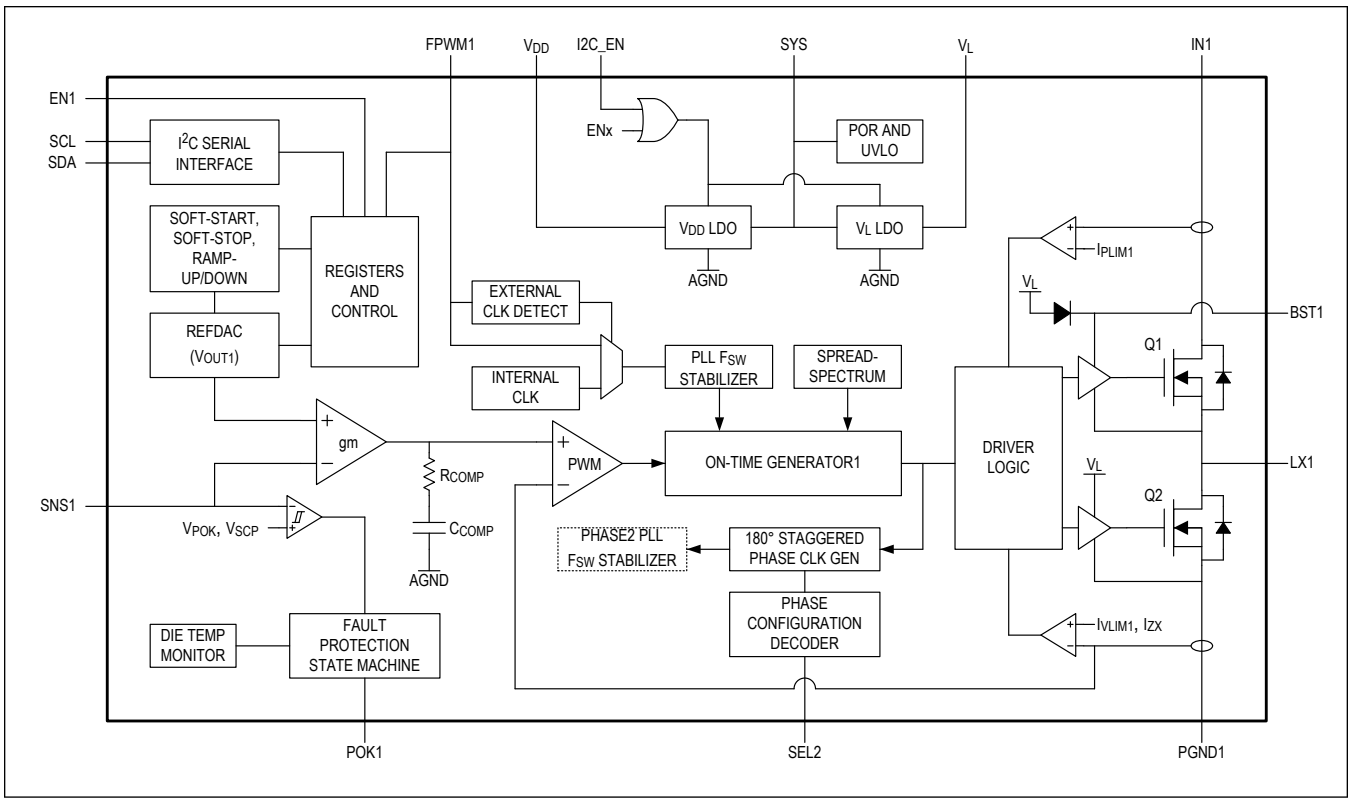


Figure 2. Functional Block Diagram

An on-time (MOSFET Q1 is on) is controlled by an on-time generator circuit and this circuit calculates an on-time based on the input voltage (V_{IN1}), the output voltage (V_{OUT1}), and the target switching frequency (F_{SW1}). An off-time (MOSFET Q2 is on) begins when the on-time ends. During the dead-time, the inductor current conducts through the intrinsic body diode. A PWM comparator regulates the V_{OUT1} by modulating off-time. The positive input of the PWM comparator is a voltage proportional to the actual output voltage error. The negative input is a voltage proportional to the inductor current sensed through the MOSFET Q2. The PWM comparator begins an on-time when the error voltage becomes higher than the current-sense signal. The off-time automatically begins again when the calculated on-time expires. A phase-locked loop (PLL) stabilizes the switching frequency and controls phase spacing. The PLL stabilizes Phase2 (LX2) 180° apart from Phase1 when the output is configured for the dual-phase (2Φ) operation. In dual-phase configuration, both the master and the slave phases are activated and always switch in sequence during steady-state operation. The phases do not add or shed.

Buck Operating Modes

The Buck converters have three operating modes shown in Figure 3 and transitions between the modes are determined by operating conditions and mode control settings. The operating mode setting can be changed any time while I^2C communication is available. Toggling between SKIP and FPWM modes is also controlled by the FPWMx pins. Pulling the FPWMx pin high to operate the corresponding Buck in forced-PWM mode. When the FPWMx pin is held low, the operating mode is controlled by the Mx_LPM and the Mx_FPWM bits.

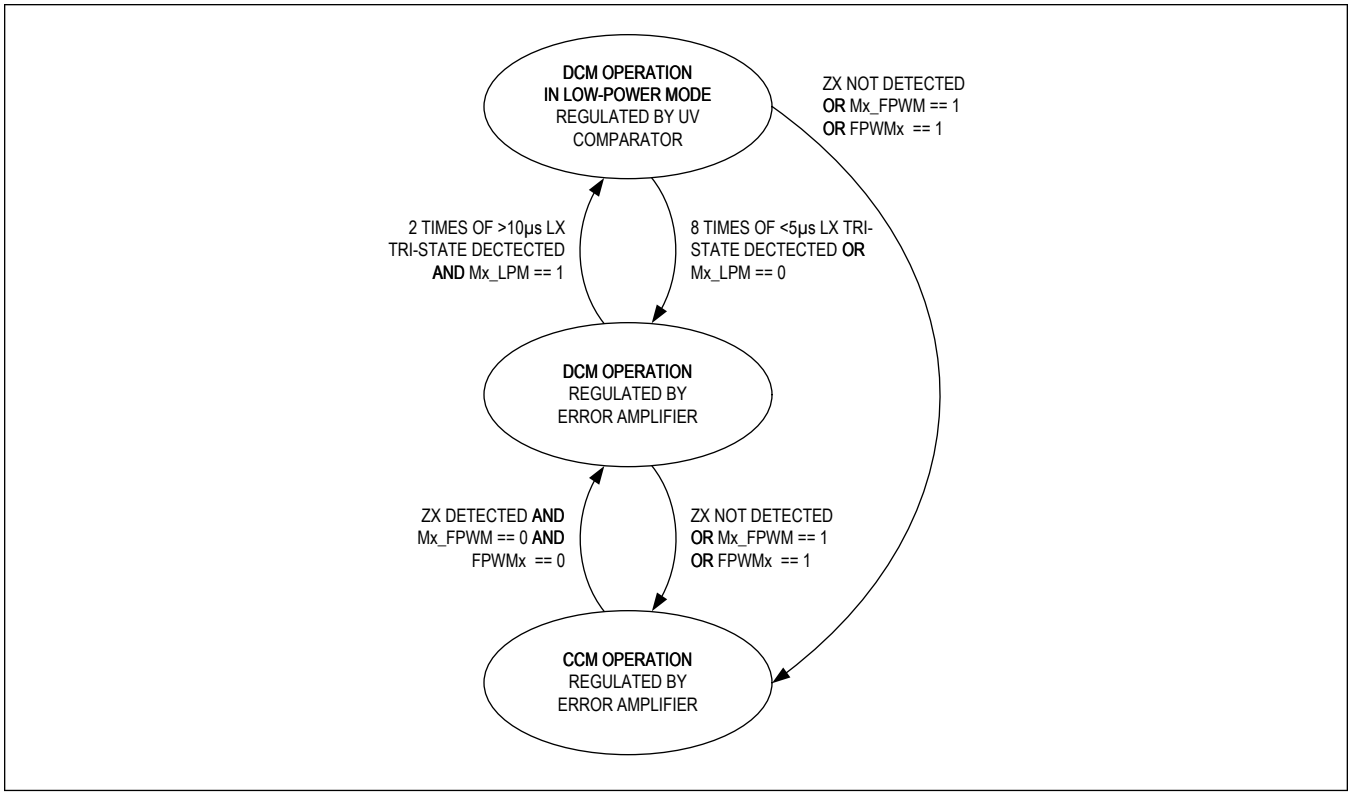


Figure 3. Buck Operating Modes

Detail mode control settings are described below:

SKIP Mode

In SKIP mode (Mx_LPM == Mx_FPWM == FPWMx == 0), the Buck converter operates either in DCM (Discontinuous Conduction Mode) or CCM (Continuous Conduction Mode) depending on loading. If the averaged output current is lower than a half of inductor peak-to-peak ripple current under light load condition, the low-side MOSFET turns off as soon as the inductor current drops to near zero ampere (zero-crossing). Then, the switching node (LX) remains in tri-state (Hi-Z) until the next on-time is triggered. In this way, the Buck prevents a negative inductor current which results in improving light-load efficiency by reducing the total number of switching cycles needed to regulate the output voltage.

When no zero-crossing (ZX) is detected (under heavier load), the Buck controller goes into CCM where the averaged output current is greater than a half of inductor ripple current. In both DCM and CCM, the output voltage is regulated by an error amplifier. In case the on-time determined by a given operating condition in high output voltage range (Mx_RNG[1:0] = 0x2) is not long enough, the on-time automatically extends until the inductor current reaches 660mA to ensure enough off-time to detect the ZX reliably.

Low-Power SKIP (LP-SKIP) Mode

Low-power SKIP mode (Mx_LPM == 1 **AND** Mx_FPWM == FPWMx == 0) is similar to SKIP mode becasue a negative inductor current is not allowed in LP-SKIP mode as well. When the averaged output current is decreased further down (>10µs of LX tri-state is detected two times consecutively) in SKIP mode, the Buck converter enters LP-SKIP mode when Low Power mode is enabled. In LP-SKIP mode, the error amplifier and other internal blocks are deactivated to reduce IQ consumption. Instead of the error amplifier, a low-power comparator monitors the output voltage in LP-SKIP mode.

The Buck enters DCM operation in SKIP mode when the duration of LX tri-state is shorter than 4µs for eight times in a row or LP-SKIP mode is disabled (Mx_LPM = 0). If zero-crossing is not detected (e.g., sudden load transient) or FPWM mode is enabled (Mx_FPWM = 1 **OR** FPWMx = 1), the Buck enters CCM operation directly from LP-SKIP mode.

Forced-PWM (FPWM) Mode

Forced-PWM mode (Mx_FPWM == 1 **OR** FPWMx == 1) ensures a continuous inductor current under all load conditions. In FPWM mode, a negative inductor current through the low-side MOSFET is allowed but the maximum current is limited to I_{NLIM} (typ -3A). When the Buck converters enter/exit FPWM mode by the FPWMx inputs, there is 1ms of delay in mode transition due to 1ms of debounce timer on the FPWMx inputs. In case a valid external frequency is detected on the FPWMx input, the corresponding Buck enters FPWM mode regardless of its operating mode settings. See the *Frequency Tracking (FTRAK)* section for more information.

Dropout Mode

The MAX77541 architecture allows the Buck converter to operate even when the input voltage approaches the target output voltage. When the headroom between the input and the output voltages reduces during operation, the Buck controller tries to maintain the output voltage regulation by increasing the duty cycle. In case the Buck is not able to regulate the target output voltage with the maximum duty cycle (typ 98%), it automatically extends the on-time by skipping the off-times (drop-out mode). In drop-out mode, the low-side MOSFET turns on occasionally in order to refresh the bootstrap circuit for driving the high-side MOSFET. See the *Bootstrap Refresh* section for more information.

Switching Frequency

The MAX77541 has three nominal switching frequency options (0.5MHz, 1.0MHz, and 1.6MHz) to optimize the efficiency, the transient response, the noise performance, and the solution size. The default switching frequency of the Bucks are set by the CFG input (see Table 2) and the switching frequencies of individual Bucks are also selectable with the Mx_FREQ[1:0] bits.

At any given time, the switching frequency (F_{SW}) of the adaptive on-time Buck converter is not fixed and is heavily influenced by the instantaneous load current. More on-time pulses in a given time (higher F_{SW}) are observed as the output current increases, while fewer on-times in a given time (lower F_{SW}) are observed when the output current decreases. A valid external frequency at the FPWMx input or enabling the internal frequency tracking feature (Mx_FTRAK = 1) stabilizes the switching frequency of the corresponding Buck in steady-state operation. See the *Frequency Tracking (FTRAK)* section for more information.

In case the on-time calculated by the given operating condition is less than the minimum on-time (typ 60ns), the Buck controller regulates the output voltage by increasing the off-time. As a result, the actual switching frequency becomes slower than its nominal frequency setting. For example, the calculated duty cycle for 5.5V_{IN} and 0.5V_{OUT} is about 9.1%, which gives less than 60ns of on-time at 1.6MHz of nominal switching frequency. It means that the actual switching frequency under this condition is slower than 1.6MHz, so a 1MHz or slower nominal switching frequency setting is recommended.

Phase Configuration

The MAX77541 has two 3A switching phases configurable to either two single-phase Bucks or one dual-phase Buck. As shown in Table 3, the Buck is configured as single-output dual-phase (2Φ) when the SEL2 is shorted to the AGND. In dual-phase (2Φ) configuration, logic I/O pins and control registers for Buck2 are deactivated so that register settings of the master phase (M1) dictate the operation of the slave phase as well.

Table 3. Phase Configuration Selection

R_{SEL1} (Ω)	R_{SEL2} (Ω)	PHASE (Φ) CONFIGURATION	NUMBER OF OUTPUTS
Any	≤ 95.3	2Φ	1
Any	≥ 200	1Φ + 1Φ	2

Also, the output voltage sensing of the Buck converter is assigned based on the phase configuration setting. In dual-phase configuration, the Buck controller regulates the output voltage using the SNS1 pin only (the SNS2 pin is unused). Table 4 shows how to configure the output voltage sensing pins for each phase configuration.

Table 4. Buck Output Voltage Sensing Assignment

PHASE (Φ) CONFIGURATION	PHASE ASSIGNED	BUCK NAMING CONVENTION	V_{OUT} SENSING INPUT
2Φ (1 Output)	Phase1 (M1) Phase2 (S)	Buck1 (V_{OUT1})	SNS1
1Φ + 1Φ (2 Outputs)	Phase1 (M1)	Buck1 (V_{OUT1})	SNS1
	Phase2 (M2)	Buck2 (V_{OUT2})	SNS2
(Mx): Master Phase (S): Slave Phase			

Default Output Voltage Selection (SELx)

The MAX77541 supports user-selectable default voltages of individual Buck outputs with 1% tolerance (or better) resistors. The MAX77541 evaluates the resistances between the SELx and the AGND whenever the V_{DD} regulator first turns on (exits shutdown by either the I2C_EN or the ENx). The decoded values of the R_{SELx} are latched until the next time the device exits shutdown mode. The SELx_LATCH[4:0] status bits reflect the latched decoded values of the R_{SELx}. See the *Register Map* for more details.

The resistance between the SEL1 and the AGND (R_{SEL1}) configures the default voltage of Buck1, while the R_{SEL2} between the SEL2 and the AGND configures Buck2 default voltage. If the SEL2 pin is tied to the AGND on the PCB (R_{SEL2} ≤ 95.3Ω), the Buck is configured as a single-output dual-phase (2Φ) converter. When the dual-phase operation is selected, the decoded resistance on the SEL1 (R_{SEL1}) sets the default output voltage (V_{OUT1}). Table 5 and Table 6 decode the default selection options for the V_{OUT1} and the V_{OUT2} respectively. Once latched, the Mx_VOUT[7:0] and the Mx_RNG[1:0] bits reflect the selected options. The decoded values for R_{SELx} ≥ 115kΩ are programmable at the factory.

Table 5. Default V_{OUT1} Selection

R_{SEL1} (Ω)	TARGET V_{OUT1} (V)	V_{OUT1} RANGE
≤ 95.3	0.300	Low
200	0.400	Low
309	0.500	Low
422	0.550	Low
536	0.600	Low
649	0.650	Low
768	0.675	Low
909	0.700	Low
1.05k	0.720	Low

Table 5. Default V_{OUT1} Selection (continued)

R_{SEL1} (Ω)	TARGET V_{OUT1} (V)	V_{OUT1} RANGE
1.21k	0.750	Low
1.40k	0.800	Low
1.62k	0.820	Low
1.87k	0.850	Low
2.15k	0.900	Low
2.49k	0.950	Low
2.87k	1.000	Low
3.74k	1.050	Low
8.06k	1.100	Low
12.4k	1.150	Low
16.9k	1.200	Low
21.5k	1.25	Mid
26.1k	1.35	Mid
30.9k	1.40	Mid
36.5k	1.50	Mid
42.2k	1.80	Mid
48.7k	2.00	Mid
56.2k	2.50	High
64.9k	2.80	High
75.0k	3.30	High
86.6k	3.40	High
100k	3.80	High
≥ 115k	Factory Option	

Table 6. Default V_{OUT2} Selection

R_{SEL2} (Ω)	TARGET V_{OUT2} (V)	V_{OUT2} RANGE
≤ 95.3	N/A (2Φ Operation)	
200	0.500	Low
309	0.550	Low
422	0.600	Low
536	0.650	Low
649	0.700	Low
768	0.720	Low
909	0.750	Low
1.05k	0.800	Low
1.21k	0.820	Low
1.40k	0.850	Low
1.62k	0.900	Low
1.87k	0.950	Low
2.15k	1.000	Low
2.49k	1.050	Low
2.87k	1.100	Low

Table 6. Default V_{OUT2} Selection (continued)

R_{SEL2} (Ω)	TARGET V_{OUT2} (V)	V_{OUT2} RANGE
3.74k	1.150	Low
8.06k	1.200	Low
12.4k	1.25	Mid
16.9k	1.35	Mid
21.5k	1.40	Mid
26.1k	1.50	Mid
30.9k	1.80	Mid
36.5k	2.00	Mid
42.2k	2.50	High
48.7k	2.80	High
56.2k	3.00	High
64.9k	3.30	High
75.0k	3.40	High
86.6k	3.80	High
100k	4.30	High
≥ 115k	Factory Option	

Output Voltage Setting

The output voltages (V_{OUTx}) are adjustable between 0.3V and 5.2V in 5mV, 10mV, or 20mV steps depending on the Mx_RNG[1:0] bits as shown in Table 7. Note that the Mx_RNG[1:0] bits must not be changed while the corresponding Buck is enabled.

In each output voltage range, the lowest code (0x00) of the Mx_VOUT[7:0] bits represents the minimum output voltage and the target output voltage is increased by one LSB step as the code increases. The maximum programmable output voltage is digitally limited to the maximum output voltage in each range even if the code increases beyond that point. The default values of the Mx_VOUT[7:0] and the Mx_RNG[1:0] bits are set by the corresponding RSELx values. See the *Default Output Voltage Selection (SELx)* section for more information.

For output voltages that have overlapping ranges (e.g., 1V), select the desired range by trading off the load transient response and the required effective output capacitance. Using the 1V output example: use low-range for a slightly better load transient response, or mid-range for a slightly worse transient response but with less effective output capacitance requirement. See the *Output Capacitor Selection* for more information on the required effective output capacitance for the different output voltage ranges.

Table 7. Buck Output Voltage Range

Mx_RNG[1:0]	V_{OUT} PROGRAMMING RANGE	STEP PER LSB
0x0 (Low-range)	0.3V to 1.2V	5mV
0x1 (Mid-range)	1.0V to 2.4V	10mV
0x2 (High-range)	2.0V to 5.2V	20mV

Soft-Start and Soft-Stop

The Bucks always soft-start whenever they are enabled (regardless of the ENx or I^2C command) or when recovering from a fault condition. When the individual Buck is disabled by the ENx or I^2C command, the Buck always initiates soft-stop. If a POK fault time-out or a SCP event occurs to a Buck output, only the corresponding Buck stops switching immediately (LX node becomes Hi-Z) without affecting the operation of the other Buck. In case an UVLO or a T_{SHDN} fault happens, all Buck outputs stop switching immediately.

The Bucks have internal ramps that control the slew-rate of output voltage changes during soft-start and soft-stop.

The soft-start and the soft-stop slew-rates are set individually by the SSTRT_SR[2:0] and the SSTOP_SR[2:0] bits respectively, and they are global settings for all Buck phases. During soft-start and soft-stop, the Buck automatically enters FPWM mode regardless of operating mode settings when the Mx_FSREN bit is set to 1 (default). To support "prebiased" startup (startup without discharging preexisting voltage at the output), the Mx_FSREN and the Mx_ADIS100 bits need to be set to 0 before the Buck is enabled.

The SSTRT_SR[2:0] and the SSTOP_SR[2:0] bits set the slew-rates of a voltage reference to an error amplifier. When the fastest slew-rate option is selected, the actual output voltage slew-rate might be slower than the target setting due to limited sourcing and the sinking current capabilities of Bucks under given circuit parameters and operating conditions. See Table 8 for more information.

Dynamic Output Voltage Scaling

Whenever a new target value is written in the Mx_VOUT[7:0] bits through I^2C while the corresponding Buck is enabled, the output voltage starts to change. The output voltage ramps up (or down) at a positive (or negative) slew-rate set by the corresponding Mx_RU_SR[2:0] (or Mx_RD_SR[2:0]) bits. When the Mx_FSREN bit is set, the corresponding Buck enters FPWM mode automatically (regardless of the Mx_FPWM bit) during the output voltage ramp-down (or soft-stop). In FPWM mode, the Buck can sink current from the C_{OUTx} to the PGNDx through the low-side MOSFET which allows the V_{OUTx} to track the negative rate set by the Mx_RD_SR[2:0] bits.

Table 8. Mx_FSREN Effect On Buck Behavior

OPERATING MODE	Mx_FSREN	BUCK BEHAVIOR IN STEADY STATE	BUCK BEHAVIOR DURING DVS
SKIP or LP-SKIP	0	Source Only	Source Only
	1	Source Only	Source or Sink
FPWM	X	Source or Sink	Source or Sink
Note: Buck outputs (V_{OUTx}) with current sinking capability can follow negative ramp rates set by the Mx_RD_SR[2:0] or the SSTOP_SR[2:0].			

If the negative inductor current reaches the I_{NLIM} (typ -3A), the low-side MOSFET is turned off immediately and the Buck initiates a new on-time (high-side MOSFET turn-on). Thus, the maximum slew-rate during output voltage ramp-down (or soft-stop) is limited if an effective output capacitance is very high for the selected ramp-down (or soft-stop) slew-rate. The maximum output voltage slew-rate is calculated by following formula, $dV_C/dt = i_C/C$.

Output Voltage Active Discharge

Each Buck converter integrates a 100Ω active discharge resistor between the LXx and the PGNDx for discharging the output capacitor when the Buck output is disabled. For faster output voltage discharge at the end of soft-stop, a 7Ω active discharge function is added between the SNSx and the PGNDx. Those two active discharge resistors are individually enabled by setting the Mx_ADIS100 and the Mx_ADIS7 bits respectively. If both the Mx_ADIS100 and the Mx_ADIS7 are set to 1, the 7Ω active discharge is first activated for 1ms right after soft-stop is completed, and then the 100Ω active discharge is enabled until the next time the Buck is enabled. In shutdown mode (I2C_EN = EN1 = EN2 = 0), the 100Ω active discharge of each Buck phase is enabled by default.

Note that the 7Ω active discharge function of the corresponding output must be disabled (Mx_ADIS7 = 0) to avoid excessive power dissipation when the falling slew-rate control feature is disabled (Mx_FSREN = 0).

Bootstrap Refresh

When the Buck is in drop-out operation or in SKIP (or LP-SKIP) mode under extremely light load condition, the low-side MOSFET does not turn on for a long period of time. In this case, the Buck controller occasionally turns on the low-side MOSFET for about 100ns (typ) in order to charge a bootstrap circuit for driving the high-side MOSFET. The bootstrap refresh interval is set to 128µs by default. The bootstrap refresh interval can be reduced to 10µs when the Mx_REFRESH bit is set to '1'. The bootstrap refresh interval selection is shown in Table 9.

Table 9. Bootstrap Refresh Interval Selection

Mx_REFRESH	REFRESH INTERVAL
0	128µs
1	10µs

The bootstrap refresh is also required when the Buck converter starts switching. As a part of the startup procedure, the Buck controller forces refresh pulses 16 times with an interval of 3µs.

Frequency Tracking (FTRAK)

The MAX77541 supports the frequency tracking feature. When a valid external clock is detected on the FPWMx input (triggers the EXT_FREQ_DET_I interrupt if unmasked), the corresponding Buck converter enters FPWM mode regardless of its operating mode setting and tracks the external frequency by modulating on-times. Buck1 attempts to track the beginning of on-times to the falling edges of the external clock on the FPWM1 input, while Buck2 attempts to track the beginning of on-times to the rising edges of the external clock on the FPWM2 input. The external frequency detection is deactivated when all Buck outputs are disabled.

Table 10. Mx_FTRAK Enable Truth Table

EXT_FREQ_DET	Mx_FTRAK	PLL	BUCK OPERATING MODE	NOTE
0	0	Disabled	Depends on Buck Mode Setting	No Tracking
0	1	Enabled	Depends on Buck Mode Setting	Internal Freq. Tracking
1	0	Enabled	FPWM	External Freq. Tracking
1	1	Enabled	FPWM	External Freq. Tracking

As shown in Table 10, the Bucks can also track an internal clock. When the FTRAK function is enabled (Mx_FTRAK = 1), the corresponding Buck tracks the internal PLL frequency (set by the Mx_FREQ[1:0] bits) if no valid external clock is applied. In case a valid external clock is detected while the corresponding Buck is tracking the internal PLL, it switches to the external clock tracking. The frequency window for both external and internal tracking is about ±5% of the nominal switching frequency. The frequency tracking operation is valid whenever one of Buck converters is enabled regardless of the I2C_EN pin status. The FPWM1 and the FPWM2 must be driven either low or high to prevent chattering or false tracking.

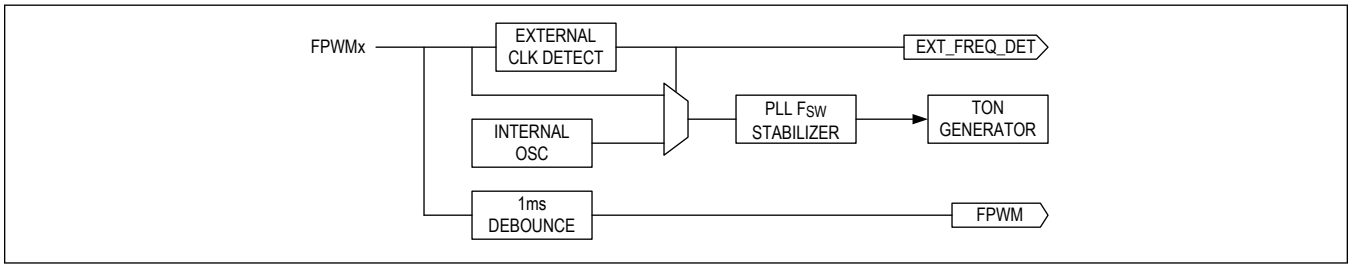


Figure 4. Frequency Tracking

Note that the frequency tracking feature is deactivated if the on-time determined by the operating condition is less than 60ns.

Spread-Spectrum Modulation

The Bucks are capable of dithering its switching frequency for noise-sensitive applications. Spread-spectrum function of each Buck is individually enabled by setting the Mx_SS_ENV[1:0] bits. The spread-spectrum function is activated only in CCM (Continuous Conduction Mode) and it is automatically deactivated when the Bucks enter DCM (Discontinuous Conduction Mode). The spread-spectrum modulation pattern is programmable either in pseudo-random or triangular patterns by the Mx_SS_PAT[1:0] bits. Spread-spectrum modulation is characterized by modulation envelope and modulation frequency:

- The modulation envelope (ΔF_{SS}) determines the maximum difference between the modulated switching frequency and the nominal switching frequency. The modulation envelope is programmable (±8%, ±12%, or ±16%) with the Mx_SS_ENV[1:0] bits and it controls how wide the switching frequency dithers
- The modulation frequency (F_{SS_MOD}) determines how often the switching frequency changes from one value to another. The modulation frequency is also programmable (1kHz, 3kHz, 5kHz or 7kHz) with the Mx_SS_FREQ[1:0] bits and it controls how fast the switching frequency dithers

Pseudo-Random Pattern

The pseudo-random engine uses a 4-bit linear feedback shift register (LFSR) to create a pseudo-random value as shown in Figure 5. The LFSR value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The pseudo-random value shortens or lengthens the on-time. This causes the Buck controller to increase or decrease the switching frequency to maintain voltage regulation. Each Buck has its own pseudo-random pattern generator.

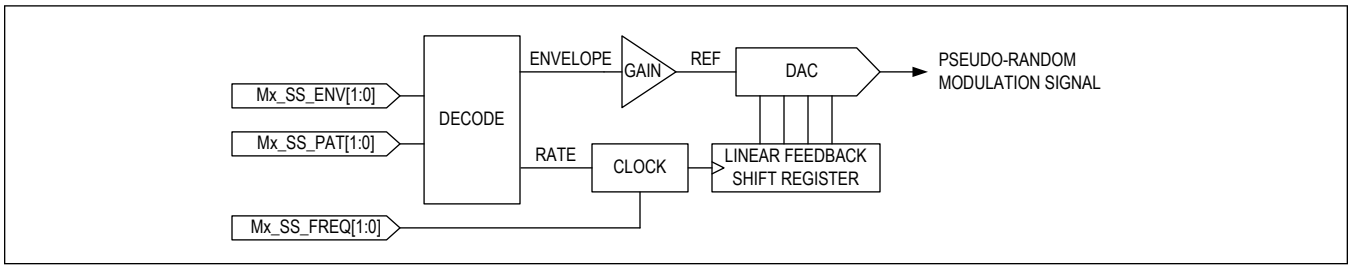


Figure 5. Pseudo-Random Modulator Engine

The modulation envelope and frequency are programmable with the Mx_SS_ENV[1:0] and the Mx_FREQ[1:0] bits. The F_{SS_MOD} sets the frequency at which the LFSR wraps back to the seed value. The clock rate of the LFSR is the F_{LFSR}. This is the frequency at which one pseudo-random value changes to another. An example is shown in Figure 6.

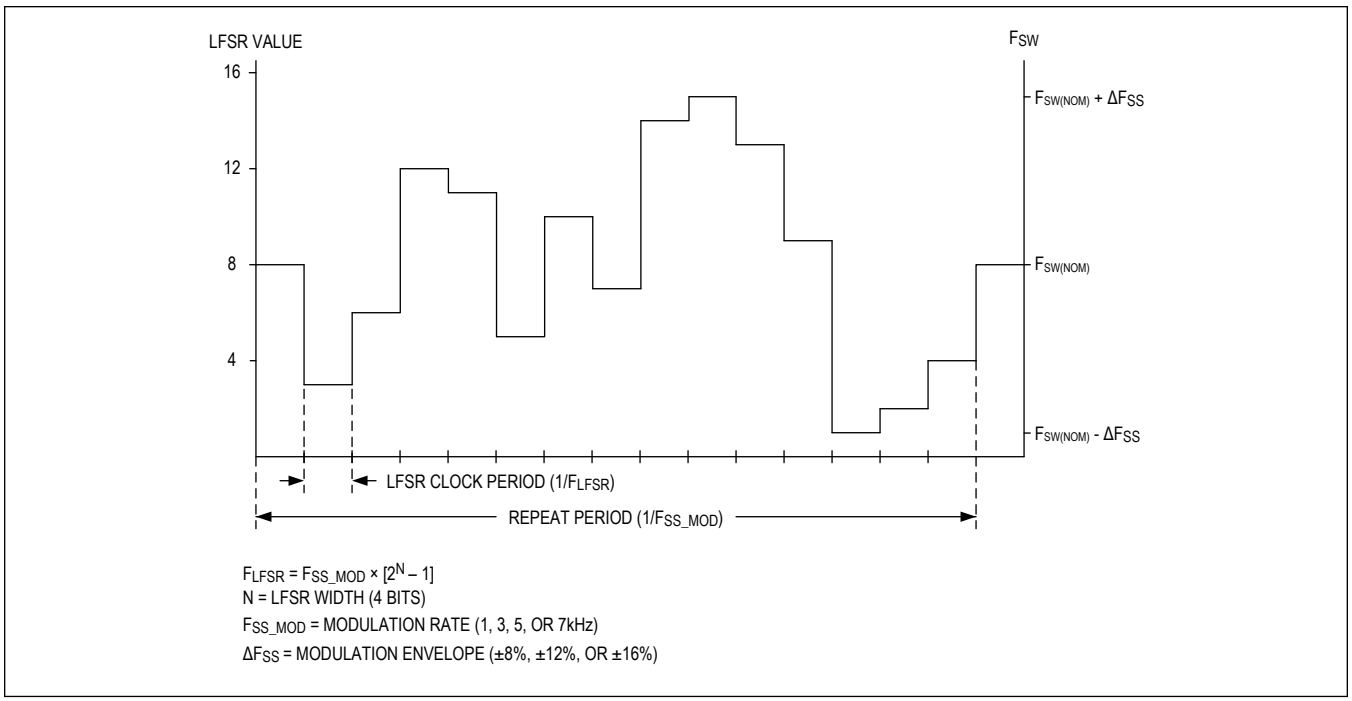


Figure 6. 4-Bit Pseudo-Random Modulation Signal Example

Triangular Pattern

The triangular engine uses a 4-bit up/down synchronous counter to create a stepped triangle pattern as shown in Figure 7. The counter value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The counter value progressively shortens and lengthens the on-time. This causes the Buck controller to progressively increase and decrease the switching frequency to maintain voltage regulation. Each Buck has its own triangular pattern generator.

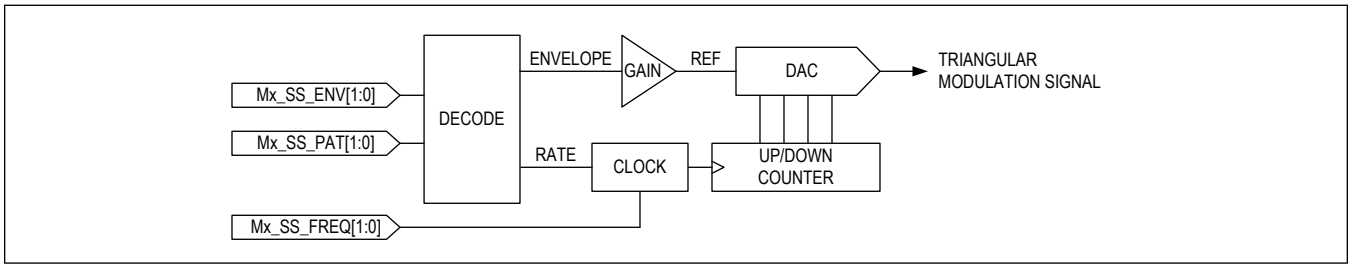


Figure 7. Triangular Modulator Engine

The modulation envelope and frequency are programmable with the Mx_SS_ENV[1:0] and the Mx_FREQ[1:0] bits. The F_{SS_MOD} sets the frequency at which the counter returns to the same value. The clock rate of the counter is the F_{COUNT}. This is the frequency at which the frequency changes from one value to another. An example is shown in Figure 8.

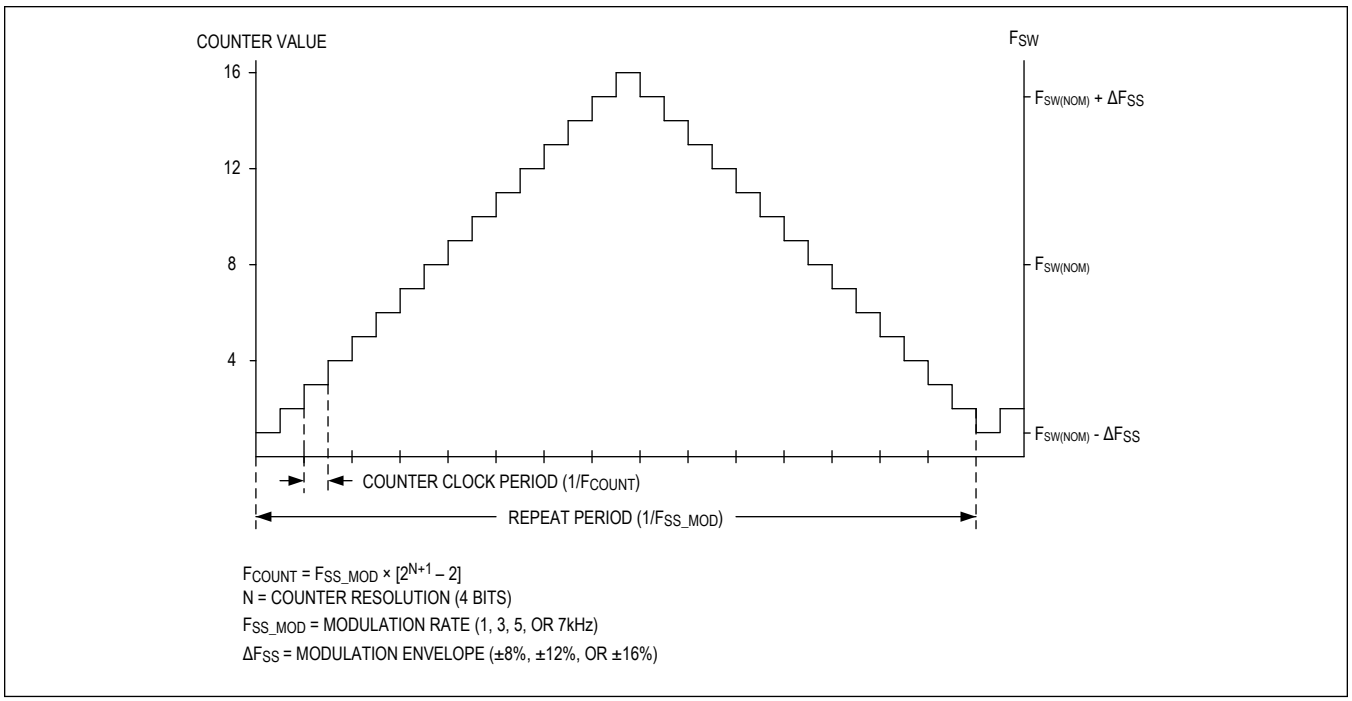


Figure 8. 4-Bit Triangular Modulation Signal Example

Inductor Current Limits

The MAX77541 has a cycle-by-cycle current limit feature that prevents the inductor current in each phase from increasing beyond the I_{PLIM}. If an on-time is ended by the peak current limit, the Buck prevents a new on-time from starting until the inductor current falls below the valley current limit (I_{VLIM}) which is typically set 1A less than the I_{PLIM}. This prevents the inductor current from increasing uncontrollably due to the overloaded output. In case the on-time determined by the given operating condition is less than 130ns (typ), the next on-time pulse is not triggered until the inductor current hits the I_{VLIM}. Each Buck has four PLIM thresholds which are individually set with the Mx_ILIM[1:0] bits. See the *Register Map* for more details. The programmable PLIM thresholds allow an optimal circuit protection and inductor selections for the given operating conditions and load requirements.

Power-OK (POK)

The MAX77541 features the Power-OK (POK) comparators to monitor the quality of each Buck output. The Mx_POK status bits continuously reflect the status of these monitors. The Mx_POK bit goes high if the corresponding Buck output voltage rises above the V_{POK_R} (typ 82% of the V_{OUT} target) when soft-start is completed. When the corresponding Buck output falls below the V_{POK_F} (typ 78% of the V_{OUT} target), the Mx_POK bit goes low. When unmasked, the Mx_POKFLT_I interrupt sets whenever the Mx_POK status bit changes from 1 to 0. The Mx_POKFLT_I bits are individually maskable. See the *Register Map* for more details.

The quality of Buck outputs can be directly monitored using the POKx pins. The POKx is an active-high, open-drain output that requires an external pullup resistor (typ 10kΩ to 100kΩ).

Fault Protection

The MAX77541 has a fault protection scheme designed to protect itself from abnormal conditions. Each individual Buck has its own fault state machine (shown in Figure 9) which is independently triggered by a short-circuit protection (SCP), a thermal shutdown (T_{SHDN}), and/or an undervoltage lockout (UVLO) event. The operation of the state machine is summarized as follows:

- If the V_{SYS} falls below the V_{UVLO_F} (typ. 2.0V), then all individual Buck outputs are disabled immediately (the UVLO_I interrupt asserts) and all Buck configuration registers are reset to their default values (enters BUCKx OUTPUT OFF state)
- If one of the enabled Buck outputs falls below the V_{POK_F} (typ 78% of regulation target), then the Mx_POKFLT_I asserts
- If one of the enabled Buck outputs stays below the V_{POK_R} (typ 82% of regulation target) for longer than t_{POK_TO}, then only the corresponding output is disabled immediately and its Buck configuration registers are reset to their default values
- If one of enabled Buck outputs falls below the V_{SCP} (typ 20% of regulation target), then only the corresponding output is disabled immediately (the Mx_SCFLT_I interrupt asserts) and its Buck configuration registers are reset to their default values
- If the junction temperature exceeds the T_{SHDN} (typ 165°C), then all individual Buck outputs are disabled immediately (the TSHDN_I interrupt asserts) and all Buck configuration registers are reset to their default values
- POK and SCP monitoring is not active (masked) during soft-start and soft-stop

When a POK time-out, SCP, and/or T_{SHDN} fault occurs, the corresponding Buck enters either the LATCH-OFF or WAIT state from the RESET state, depending on the AUTO_RSTRT bit setting.

- If AUTO_RSTRT = 0,
  - The output of individual Buck is forced disabled in LATCH-OFF state
  - When ENx == Mx_EN == 0 **AND** $T_J \le +150°C$, the individual Buck exits LATCH-OFF state and enters BUCKx OUTPUT OFF state
- If AUTO_RSTRT = 1,
  - After 500ms of forced-disable in WAIT state, the individual Buck automatically exits WAIT state and enters BUCKx OUTPUT OFF state, if the junction temperature falls below +150°C (T_{SHDN} = 0)
  - If the enable logic of individual Buck is still valid when it enters BUCKx OUTPUT OFF state, the corresponding Buck initiates soft-start. as it goes into BUCKx OUTPUT ON state immediately

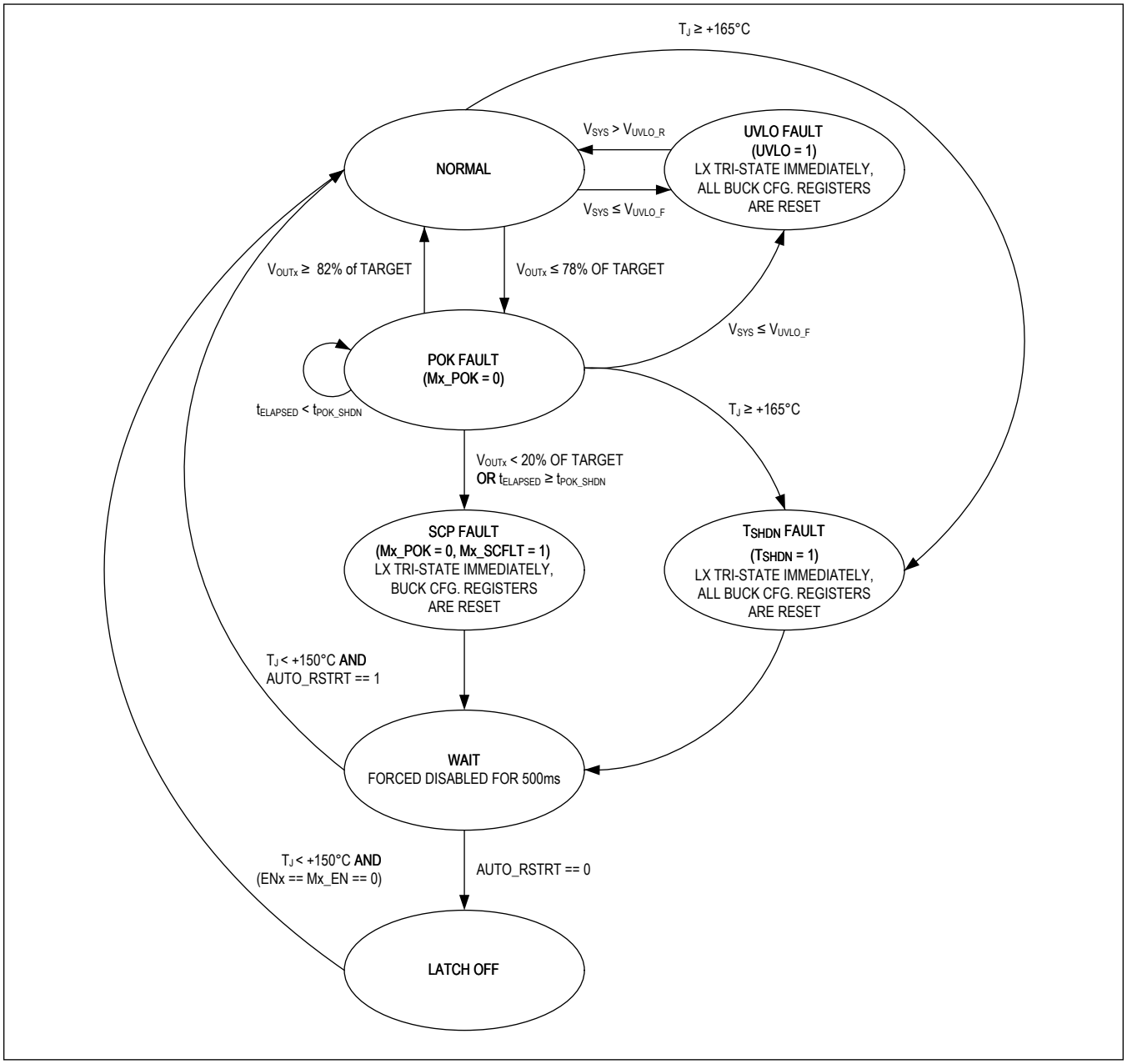


Figure 9. Fault Protection State Diagram

Detailed Description—ADC

The MAX77541 has an 8-bit Successive Approximation Register (SAR) ADC with four multiplexers for supporting the telemetry feature. The four multiplexers are assigned for the V_{SYS} voltage, the output voltage of each Buck converter, and the junction temperature. Each ADC channel is individually controlled through I^2C and has a set of interrupt and interrupt mask bits. When unmasked, the interrupt bit sets whenever the ADC data is ready to be read.

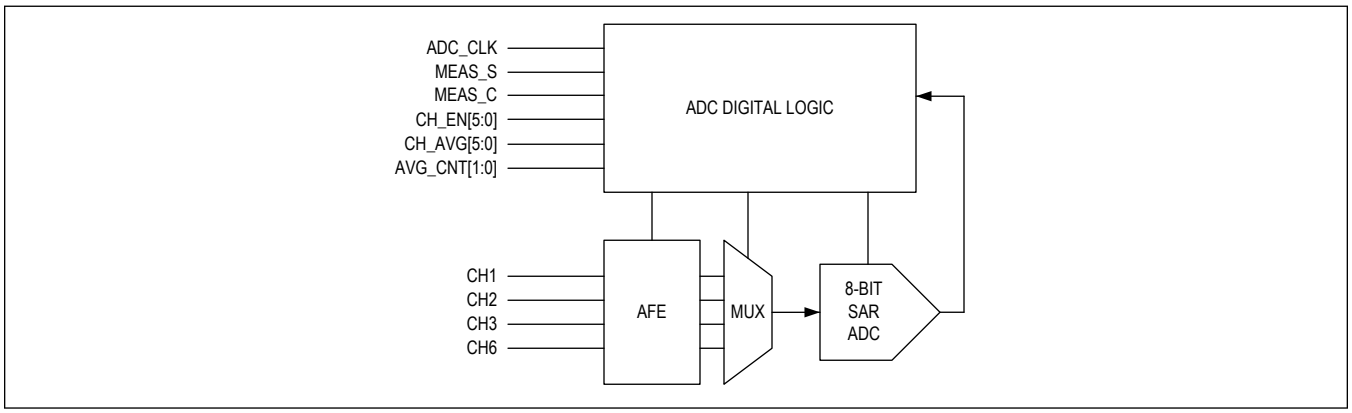


Figure 10. ADC Block Diagram

ADC Enable and Measurement Options

Each individual ADC channel is enabled by setting the CHx_EN bit. The ADC starts sampling the data about 20µs after the MEAS_S bit is set (single measurement). Once the sampling is completed, it takes about 10µs of conversion time to upload the the read-back data into its corresponding data register (ADC_DATAx). In case more than one channel is enabled, the ADC engine measures all enabled channels one by one and uploads the read-back data to the ADC_DATAx registers in turn. The AVG_CNT[1:0] bits set the number of readings (2, 4, 8, or 16 points) before the ADC uploads the averaged data into the ADC_DATAx registers.

The ADC also provides continuous reading options by setting the MEAS_C bit. When MEAS_C = 1, the ADC engine reads all enabled channels and upload the data onto the ADC_DATAx registers every second. While continuous measurement is enabled (MEAS_C = 1), the MEA_S bit is ignored.

When unmasked, an interrupt (ADC_CHx_I) is triggered whenever the new data is uploaded into the corresponding data register. This is to indicate to the host processor that the data is ready to be read.

SYS Voltage Measurement

The supply voltage at the SYS node (V_{SYS}) can be monitored using the ADC CH1. The measurement range is from 0V to 6.375V with 25mV of LSB. The sampling time for the input voltage measurement is about 10µs. See the *Register Map* for the conversion formula between the read-back code and the measured SYS voltage.

Output Voltage Measurement

The MAX77541 is also capable of measuring DC output voltage of each switching phase. Data codes in the ADC_DATA2 and the ADC_DATA3 registers represent the measured output voltages of Phase1 and Phase2 respectively. In dual-phase configuration, it is redundant to measure the output voltages of slave phase if the output voltage of master phase is already measured. The sampling time for the output voltage measurement is about 10µs. See the *Register Map* for the conversion formula between the read-back code and the measured output voltage.

Junction Temperature Measurement

The ADC CH6 is dedicated for measuring the junction temperature of the device. It takes about 1ms to complete sampling the junction temperature. This allows the host processor to optimize its power consumption for reliable operation. See the *Register Map* for the conversion formula between the read-back code and the measured junction temperature.

Detailed Description—I²C Serial Interface

The MAX77541 features a revision 3.0 I²C-compatible, 2-wire serial interface consisting of a serial clock line (SCL) and a bidirectional serial data line (SDA). The MAX77541 is a slave-only device that relies on an external bus master to generate the SCL clock. The SCL clock rates from 0Hz to 3.4MHz are supported. As I²C is an open-drain bus, the SCL and the SDA require external pullup resistors.

Slave Address

The device's I²C communication controller implements 7-bit slave addressing. An I²C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The MAX77541 supports four slave addresses which are selected by R_{CFG} (See the *Device Configuration (CFG)* section). All slave addresses not mentioned in are not acknowledged. The device uses 8-bit registers with 8-bit register addressing. They support standard communication protocols:

- Writing to a single register
- Writing to multiple sequential registers with an automatically incrementing data pointer
- Reading from a single register
- Reading from multiple sequential registers with an automatically incrementing data pointer.

For additional information about I²C protocols, refer to the I²C specification.

Register Map

MAX77541 WLP Package

ADDRESS	NAME	MSB							LSB
GLOBAL CONFIGURATION 1									
0x00	INT_SRC[7:0]	RESERVED[4:0]					–	BUCK_I	TOPSYS_I
0x01	INT_SRC_MSK[7:0]	RESERVED[4:0]					–	BUCK_M	TOPSYS_M
0x02	TOPSYS_INT[7:0]	RESERVED[1:0]		EXT_FREQ_DET_I	RSVD_TOPSYS_INT_4	UVLO_I	TSHDN_I	TJ_140C_I	TJ_120C_I
0x03	TOPSYS_MSK[7:0]	RESERVED[1:0]		EXT_FREQ_DET_M	RSVD_TOPSYS_MSK_4	UVLO_M	TSHDN_M	TJ_140C_M	TJ_120C_M
0x04	TOPSYS_STAT[7:0]	RESERVED[1:0]		EXT_FREQ_DET	RSVD_TOPSYS_STAT_4	UVLO	TSHDN	TJ_140C	TJ_120C
0x06	DEVICE_CFG1[7:0]	RESERVED[2:0]			SEL1_LATCH[4:0]				
0x07	DEVICE_CFG2[7:0]	RESERVED[2:0]			SEL2_LATCH[4:0]				
0x08	DEVICE_CFG3[7:0]	RESERVED[2:0]			CFG_LATCH[4:0]				
0x09	TOPSYS_CFG[7:0]	RESERVED[3:0]				AUTO_RSTRT	MASK_MODE	RESERVED	RSVD_TOPSYS_CFG_0
0x0A	PROT_CFG[7:0]	RESERVED[1:0]		UVLO_F[2:0]			EN_FTMON	POK_TO[1:0]	
0x0B	EN_CTRL[7:0]	RESERVED[1:0]		M2_LPM	M1_LPM	RESERVED[1:0]		M2_EN	M1_EN
GLOBAL CONFIGURATION 2									
0x11	GLB_CFG1[7:0]	RESERVED[1:0]		SSTOP_SR[2:0]			SSTRT_SR[2:0]		
BUCK1 CONFIGURATION									
0x20	BUCK_INT[7:0]	RESERVED[1:0]		M2_SCFLT_I	M1_SCFLT_I	RESERVED[1:0]		M2_POKFLT_I	M1_POKFLT_I
0x21	BUCK_MSK[7:0]	RESERVED[1:0]		M2_SCFLT_M	M1_SCFLT_M	RESERVED[1:0]		M2_POKFLT_M	M1_POKFLT_M
0x22	BUCK_STAT[7:0]	RESERVED[1:0]		M2_SCFLT	M1_SCFLT	RESERVED[1:0]		M2_POK	M1_POK
0x23	M1_VOUT[7:0]	M1_VOUT[7:0]							
0x25	M1_CFG1[7:0]	M1_RNG[1:0]		M1_RD_SR[2:0]			M1_RU_SR[2:0]		
0x26	M1_CFG2[7:0]	M1_SS_ENV[1:0]		M1_SS_FREQ[1:0]		M1_SSM_PAT[1:0]		M1_FSREN	M1_FPWM
0x27	M1_CFG3[7:0]	M1_ADIS100	M1_ADIS7	M1_REFRESH	M1_FTRAK	M1_FREQ[1:0]		M1_ILIM[1:0]	
BUCK2 CONFIGURATION									
0x33	M2_VOUT[7:0]	M2_VOUT[7:0]							
0x35	M2_CFG1[7:0]	M2_RNG[1:0]		M2_RD_SR[2:0]			M2_RU_SR[2:0]		
0x36	M2_CFG2[7:0]	M2_SS_ENV[1:0]		M2_SS_FREQ[1:0]		M2_SSM_PAT[1:0]		M2_FSREN	M2_FPWM

ADDRESS	NAME	MSB							LSB
0x37	M2_CFG3[7:0]	M2_ADIS100	M2_ADIS7	M2_REFRESH	M2_FTRAK	M2_FREQ[1:0]		M2_ILIM[1:0]	
ADC CONFIGURATION									
0x70	ADC_INT[7:0]	–	–	ADC_CH6_I	–	–	ADC_CH3_I	ADC_CH2_I	ADC_CH1_I
0x71	ADC_MSK[7:0]	–	–	ADC_CH6_M	–	–	ADC_CH3_M	ADC_CH2_M	ADC_CH1_M
0x72	ADC_DATA_CH1[7:0]	ADC_DATA1[7:0]							
0x73	ADC_DATA_CH2[7:0]	ADC_DATA2[7:0]							
0x74	ADC_DATA_CH3[7:0]	ADC_DATA3[7:0]							
0x77	ADC_DATA_CH6[7:0]	ADC_DATA6[7:0]							
0x7A	ADC_CFG1[7:0]	–	–	CH6_EN	–	–	CH3_EN	CH2_EN	CH1_EN
0x7B	ADC_CFG2[7:0]	–	–	CH6_AVG	–	–	CH3_AVG	CH2_AVG	CH1_AVG
0x7C	ADC_CFG3[7:0]	RESERVED[1:0]		–	–	AVG_CNT[1:0]		MEAS_C	MEAS_S

Register Details

INT_SRC (0x00)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					–	BUCK_I	TOPSYS_I
Reset	0x0					–	0x0	0x0
Access Type	Read Only					–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:3	Reserved. Returns '0'	
BUCK_I	1	Buck Interrupt Source	0x0 = Interrupt event in Buck has not been detected 0x1 = Interrupt event in Buck has been detected
TOPSYS_I	0	Top-Level Interrupt Source	0x0 = Interrupt event in TOPSYS has not been detected 0x1 = Interrupt event in TOPSYS has been detected

INT_SRC_MSK (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					–	BUCK_M	TOPSYS_M
Reset	0x1F					–	0x1	0x0
Access Type	Write, Read					–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:3	Reserved. Returns 1	
BUCK_M	1	Buck Interrupt Source Mask	0x0 = Enable BUCK_I 0x1 = Mask BUCK_I

BITFIELD	BITS	DESCRIPTION	DECODE
TOPSYS_M	0	Top-Level Interrupt Source Mask	0x0 = Enable TOPSYS_I 0x1 = Mask TOPSYS_I

TOPSYS_INT (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		EXT_FREQ_DET_I	RSVD_TOPSYS_INT_4	UVLO_I	TSHDN_I	TJ_140C_I	TJ_120C_I
Reset	0x0		0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
EXT_FREQ_DET_I	5	External Clock Frequency Detection interrupt	0x0 = Valid external frequency has not been detected at one of FPWMx inputs 0x1 = Valid external frequency has been detected at one of FPWMx inputs
RSVD_TOPSYS_INT_4	4	Reserved. Returns 0	
UVLO_I	3	SYS Under-voltage Lock-out Interrupt	0x0 = Input voltage (V_{SYS}) has not dropped below UVLO threshold 0x1 = Input voltage (V_{SYS}) has dropped below UVLO threshold
TSHDN_I	2	Thermal Shutdown Interrupt	0x0 = Junction temperature has not risen above T_{SHDN} threshold (T_J < +165°C) 0x1 = Junction temperature has risen above T_{SHDN} threshold (T_J ≥ +165°C)
TJ_140C_I	1	Thermal Warning2 Interrupt	0x0 = Junction temperature has not risen above +140°C 0x1 = Junction temperature has risen above +140°C
TJ_120C_I	0	Thermal Warning1 Interrupt	0x0 = Junction temperature has not risen above +120°C 0x1 = Junction temperature has risen above +120°C

TOPSYS_MSK (0x03)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		EXT_FREQ_DET_M	RSVD_TOPSYS_MSK_4	UVLO_M	TSHDN_M	TJ_140C_M	TJ_120C_M
Reset	0x3		0x1	0x1	0x0	0x1	0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 1	
EXT_FREQ_DET_M	5	External Clock Frequency Detection Interrupt Mask	0x0 = Enable EXT_FREQ_DET_I 0x1 = Mask EXT_FREQ_DET_I

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD_TOPSYS_MSK_4	4	Reserved. Returns 1	
UVLO_M	3	SYS Undervoltage Lock-Out Interrupt Mask	0x0 = Enable UVLO_I 0x1 = Mask UVLO_I
TSHDN_M	2	Thermal Shutdown Interrupt Mask	0x0 = Enable TSHDN_I 0x1 = Mask TSHDN_I
TJ_140C_M	1	Thermal Warning2 Interrupt Mask	0x0 = Enable TJ_140C_I 0x1 = Mask TJ_140C_I
TJ_120C_M	0	Thermal Warning1 Interrupt Mask	0x0 = Enable TJ_120C_I 0x1 = Mask TJ_120C_I

TOPSYS_STAT (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		EXT_FREQ_DET	RSVD_TOPSYS_STAT_4	UVLO	TSHDN	TJ_140C	TJ_120C
Reset	0x0		0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
EXT_FREQ_DET	5	External Clock Frequency Detection Status	0x0 = Valid external frequency is not detected 0x1 = Valid external frequency is detected
RSVD_TOPSYS_STAT_4	4	Reserved. Returns 0	
UVLO	3	SYS Undervoltage Lock-Out Status	0x0 = $V_{SYS} \geq V_{UVLO\_R}$ 0x1 = $V_{SYS} \leq V_{UVLO\_F}$
TSHDN	2	Thermal Shutdown Status	0x0 = $T_J \leq 150°C$ 0x1 = $T_J \geq 165°C$
TJ_140C	1	Thermal Warning2 Status	0x0 = $T_J \leq 125°C$ 0x1 = $T_J \geq 140°C$
TJ_120C	0	Thermal Warning1 Status	0x0 = $T_J \leq 105°C$ 0x1 = $T_J \geq 120°C$

DEVICE_CFG1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL1_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION
RESERVED	7:5	Reserved. Returns 0
SEL1_LATCH	4:0	SEL1 Latched Code

DEVICE_CFG2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL2_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION
RESERVED	7:5	Reserved. Returns 0
SEL2_LATCH	4:0	SEL2 Latched Code

DEVICE_CFG3 (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			CFG_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION
RESERVED	7:5	Reserved. Returns 0
CFG_LATCH	4:0	CFG Latched Code

TOPSYS_CFG (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[3:0]				AUTO_RSTRT	MASK_MODE	RESERVED	RSVD_TOPSYS_CFG_0
Reset	0x0				0x0	0x0	0x0	0x0
Access Type	Write, Read				Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:4	Reserved. Returns 0	
AUTO_RSTRT	3	Auto Restart from POK Fault-Off, SCP, and T_{SHDN}	0x0 = Disable (Mx_EN bit and/or ENx signals need to be toggled to exit 'LATCH-OFF' state) 0x1 = Enable (Allow auto-restart after 500ms of forced OFF time)
MASK_MODE	2	Interrupt Mask Mode Setting	0x0 = Interrupt signal is gated after the corresponding interrupt bit when masked 0x1 = Interrupt signal is gated before the corresponding interrupt bit when masked
RESERVED	1	Reserved. Returns '0'	
RSVD_TOPSYS_CFG_0	0	Reserved. Returns '0'	

PROT_CFG (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		UVLO_F[2:0]			EN_FTMON	POK_TO[1:0]	
Reset	0x0		0x0			0x0	0x0	
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
UVLO_F	5:3	V_{SYS} UVLO Falling Threshold Note that UVLO falling threshold must be lower than UVLO rising threshold (typ 2.2V) set by an OTP.	0x0 = 2.00V 0x1 = 2.00V 0x2 = 2.00V 0x3 = 2.05V 0x4 = 2.10V 0x5 = 2.15V 0x6 = 2.20V 0x7 = 2.25V
EN_FTMON	2	Forced Junction Temperature Monitor	0x0 = Monitor junction temperature only when one or more outputs is/are enabled 0x1 = Monitor junction temperature even when all the outputs are disabled
POK_TO	1:0	Power-OK Fault Time-Out Setting	0x0 = Disable 0x1 = 1ms 0x2 = 5ms 0x3 = 10ms

EN_CTRL (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_LPM	M1_LPM	RESERVED[1:0]		M2_EN	M1_EN
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
M2_LPM	5	Buck Master2 Low-Power Mode Control	0x0 = Disable 0x1 = Enable
M1_LPM	4	Buck Master1 Low-Power Mode Control	0x0 = Disable 0x1 = Enable
RESERVED	3:2	Reserved. Returns 0	
M2_EN	1	Buck Master2 Enable Control	0x0 = Disable 0x1 = Enable (‘OR’ Logic with EN2 Input)
M1_EN	0	Buck Master1 Enable Control	0x0 = Disable 0x1 = Enable (‘OR’ Logic with EN1 Input)

GLB_CFG1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		SSTOP_SR[2:0]			SSTRT_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
SSTOP_SR	5:3	Global Soft-Stop Slew-Rate Control	0x0 = -0.15mV/µs 0x1 = -0.625mV/µs 0x2 = -1.25mV/µs 0x3 = -2.5mV/µs 0x4 = -5.0mV/µs 0x5 = -10mV/µs 0x6 = -20mV/µs 0x7 = -40mV/µs
SSTRT_SR	2:0	Global Soft-Start Slew-Rate Control	0x0 = 0.15mV/µs 0x1 = 0.625mV/µs 0x2 = 1.25mV/µs 0x3 = 2.5mV/µs 0x4 = 5.0mV/µs 0x5 = 10mV/µs 0x6 = 20mV/µs 0x7 = 40mV/µs

BUCK_INT (0x20)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SCFLT_I	M1_SCFLT_I	RESERVED[1:0]		M2_POKFLT_I	M1_POKFLT_I
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Clears All		Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
M2_SCFLT_I	5	Buck Master2 Short-Circuit Fault Interrupt	0x0 = Buck Master2 Short-circuit Fault has not been detected 0x1 = Buck Master2 Short-circuit Fault has been detected
M1_SCFLT_I	4	Buck Master1 Short-Circuit Fault Interrupt	0x0 = Buck Master1 Short-circuit Fault has not been detected 0x1 = Buck Master1 Short-circuit Fault has been detected
RESERVED	3:2	Reserved. Returns 0	
M2_POKFLT_I	1	Buck Master2 Power-OK Fault Interrupt	0x0 = Buck Master2 Power-OK Fault has not been detected 0x1 = Buck Master2 Power-OK Fault has been detected

BITFIELD	BITS	DESCRIPTION	DECODE
M1_POKFLT_I	0	Buck Master1 Power-OK Fault Interrupt	0x0 = Buck Master1 Power-OK Fault has not been detected 0x1 = Buck Master1 Power-OK Fault has been detected

BUCK_MSK (0x21)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SCFLT_M	M1_SCFLT_M	RESERVED[1:0]		M2_POKFLT_M	M1_POKFLT_M
Reset	0x3		0x1	0x1	0x3		0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 1	
M2_SCFLT_M	5	Buck Master2 Short-Circuit Fault Interrupt Mask	0x0 = Enable M2_SCFLT_I 0x1 = Mask M2_SCFLT_I
M1_SCFLT_M	4	Buck Master1 Short-Circuit Fault Interrupt Mask	0x0 = Enable M1_SCFLT_I 0x1 = Mask M1_SCFLT_I
RESERVED	3:2	Reserved. Returns 1	
M2_POKFLT_M	1	Buck Master2 Power-OK Fault Interrupt Mask	0x0 = Enable M2_POKFLT_I 0x1 = Mask M2_POKFLT_I
M1_POKFLT_M	0	Buck Master1 Power-OK Fault Interrupt Mask	0x0 = Enable M1_POKFLT_I 0x1 = Mask M1_POKFLT_I

BUCK_STAT (0x22)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SCFLT	M1_SCFLT	RESERVED[1:0]		M2_POK	M1_POK
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Read Only		Read Only	Read Only	Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
M2_SCFLT	5	Buck Master2 Short-Circuit Fault Status	0x0 = Buck Master2 output voltage is higher than its SCP threshold, or Buck Master2 is disabled 0x1 = Buck Master2 output voltage is lower than its SCP threshold
M1_SCFLT	4	Buck Master1 Short-Circuit Fault Status	0x0 = Buck Master1 output voltage is higher than its SCP threshold, or Buck Master1 is disabled 0x1 = Buck Master1 output voltage is lower than its SCP threshold
RESERVED	3:2	Reserved. Returns 0	
M2_POK	1	Buck Master2 Power_OK Status	0x0 = Buck Master2 output voltage is lower than its POK threshold, or Buck Master2 is disabled 0x1 = Buck Master2 output voltage is higher than its POK threshold

BITFIELD	BITS	DESCRIPTION	DECODE
M1_POK	0	Buck Master1 Power-OK Status	0x0 = Buck Master1 output voltage is lower than its POK threshold, or Buck Master1 is disabled 0x1 = Buck Master1 output voltage is higher than its POK threshold

M1_VOUT (0x23)

BIT	7	6	5	4	3	2	1	0
Field	M1_VOUT[7:0]							
Reset	0x46							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
M1_VOUT	7:0	Buck Master1 Output Voltage Control Register	When M1_RNG = 0x0, 0x0 - 0xB3 = (0.3 + 0.005 * M1_VOUT)V, 0xB4 - 0xFF = 1.200V When M1_RNG = 0x1, 0x0 - 0x8B = (1.0 + 0.01 * M1_VOUT)V, 0x8C - 0xFF = 2.40V When M1_RNG = 0x2, 0x0 - 0x9F = (2.0 + 0.02 * M1_VOUT)V, 0xA0 - 0xFF = 5.20V

M1_CFG1 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	M1_RNG[1:0]		M1_RD_SR[2:0]			M1_RU_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
M1_RNG	7:6	Buck Master1 Output Voltage Range Setting, (Register setting must not be changed while the output is enabled)	0x0 = Low-range (0.3V to 1.2V, 5mV Step) 0x1 = Mid-range (1.0V to 2.4V, 10mV Step) 0x2 = High-range (2.0V to 5.2V, 20mV Step) 0x3 = Reserved
M1_RD_SR	5:3	Buck Master1 Ramp-down Slew-rate Setting	0x0 = -0.15mV/µs 0x1 = -0.625mV/µs 0x2 = -1.25mV/µs 0x3 = -2.5mV/µs 0x4 = -5.0mV/µs 0x5 = -10mV/µs 0x6 = -20mV/µs 0x7 = -40mV/µs

BITFIELD	BITS	DESCRIPTION	DECODE
M1_RU_SR	2:0	Buck Master1 Ramp-up Slew-rate Setting	0x0 = 0.15mV/µs 0x1 = 0.625mV/µs 0x2 = 1.25mV/µs 0x3 = 2.5mV/µs 0x4 = 5.0mV/µs 0x5 = 10mV/µs 0x6 = 20mV/µs 0x7 = 40mV/µs

M1_CFG2 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	M1_SS_ENV[1:0]		M1_SS_FREQ[1:0]		M1_SSM_PAT[1:0]		M1_FSREN	M1_FPWM
Reset	0x0		0x0		0x0		0x1	0x0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
M1_SS_ENV	7:6	Buck Master1 Spread Spectrum Envelope Setting	0x0 = Disable 0x1 = ±8% 0x2 = ±12% 0x3 = ±16%
M1_SS_FREQ	5:4	Buck Master1 Spread Spectrum Frequency Setting	0x0 = 1kHz 0x1 = 3kHz 0x2 = 5kHz 0x3 = 7kHz
M1_SSM_PAT	3:2	Buck Master1 Spread Spectrum Pattern Setting	0x0 = Triangular Pattern (0001b to 1111b) 0x1 = Pseudo-Random Polynomial ($x^4 + x + 1$) 0x2 = Pseudo-Random Polynomial ($x^4 + x^3 + 1$) 0x3 = Pseudo-Random Polynomial (Alternating "$x^4 + x + 1$" and "$x^4 + x^3 + 1$" every cycle)
M1_FSREN	1	Buck Master1 Falling Slew-rate Control	0x0 = Disable (Buck does not sink current from C_{OUT} in SKIP or LP-SKIP mode) 0x1 = Enable (Buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT})
M1_FPWM	0	Buck Master1 Forced-PWM Control	0x0 = Disable (Automatic SKIP mode operation under light load condition) 0x1 = Enable (‘OR’ Logic with FPWM1 input)

M1_CFG3 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	M1_ADIS100	M1_ADIS7	M1_REFRESH	M1_FTRAK	M1_FREQ[1:0]		M1_ILIM[1:0]	
Reset	0x1	0x0	0x0	0x0	0x1		0x2	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
M1_ADIS100	7	Buck Master1 100Ω Active Discharge	0x0 = Disable 0x1 = Enable

BITFIELD	BITS	DESCRIPTION	DECODE
M1_ADIS7	6	Buck Master1 7Ω Active Discharge, Note that 7Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M1_FSREN = 0)	0x0 = Disable 0x1 = Enable (Active for 1ms after soft-stop is completed)
M1_REFRESH	5	Buck Master1 Bootstrap Refresh Interval Control	0x0 = 128µs 0x1 = 10µs
M1_FTRAK	4	Buck Master1 Internal Frequency Tracking Control	0x0 = Disable 0x1 = Enable
M1_FREQ	3:2	Buck Master1 Switching Frequency Setting	0x0 = 0.5MHz 0x1 = 1.0MHz 0x2 = 1.6MHz 0x3 = Reserved
M1_ILIM	1:0	Buck Master1 Peak Current Limit Setting	0x0 = 2.2A 0x1 = 3.4A 0x2 = 4.0A 0x3 = 4.6A

M2_VOUT (0x33)

BIT	7	6	5	4	3	2	1	0
Field	M2_VOUT[7:0]							
Reset	0xA0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
M2_VOUT	7:0	Buck Master2 Output Voltage Control Register	When M2_RNG = 0x0, 0x0 - 0xB3 = (0.3 + 0.005 * M2_VOUT)V, 0xB4 - 0xFF = 1.200V When M2_RNG = 0x1, 0x0 - 0x8B = (1.0 + 0.01 * M2_VOUT)V, 0x8C - 0xFF = 2.40V When M2_RNG = 0x2, 0x0 - 0x9F = (2.0 + 0.02 * M2_VOUT)V, 0xA0 - 0xFF = 5.20V

M2_CFG1 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	M2_RNG[1:0]		M2_RD_SR[2:0]			M2_RU_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
M2_RNG	7:6	Buck Master2 Output Voltage Range Setting, (Register setting must not be changed while the output is enabled)	0x0 = Low-range (0.3V to 1.2V, 5mV Step) 0x1 = Mid-range (1.0V to 2.4V, 10mV Step) 0x2 = High-range (2.0V to 5.2V, 20mV Step) 0x3 = Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
M2_RD_SR	5:3	Buck Master2 Ramp-down Slew-rate Setting	0x0 = -0.15mV/µs 0x1 = -0.625mV/µs 0x2 = -1.25mV/µs 0x3 = -2.5mV/µs 0x4 = -5.0mV/µs 0x5 = -10mV/µs 0x6 = -20mV/µs 0x7 = -40mV/µs
M2_RU_SR	2:0	Buck Master2 Ramp-up Slew-rate Setting	0x0 = 0.15mV/µs 0x1 = 0.625mV/µs 0x2 = 1.25mV/µs 0x3 = 2.5mV/µs 0x4 = 5.0mV/µs 0x5 = 10mV/µs 0x6 = 20mV/µs 0x7 = 40mV/µs

M2_CFG2 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	M2_SS_ENV[1:0]		M2_SS_FREQ[1:0]		M2_SSM_PAT[1:0]		M2_FSREN	M2_FPWM
Reset	0x0		0x0		0x0		0x1	0x0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
M2_SS_ENV	7:6	Buck Master2 Spread Spectrum Envelope Setting	0x0 = Disable 0x1 = ±8% 0x2 = ±12% 0x3 = ±16%
M2_SS_FREQ	5:4	Buck Master2 Spread Spectrum Frequency Setting	0x0 = 1kHz 0x1 = 3kHz 0x2 = 5kHz 0x3 = 7kHz
M2_SSM_PAT	3:2	Buck Master2 Spread Spectrum Pattern Setting	0x0 = Triangular Pattern (0001b to 1111b) 0x1 = Pseudo-Random Polynomial ($x^4 + x + 1$) 0x2 = Pseudo-Random Polynomial ($x^4 + x^3 + 1$) 0x3 = Pseudo-Random Polynomial (Alternating "$x^4 + x + 1$" and "$x^4 + x^3 + 1$" every cycle)
M2_FSREN	1	Buck Master2 Falling Slew-rate Control	0x0 = Disable (Buck does not sink current from C_{OUT} in SKIP or LP-SKIP mode) 0x1 = Enable (Buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT})
M2_FPWM	0	Buck Master2 Forced-PWM Control	0x0 = Disable (Automatic SKIP mode operation under light load condition) 0x1 = Enable (‘OR’ Logic with FPWM2 input)

M2_CFG3 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	M2_ADIS100	M2_ADIS7	M2_REFRESH	M2_FTRAK	M2_FREQ[1:0]		M2_ILIM[1:0]	
Reset	0x1	0x0	0x0	0x0	0x1		0x2	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
M2_ADIS100	7	Buck Master2 100Ω Active Discharge	0x0 = Disable 0x1 = Enable
M2_ADIS7	6	Buck Master2 7Ω Active Discharge, Note that 7Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M2_FSREN = 0)	0x0 = Disable 0x1 = Enable (Active for 1ms after soft-stop is completed)
M2_REFRESH	5	Buck Master2 Bootstrap Refresh Interval Control	0x0 = 128µs 0x1 = 10µs
M2_FTRAK	4	Buck Master2 Intrenal Frequency Tracking Control	0x0 = Disable 0x1 = Enable
M2_FREQ	3:2	Buck Master2 Switching Frequency Setting	0x0 = 0.5MHz 0x1 = 1.0MHz 0x2 = 1.6MHz 0x3 = Reserved
M2_ILIM	1:0	Buck Master2 Peak Current Limit Setting	0x0 = 2.2A 0x1 = 3.4A 0x2 = 4.0A 0x3 = 4.6A

ADC_INT (0x70)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ADC_CH6_I	–	–	ADC_CH3_I	ADC_CH2_I	ADC_CH1_I
Reset	–	–	0x0	–	–	0x0	0x0	0x0
Access Type	–	–	Read Clears All	–	–	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_CH6_I	5	ADC Channel6 Interrupt	0x0 = ADC Channel6 data has not updated 0x1 = ADC Channel6 data has updated
ADC_CH3_I	2	ADC Channel3 Interrupt	0x0 = ADC Channel3 data has not updated 0x1 = ADC Channel3 data has updated
ADC_CH2_I	1	ADC Channel2 Interrupt	0x0 = ADC Channel2 data has not updated 0x1 = ADC Channel2 data has updated
ADC_CH1_I	0	ADC Channel1 Interrupt	0x0 = ADC Channel1 data has not updated 0x1 = ADC Channel1 data has updated

ADC_MSK (0x71)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ADC_CH6_M	–	–	ADC_CH3_M	ADC_CH2_M	ADC_CH1_M
Reset	–	–	0x1	–	–	0x1	0x1	0x1
Access Type	–	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_CH6_M	5	ADC Channel6 Interrupt Mask	0x0 = Enable ADC_CH6_I 0x1 = Mask ADC_CH6_I
ADC_CH3_M	2	ADC Channel3 Interrupt Mask	0x0 = Enable ADC_CH3_I 0x1 = Mask ADC_CH3_I
ADC_CH2_M	1	ADC Channel2 Interrupt Mask	0x0 = Enable ADC_CH2_I 0x1 = Mask ADC_CH2_I
ADC_CH1_M	0	ADC Channel1 Interrupt Mask	0x0 = Enable ADC_CH1_I 0x1 = Mask ADC_CH1_I

ADC_DATA_CH1 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA1[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_DATA1	7:0	ADC CH1 (V_{SYS}) Data Readback	0x0 - 0xFF = (0.025 x ADC_DATA1)V

ADC_DATA_CH2 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA2[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_DATA2	7:0	ADC CH2 (V_{OUT1}) Data Readback	When M1_RNG = 0x0, 0x0 - 0xFF = (0.00625 x ADC_DATA2)V When M1_RNG = 0x1, 0x0 - 0xFF = (0.0125 x ADC_DATA2)V When M1_RNG = 0x2, 0x0 - 0xFF = (0.025 x ADC_DATA2)V

ADC_DATA_CH3 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA3[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_DATA3	7:0	ADC CH3 (V_{OUT2}) Data Readback	When M2_RNG = 0x0, 0x0 - 0xFF = (0.00625 x ADC_DATA3)V When M2_RNG = 0x1, 0x0 - 0xFF = (0.0125 x ADC_DATA3)V When M2_RNG = 0x2, 0x0 - 0xFF = (0.025 x ADC_DATA3)V

ADC_DATA_CH6 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	ADC_DATA6[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
ADC_DATA6	7:0	ADC CH6 (Junction Temperature) Data Readback	0x0 - 0xFF = (-273 + 1.725 * ADC_DATA6)°C

ADC_CFG1 (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CH6_EN	–	–	CH3_EN	CH2_EN	CH1_EN
Reset	–	–	0x0	–	–	0x0	0x0	0x0
Access Type	–	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CH6_EN	5	ADC Channel6 Data Readback Control	0x0 = Disable 0x1 = Enable
CH3_EN	2	ADC Channel3 Data Readback Control	0x0 = Disable 0x1 = Enable
CH2_EN	1	ADC Channel2 Data Readback Control	0x0 = Disable 0x1 = Enable
CH1_EN	0	ADC Channel1 Data Readback Control	0x0 = Disable 0x1 = Enable

ADC_CFG2 (0x7B)

BIT	7	6	5	4	3	2	1	0
Field	–	–	CH6_AVG	–	–	CH3_AVG	CH2_AVG	CH1_AVG
Reset	–	–	0x0	–	–	0x0	0x0	0x0
Access Type	–	–	Write, Read	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CH6_AVG	5	ADC Channel6 Data Averaging Control	0x0 = Disable 0x1 = Enable
CH3_AVG	2	ADC Channel3 Data Averaging Control	0x0 = Disable 0x1 = Enable
CH2_AVG	1	ADC Channel2 Data Averaging Control	0x0 = Disable 0x1 = Enable
CH1_AVG	0	ADC Channel1 Data Averaging Control	0x0 = Disable 0x1 = Enable

ADC_CFG3 (0x7C)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		–	–	AVG_CNT[1:0]		MEAS_C	MEAS_S
Reset	0x0		–	–	0x0		0x0	0x0
Access Type	Write, Read		–	–	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns 0	
AVG_CNT	3:2	ADC Averaging Count Setting	0x0 = 2-point 0x1 = 4-point 0x2 = 8-point 0x3 = 16-point
MEAS_C	1	ADC Continuous Measurement Control	0x0 = Disable 0x1 = Enable (Update ADC Readback every second)
MEAS_S	0	ADC Single Measurement Control	0x0 = Disable 0x1 = Enable (This bit is ignored when MEAS_C = 1)

Applications Information—Dual-Phase Configurable Buck Converter

Inductor Selection

An inductor with a saturation current that is greater than or equal to the peak current limit setting (I_{PLIM}) is recommended. The load current requirement (per phase) of the system is also a consideration when choosing the RMS current rating of the inductor. Inductors with lower saturation current and higher DCR ratings tend to be physically small, however higher values of DCR reduce the efficiency. To choose a suitable inductor for the given application, consider the trade-off between the size of the inductor versus the DCR value. It is recommended to choose an inductance such that the inductor's ripple current to the average current ratio is between 30% and 60%. Consider the output voltage range and switching frequency when choosing the inductance. In general, for 1MHz switching frequency, 0.47µH is suitable for low-range outputs and 1.0µH is suitable for mid-range outputs and high range outputs. For other switching frequencies, the inductance may need to be adjusted to account for the inductor current ripple. Lower switching frequencies require higher inductance values. Note that higher inductances slow down the maximum slew rate of the inductor current, and high duty cycles (V_{IN} close to V_{OUT}) coupled with large inductance can slow down the load transient response.

Table 11. Recommended Inductors

MANUFACTURER P/N	INDUCTANCE (µH)	TYPICAL DCR (mΩ)	TYPICAL I_{SAT} (A)	TYPICAL I_{TEMP} (A)	DIMENSION (L x W x H) (mm)
GLULMR4701A	0.47 ±20%	17	4.8	5.6	2.5 x 2.0 x 1.2
DFE252012F-R47M	0.47 ±20%	23	6.7	4.9	2.5 x 2.0 x 1.2
DFE252012F-1R0M	1.0 ±20%	40	4.7	3.3	2.5 x 2.0 x 1.2
HTEL25201B-R47MSR	0.47 ±20%	11.0	7.4	6.7	2.5 x 2.0 x 1.2
HTEL25201B-1R0MSR	1.0 ±20%	18.0	5.8	5.7	2.5 x 2.0 x 1.2
HTEP25201T-1R0MSR	1.0 ±20%	18.0	5.5	5.7	2.5 x 2.0 x 1.0

For the dual-phase configuration, each phase needs its own inductor with the same inductance value (do not short the LX nodes of two phases together on the PCB). See the *Phase Configuration* section for more information regarding different phase configurations.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or the input power source and reduces switching noise in the device. The impedance of the C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor (C_{OUT}) is required to keep the output voltage ripple small and to ensure regulation loop stability. The C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. The recommended minimum effective output capacitance per phase is shown in Table 12.

Table 12. Recommended Minimum Effective Output Capacitance

V_{OUT} RANGE	SWITCHING FREQUENCY	MINIMUM EFFECTIVE C_{OUT}*
Low (0.3V to 1.2V)	1MHz	83µF
Mid (1.0V to 2.4V)	1MHz	52µF
High (2.0V to 5.2V)	1MHz	32µF
*Required minimum $C_{OUT(EFF)}$ is inversely proportional to the switching frequency setting. For example, a Buck output using Mx_RNG = 0x0 and 1MHz switching frequency requires 42µF of minimum effective output capacitance. Changing the switching frequency to 1.6MHz decreases the effective output capacitance requirement to 52µF (= 83µF / 1.6).		

The effective C_{OUT} is the actual capacitance value seen by the Buck output during operation. The nominal capacitance

(C_{OUT}) needs to be selected carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias. Refer to *Tutorial 5527* for more information. Larger values of the C_{OUT} (above the required minimum effective) improve load transient performance, but increase the input inrush currents during startup. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple in continuous conduction mode. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple specifications.

General PCB Layout Guidelines

- The power components should be placed first and then small analog control signals
- It is important to always have a ground layer next to the power stage layer because a solid ground layer provides uninterrupted ground return path between the input and the output caps during switch on-time (a solid plane minimizes inductance to the absolute minimum and is also a very good thermal conductor that can act as a heat sink)
- It is recommended to have thick copper for the external high current power layers to minimize the PCB conduction loss and thermal impedance
- The power stage loop that is made by the input capacitor (C_{IN}), the LX trace, the inductor (L), and the output capacitor (C_{OUT}) coming back to the PGNDx bumps should be minimized for EMC considerations
- The input capacitors (C_{IN}) should be located close to the input bumps of each phase
- Bypass capacitors for the V_L, the V_{DD}, and the BSTx pins should be placed as close as possible
- Analog ground (AGND) and power ground (PGND) bumps should be directly connected to the ground plane separately, in order to avoid common impedance ground
- It is recommended to avoid a direct connection between the SYS and its AGND traces to the nearest IN and the PGND traces
- The output voltage sensing trace should not intersect the power stage (the loop made by the input capacitor, the LX trace, the inductor, the output capacitor, and the PGND)
- It is important to have impedance matching between phases for stable operation in multi-phase configuration (the output PCB trace of each phase should be as symmetric as possible)
- For multi-phase configurations, the output voltage sensing bumps for the master phase should be connected to the middle point of the output phases

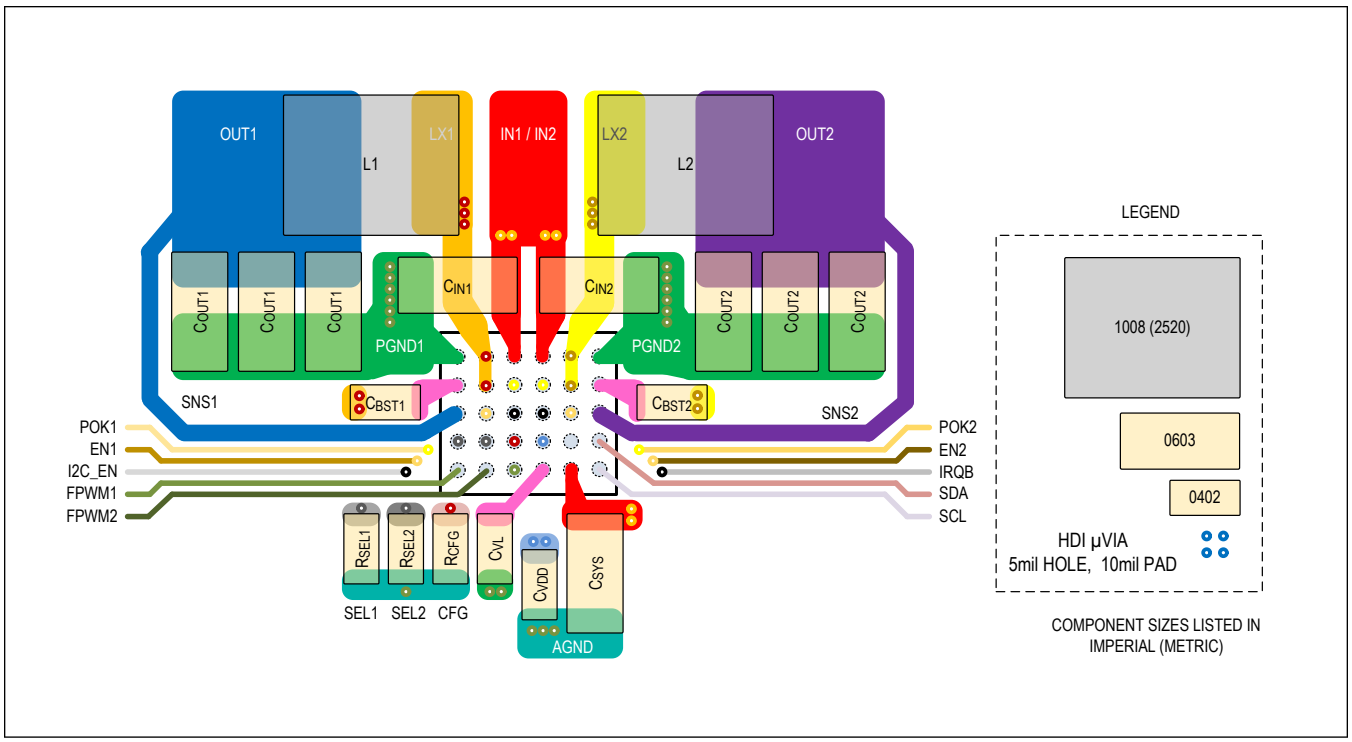


Figure 11. PCB Layout Example—WLP

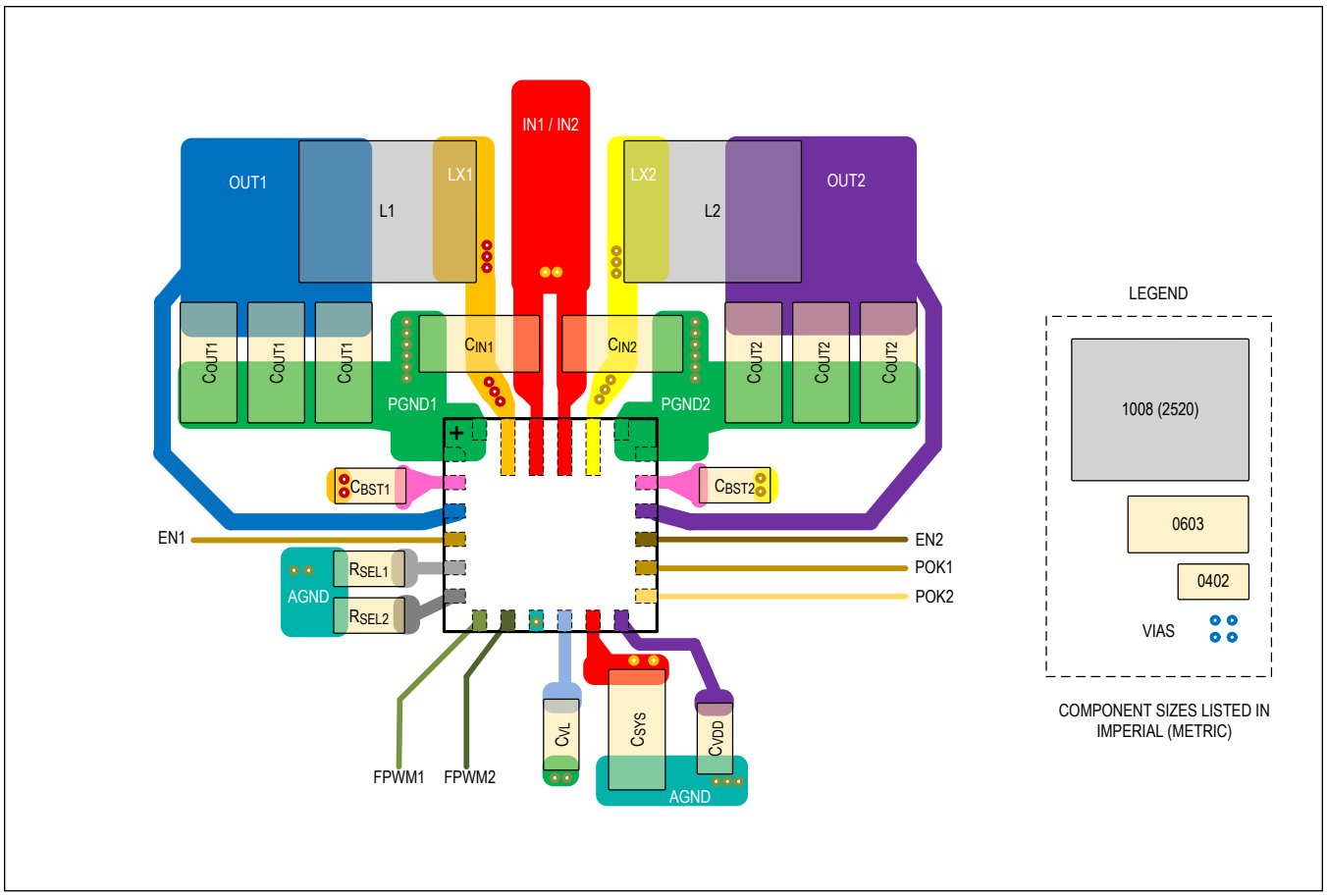
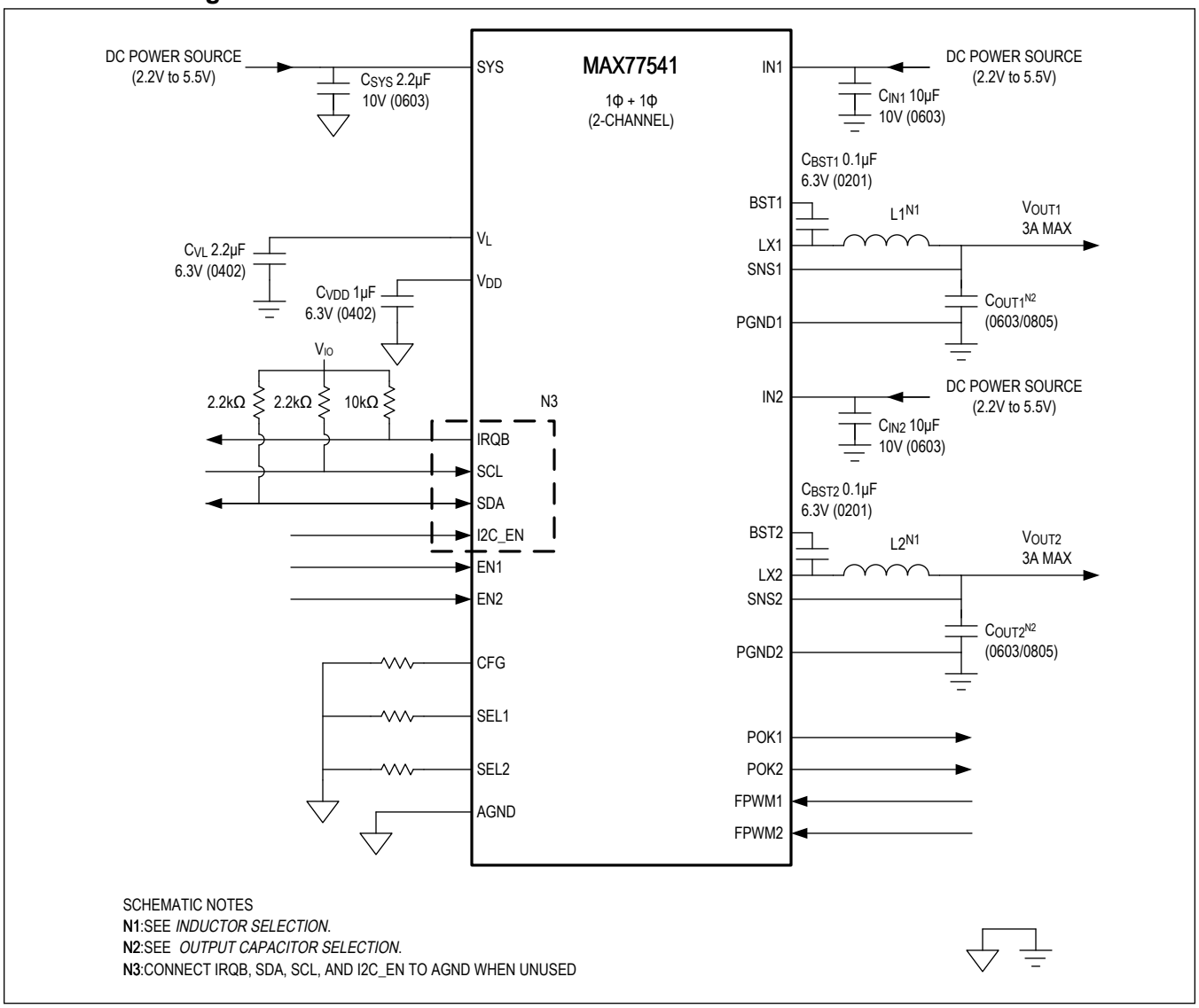


Figure 12. PCB Layout Example—FC2QFN

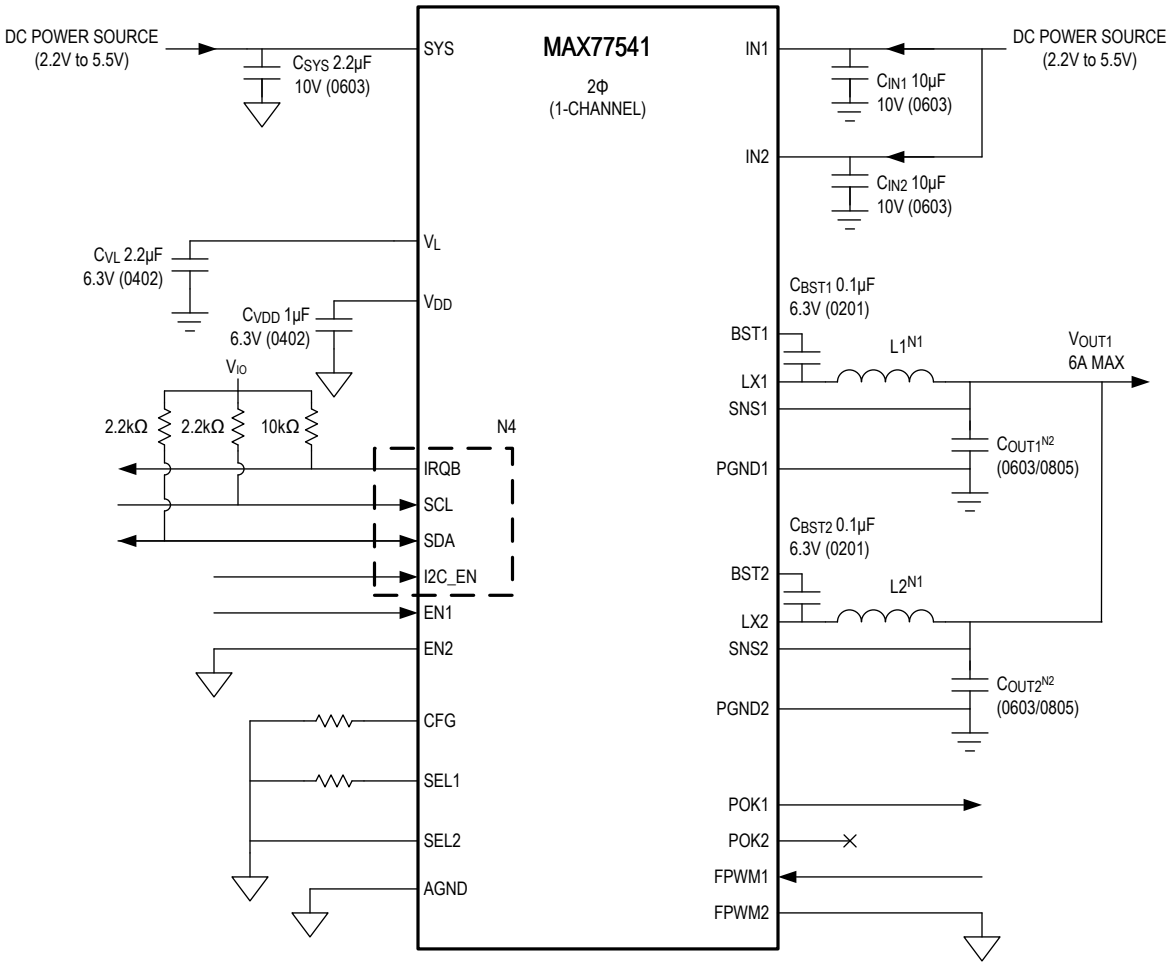
Typical Application Circuits

1+1 Phase Configuration—WLP



Typical Application Circuits (continued)

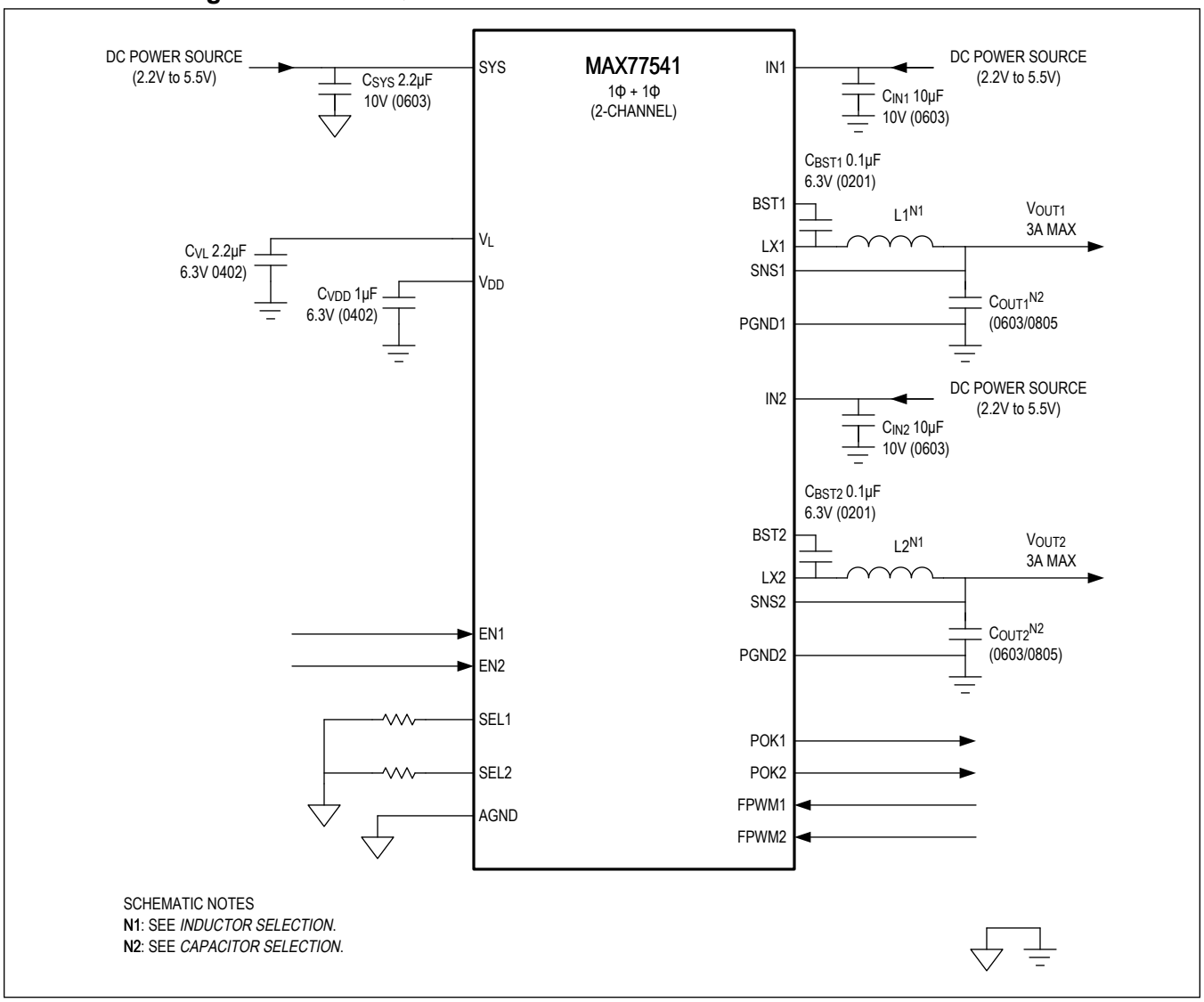
Dual-Phase Configuration—WLP



SCHEMATIC NOTES
N1:SEE *INDUCTOR SELECTION.*
N2:SEE *OUTPUT CAPACITOR SELECTION.*
N3: EN2, POK2, FPWM2 ARE ALL SHOWN AS 'NO CONNECT' BECAUSE THEY ARE UNUSED IN 2-PHASE CONFIGURATION.
N4:CONNECT IRQB, SDA, SCL, AND I2C_EN TO AGND WHEN UNUSED

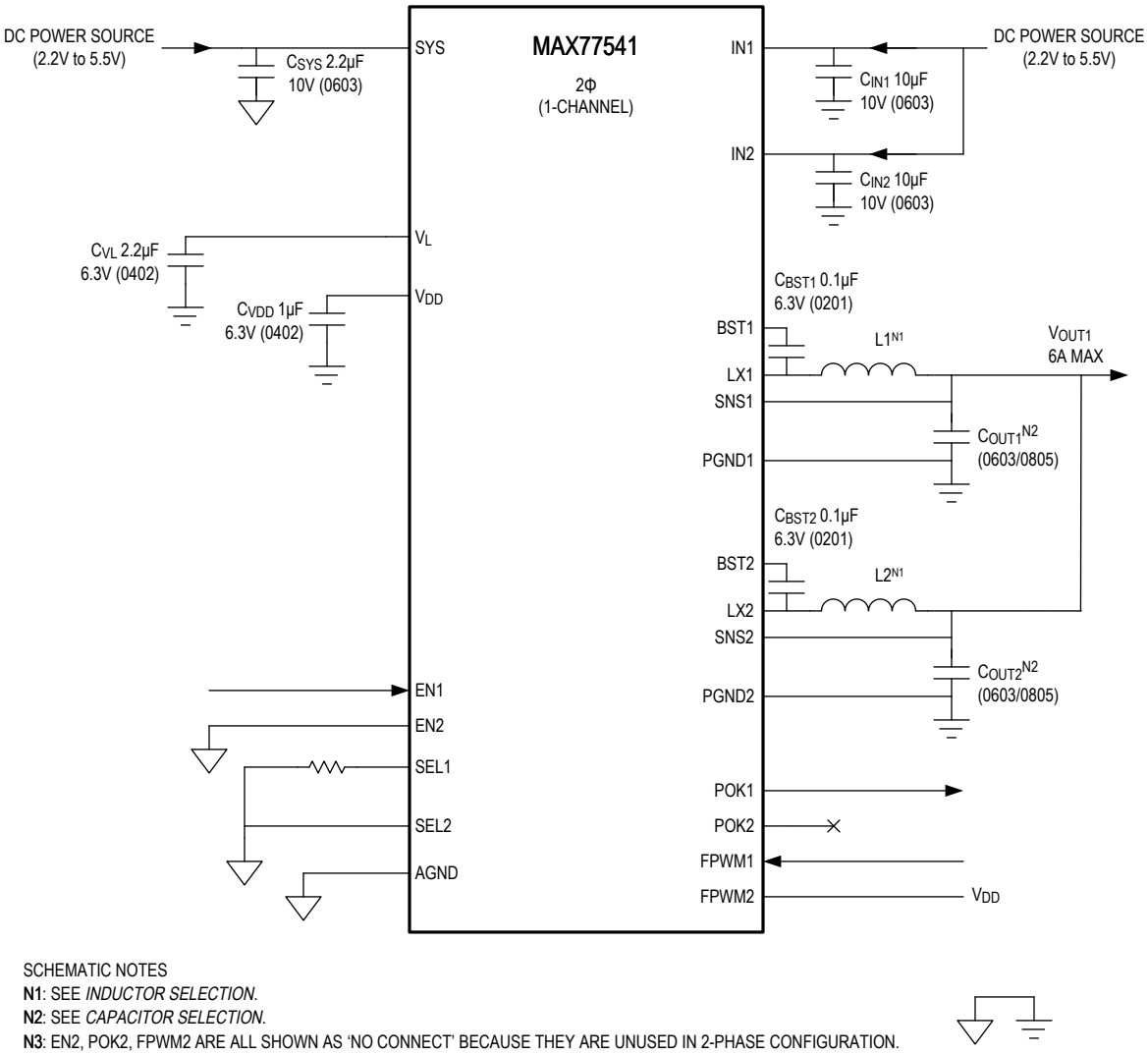
Typical Application Circuits (continued)

1+1 Phase Configuration—FC2QFN



Typical Application Circuits (continued)

Dual-Phase Configuration—FC2QFN



SCHEMATIC NOTES
N1: SEE *INDUCTOR SELECTION.*
N2: SEE *CAPACITOR SELECTION.*
N3: EN2, POK2, FPWM2 ARE ALL SHOWN AS 'NO CONNECT' BECAUSE THEY ARE UNUSED IN 2-PHASE CONFIGURATION.

Ordering Information

PART NUMBER	FACTORY OPTION	PIN-PACKAGE
MAX77541AAWV+T	A	30 WLP
MAX77541AAFG+T	A	24 FC2QFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/21	Initial release	—
1	5/22	Updated *General Description, Absolute Maximum Ratings, Package Information, Electrical Characteristics—Top-Level, Electrical Characteristics—Dual-Phase Configurable Buck Converter, Electrical Characteristics—I^2C Serial Interface, Typical Operating Characteristics, Bump Configuration, Undervoltage Lock-Out (UVLO), Thermal Warnings and Thermal Shutdown (T_{SHDN}), Register Reset Condition, FC2QFN Default Options, Output Voltage Setting, Bootstrap Refresh, Spread-Spectrum Modulation, Register Map, Inductor Selection, General PCB Layout Guidelines, Typical Application Circuits,* and *Ordering Information*	1, 6–15, 21, 23–25, 27, 29, 35, 37, 38, 45, 46, 47, 49, 54, 57, 61, 63–68