Click **here** to ask an associate for production status of specific part numbers.

MAX22500E/MAX22501E

100Mbps Half-Duplex RS-485/RS-422 Transceivers for Long Cables

General Description

The MAX22500E/MAX22501E half-duplex ESD-protected RS-485/RS-422 transceivers are optimized for high-speed (up to 100Mbps) communication over long cables.These transceivers feature integrated hot-swap protection and a fail-safe receiver, ensuring a logic-high on the receiver output when input signals are shorted or open for longer than 10μs (typ).

The MAX22500E features integrated preemphasis circuitry that extends the distance and increases the data rate of reliable communication by reducing inter-symbol interference (ISI) caused by long cables. The MAX22500E features a flexible logic interface down to 1.6V.

The MAX22501E operates without preemphasis and is powered from a 3V to 5.5V supply.

The MAX22500E is available in a 10-pin TDFN-EP package. The MAX22501E is available in a 8-pin TDFN-EP package and an 8-pin μMAX package. Both transceivers operate over the -40°C to +125°C ambient temperature range.

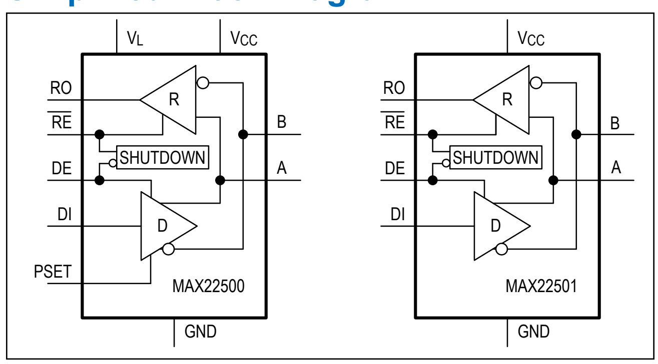
Applications

- Motion Control
- Encoder Interfaces
- Field Bus Networks
- Industrial Control Systems
- Backplane Busses

Benefits and Features

- High-Speed Operation Over Long Distances
  - Up to 100Mbps Data Rate
  - Integrated Preemphasis Extends Cable Length (MAX22500E)
  - High Receiver Sensitivity
  - Wide Receiver Bandwidth
  - Symmetrical Receiver Thresholds
- Integrated Protection Increases Robustness
  - -15V to +15V Common Mode Range
  - ±15kV ESD Protection (Human Body Model)
  - ±7kV IEC 61000-4-2 Air-Gap ESD Protection
  - ±6kV IEC 61000-4-2 Contact Discharge ESD Protection
  - Withstands up to ±4kV EFT
  - Driver Outputs are Short-Circuit Protected
- Flexibility for Many Different Applications
  - 3V to 5.5V Supply Range
  - Low Voltage Logic Supply Down to 1.6V (MAX22500E)
  - Low 5μA (max) Shutdown Current
  - Available in 8-pin or 10-pin TDFN Package and an 8-pin μMAX Package
  - -40°C to +125°C Operating Temperature Range

Simplified Block Diagram



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Ordering Information appears at end of data sheet.

19-100073; Rev 3; 12/21

Absolute Maximum Ratings

V_{CC} .... -0.3V to +6V
$\overline{RE}$, DE, DI, V_L .... -0.3V to +6V
RO (MAX22500E only)................................-0.3V to (V_L + 0.3V)
RO (MAX22501E only)..............................-0.3V to (V_{CC} + 0.3V)
PSET ....-0.3V to (V_{CC}+0.3V)
A, B...-15V to +15V
Short-Circuit Duration (RO, A, B) to GND ....
Continuous Power Dissipation (T_A = +70°C) (8-Pin TDFN (derate 24.4mW/°C above +70°C))... 1951mW
Continuous Power Dissipation (T_A = +70°C) (10-Pin TDFN (derate 24.4mW/°C above +70°C))...............................1951mW
Continuous Power Dissipation (T_A = +70°C) (8-pin μMAX)(derate at 4.8mW°C above +70°C) 387.8mW
Operating Temperature Range ....-40ºC to +125ºC
Junction Temperature ....+150ºC
Storage Temperature Range ....-65ºC to +150ºC
Lead Temperature (Soldering 10sec) ....+300ºC
Reflow Temperature ....+270ºC

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TDFN8

Package Code	T833-2
Outline Number	21-0137
Land Pattern Number	90-0059
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

TDFN10

Package Code	T1033-2
Outline Number	21-0137
Land Pattern Number	90-0061
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9°C/W

8-pin µMAX

Package Code	U8+1
Outline Number	21-0136
Land Pattern Number	90-0092
THERMAL RESISTANCE, SINGLE-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	221°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	42°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	206°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	42°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC} (MAX22500E only), $V_L \le V_{CC}$, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (*Note 1*, *Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Supply Voltage	V_{CC}	MAX22500E	Preemphasis disabled	3.0		5.5	V
			Preemphasis enabled	4.5	5	5.5	
		MAX22501E		3.0		5.5	
Supply Current	I_{CC}	DE = high, $\overline{RE}$= low, no load	MAX22500E		12.7	16.5	mA
			MAX22501E		4	5.6	
Shutdown Supply Current	I_{SHDN}	DE = low, $\overline{RE}$= high				5	µA
Logic Supply Voltage	V_L	MAX22500E only		1.6		V_{CC}	V
Logic Supply Current	I_L	MAX22500E only, no load on RO			16.4	23	µA
DRIVER							
Differential Driver Output	V_{OD}	Figure 1, Figure 2	R_L = 54Ω	1.5			V
			R_L = 100Ω	2.0			
Differential Driver Preemphasis Ratio	D_{PRE}	MAX22500E only, preemphasis enabled, 4.5V ≤ V_{CC} ≤ 5.5V (Note 3)	R_L= 54Ω	1.33	1.37	1.41	V/V
			R_L= 100Ω	1.33	1.37	1.41	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	R_L = 54Ω, Figure 1 (Note 4)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	R_L = 54Ω, Normal mode and preemphasis, Figure 1			$V_{CC}/2$	3	V

Electrical Characteristics (continued)

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC} (MAX22500E only), $V_L \le V_{CC}$, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1, Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Change In Magnitude of Common-Mode Voltage	ΔV_{OC}	R_L = 100Ω or 54Ω, Figure 1 (Note 4)				0.2	V
Single-Ended Driver Output High	V_{OH}	A or B output, I_{OUT} = -20mA		2.2			V
Single-Ended Driver Output Low	V_{OL}	A or B output, I_{OUT} = +20mA				0.8	V
Differential Output Capacitance	C_{OD}	DE = $\overline{RE}$= high, f = 4MHz			50		pF
Driver Short-Circuit Output Current	$\lvert I_{OST} \rvert$	$-15V \le V_{OUT} \le +15V$				250	mA
RECEIVER							
Input Current (A and B)	$I_{A,B}$	DE = GND, V_{CC} = GND, +3.6V or 5.5V	V_{IN} = +12V			+1350	µA
			V_{IN} = -7V	-1100			
Differential Input Capacitance	$C_{A,B}$	Between A and B, DE = GND, f = 2MHz			50		pF
Common Mode Voltage Range	V_{CM}			-15		+15	V
Receiver Differential Threshold High	V_{TH_H}	$-15V \le V_{CM} \le +15V$		+50		+200	mV
Receiver Differential Threshold Low	V_{TH_L}	$-15V \le V_{CM} \le +15V$		-200		-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V, time from last transition is less than t_{D_FS}			250		mV
Differential Input Fail-Safe Level	V_{TH_FS}	$-15V \le V_{CM} \le +15V$		-50		+50	mV
LOGIC INTERFACE ($\overline{RE}$, RO, DE, DI)							
Input Voltage High	V_{IH}	DE, DI, $\overline{RE}$	MAX22500E	2/3 x V_L			V
			MAX22501E, $3V \le V_{CC} \le 5.5V$	2/3 x V_{CC}			
			MAX22501E, V_{CC} = 5.25V	2.85			
Input Voltage Low	V_{IL}	DE, DI, $\overline{RE}$	MAX22500E			1/3 x V_L	V
			MAX22501E			1/3 x V_{CC}	
Input Current	I_{IN}	DI and DE, $\overline{RE}$ (after first transition)		-2		+2	µA
Input Impedance on First Transition	R_{IN_FT}	DE, $\overline{RE}$				10	kΩ
RO Output High Voltage	V_{OH}	$\overline{RE}$ = GND, $(V_A - V_B)$ > 200mV, I_{OUT} = -1mA	MAX22500E	V_L – 0.4			V
		$\overline{RE}$ = GND, $(V_A - V_B)$ > 200mV, I_{OUT} = -1mA	MAX22501E	V_{CC} - 0.4			
RO Output Low Voltage	V_{OL}	$\overline{RE}$ = GND, $(V_A – V_B)$ < -200mV, I_{OUT} = +1mA				0.4	V

Electrical Characteristics (continued)

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC} (MAX22500E only), $V_L \le V_{CC}$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.) (Note 1, Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Three-State Output Current at Receiver	I_{OZR}	$\overline{RE}$= high, $0 \le V_{RO} \le V_{CC}$	-1		+1	µA
PROTECTION						
Thermal Shutdown Threshold	T_{SH}	Temperature rising		+160		°C
Thermal Shutdown Hysteresis	T_{SH_HYS}			10		°C
ESD Protection (A and B Pins)		Human Body Model		±15		kV
		IEC61000-4-2 Air Gap Discharge to GND		±7		
		IEC61000-4-2 Contact Discharge to GND		±6		
ESD Protection (All Other Pins)		Human Body Model		±2		kV

Electrical Characteristics—Switching

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC} (MAX22500E only), $V_L \le V_{CC}$, TA = T_{MIN} to T_{MAX}, unless otherwise noted (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER (Note 5)							
Driver Propagation Delay	t_{DPLH}	R_L = 54Ω, CL = 50pF, Figure 3, Figure 4			7	20	ns
	t_{DPHL}	R_L = 54Ω, CL = 50pF, Figure 3, Figure 4			7	20	
Differential Driver Output Skew	t_{DSKEW}	$\lvert t_{DPLH} - t_{DPHL} \rvert$, R_L = 54Ω, C_L= 50pF, Figure 3, Figure 4 (Note 6)	MAX22501E			1.2	ns
			MAX22500E, $V_L = V_{CC}$, $V_{CC} \ge 3V$			1.2	
			MAX22500E, $V_L \ne V_{CC}$			1.6	
Driver Differential Output Rise and Fall Time	t_{HL}, t_{LH}	R_L = 54Ω, C_L = 50pF, Figure 4 (Note 6)			1.6	3	ns
Data Rate	DR					100	Mbps
Driver Enable to Output High	t_{DZH}	R_L = 500Ω, CL = 50pF, Figure 5, Figure 6			15	30	ns
Driver Enable to Output Low	t_{DZL}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6			15	30	ns
Driver Disable Time from High	t_{DHZ}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6			23	30	ns
Driver Disable Time from Low	t_{DLZ}	R_L = 500Ω, C_L = 50pF, Figure 5, Figure 6			23	30	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 5, Figure 6			52	100	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 5, Figure 6			52	100	µs
Time to Shutdown	t_{SHDN}	(Notes 7, 8)		50	140	800	ns

Electrical Characteristics—Switching (continued)

(V_{CC} = 3V to 5.5V, V_L = 1.6V to V_{CC} (MAX22500E only), $V_L \le V_{CC}$, TA = T_{MIN} to T_{MAX}, unless otherwise noted (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Preemphasis Interval	t_{PRE}	MAX22500E only, 4.5V ≤ V_{CC} ≤ 5.5V, R_L = 100Ω, Figure 2	R_{PSET} = 4kΩ	10	13	16	ns
			R_{PSET} = 400kΩ	0.8	1	1.2	µs
RECEIVER (Note 5)							
Delay to Fail-Safe Operation	t_{D_FS}				10		µs
Receiver Propagation Delay	t_{RPLH},t_{RPHL}	C_L = 15pF, Figure 7, Figure 8			17	20	ns
Receiver Output Skew	t_{RSKEW}	$\lvert t_{RPHL} - t_{RPLH} \rvert$, C_L= 15pF, Figure 7, Figure 8 (Note 6)				2.5	ns
Data Rate	DR					100	Mbps
Receiver Enable to Output High	t_{RZH}	R_L = 1kΩ, C_L = 15pF, Figure 9			19	30	ns
Receiver Enable to Output Low	t_{RZL}	R_L = 1kΩ, C_L = 15pF, Figure 9			19	30	ns
Receiver Disable Time from High	t_{RHZ}	R_L = 1kΩ, C_L = 15pF, Figure 9			12	30	ns
Receiver Disable Time from Low	t_{RLZ}	R_L = 1kΩ, C_L = 15pF, Figure 9			12	30	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 9			52	100	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, Figure 9			52	100	µs
Time to Shutdown	t_{SHDN}	(Notes 7, 8)		50	140	800	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications for all temperature limits are guaranteed by design.

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.

Note 3: V_{ODP} is the differential voltage between A and B during the preemphasis interval on the MAX22500E, and is the differential voltage when preemphasis is disabled. $V_{ODP} = D_{PRE} \times V_{OD}$.

Note 4: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 5: Capacitive load includes test probe and fixture capacitance.

Note 6: Not production tested. Guaranteed by design.

Note 7: Shutdown is enabled by driving $\overline{RE}$ high and DE low. The device is guaranteed to have entered shutdown after t_{SHDN} has elapsed.

Note 8: The timing parameter refers to the driver or receiver enable delay, when the device has exited the initial hot-swap protect state and is in normal operating mode.

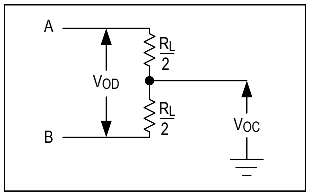


Figure 1. Driver DC Test Load

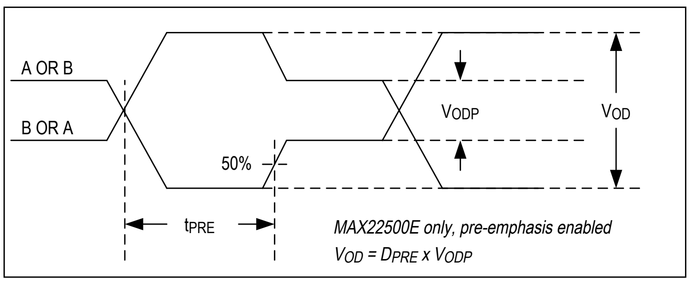


Figure 2. Driver Preemphasis Timing

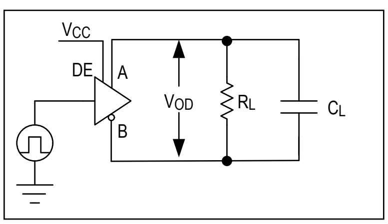


Figure 3. Driver Timing Test Circuit

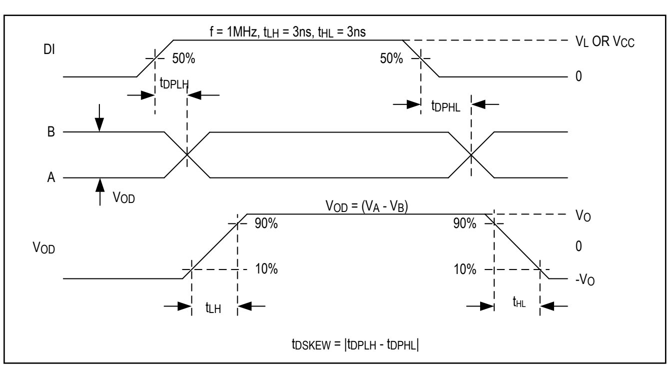


Figure 4. Driver Propagation Delays

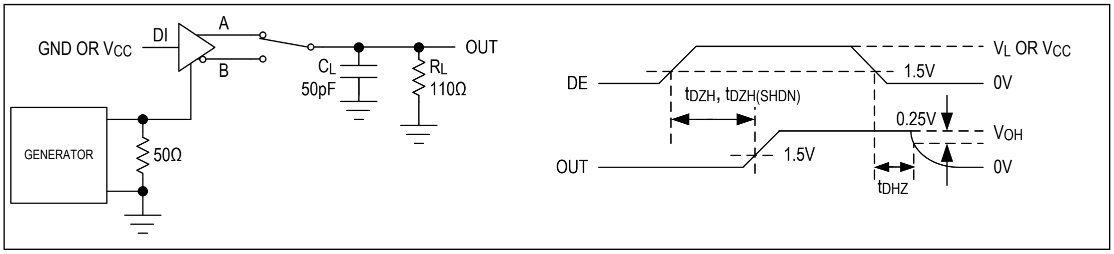


Figure 5. Driver Enable and Disable Times (t_{DZH}, t_{DHZ})

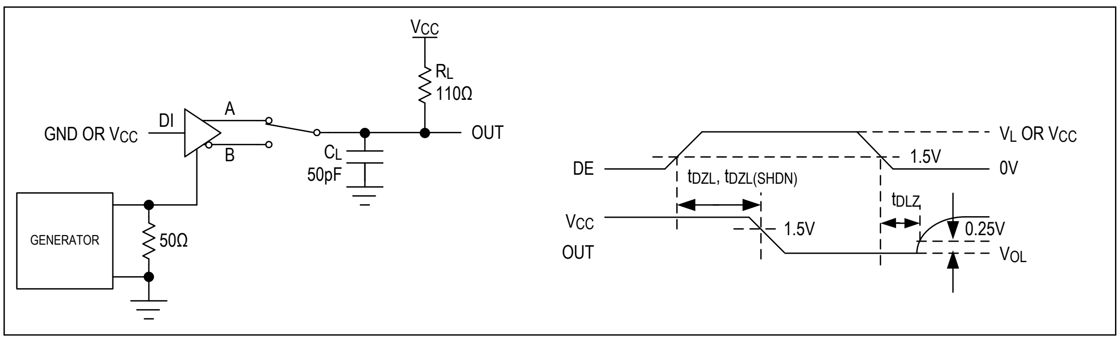


Figure 6. Driver Enable and Disable Times (t_{DZL}, t_{DLZ})

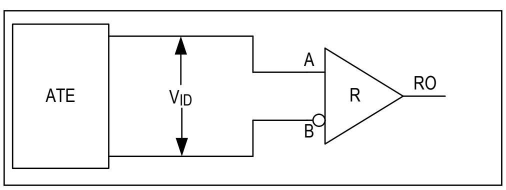


Figure 7. Receiver Propagation Delay Test Circuit

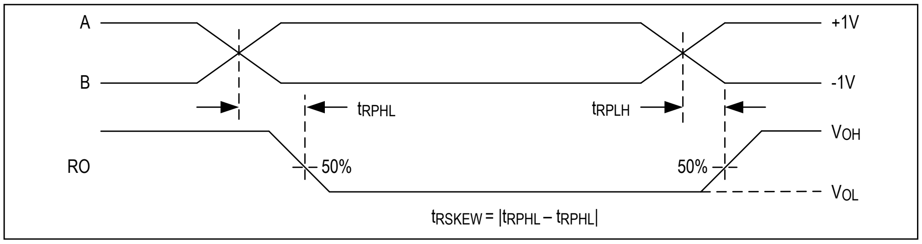


Figure 8. Receiver Propagation Delays

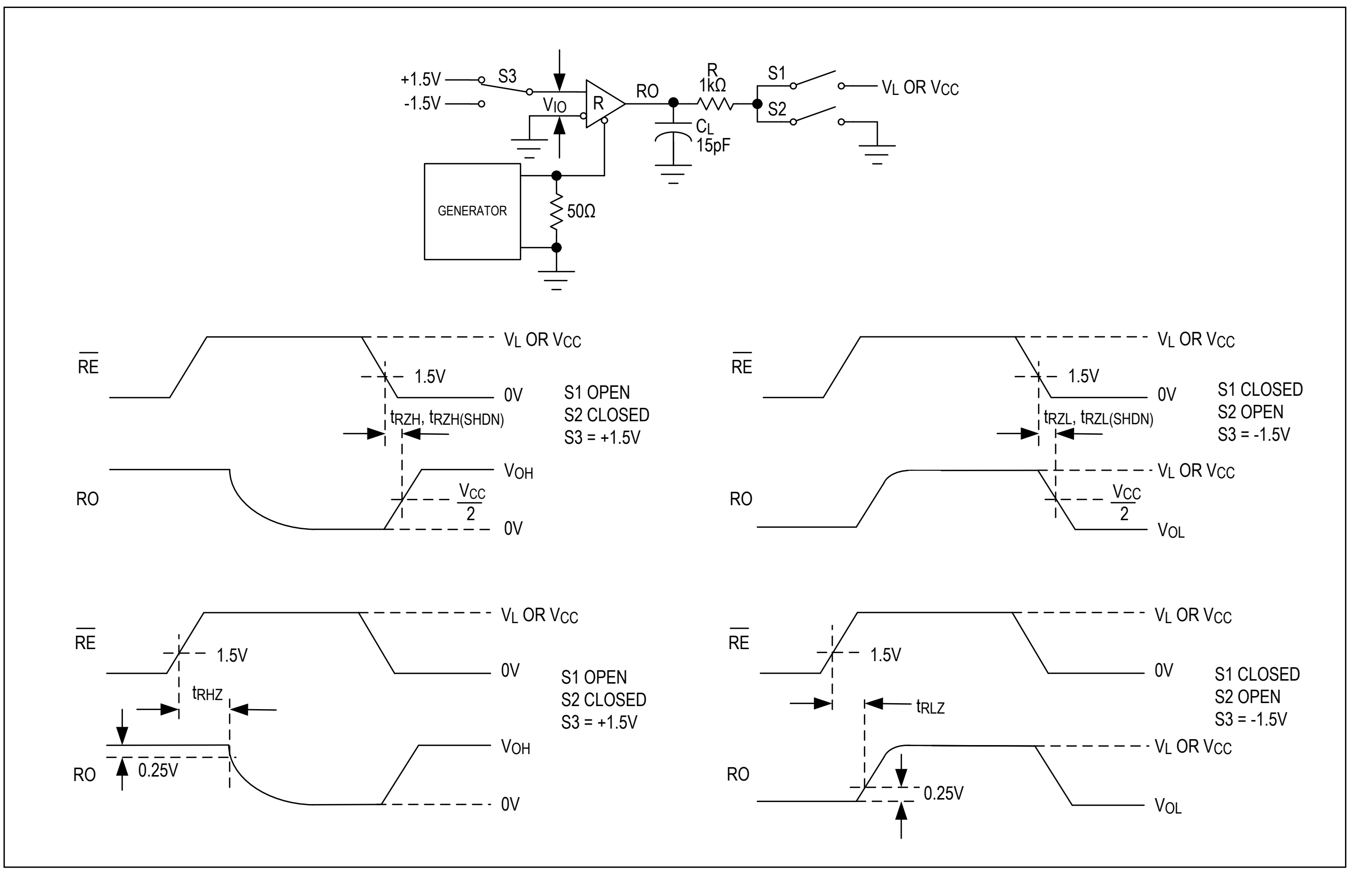
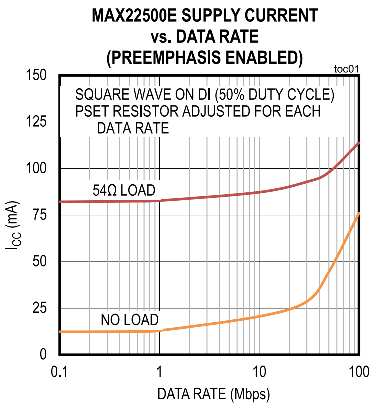
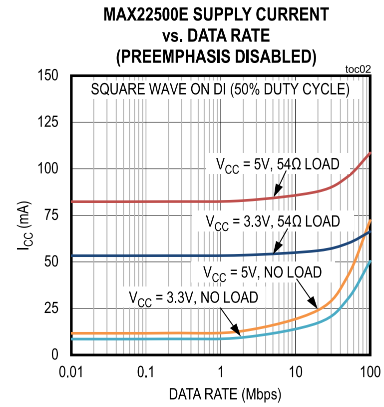


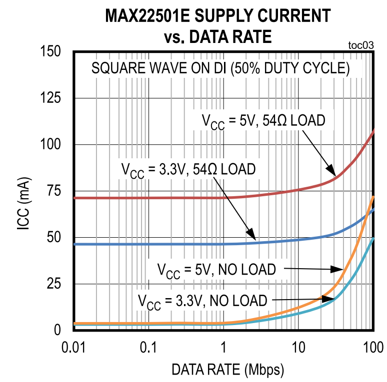
Figure 9. Receiver Enable and Disable Times

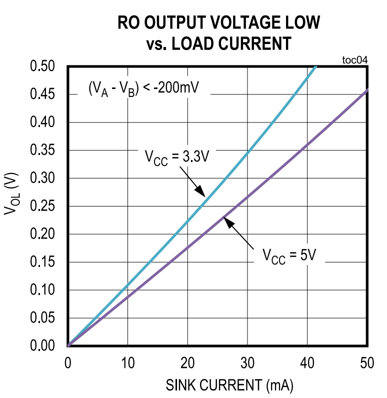
Typical Operating Characteristics

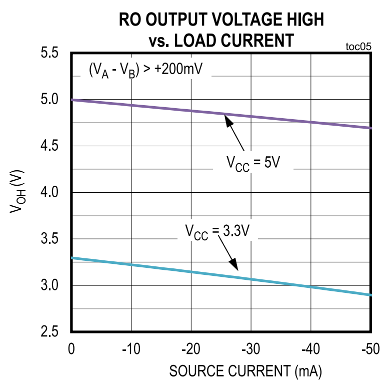
(V_{CC} = 5V, V_L = V_{CC} (MAX22500E only), 60Ω termination between A and B, T_A = 25°C, unless otherwise noted.)

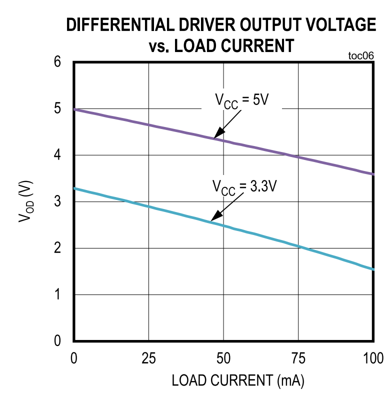


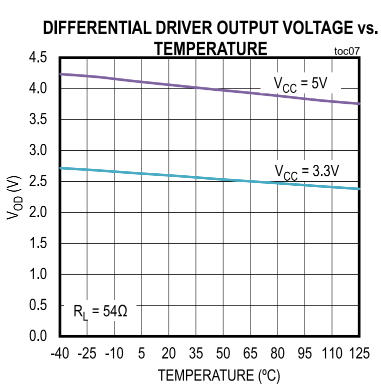


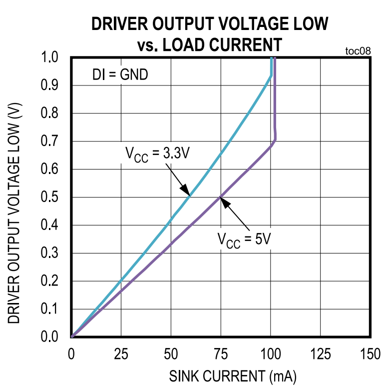


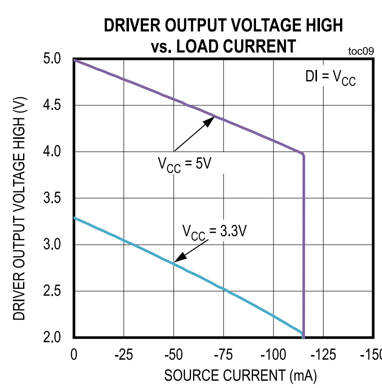






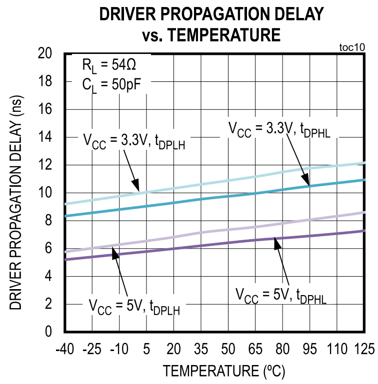


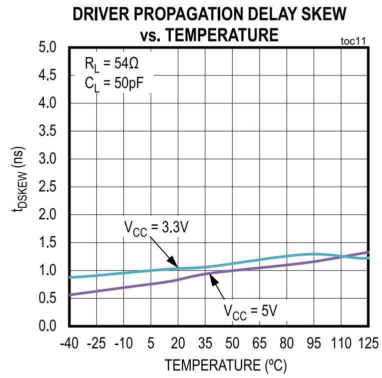


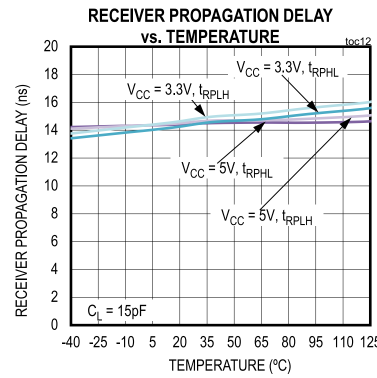


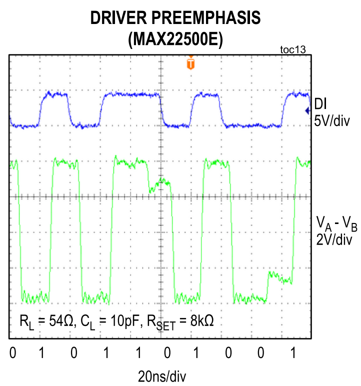
Typical Operating Characteristics (continued)

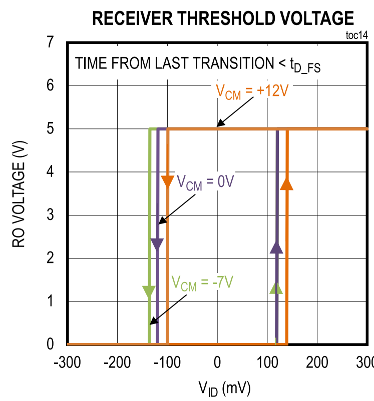
(V_{CC} = 5V, V_L = V_{CC} (MAX22500E only), 60Ω termination between A and B, T_A = 25°C, unless otherwise noted.)





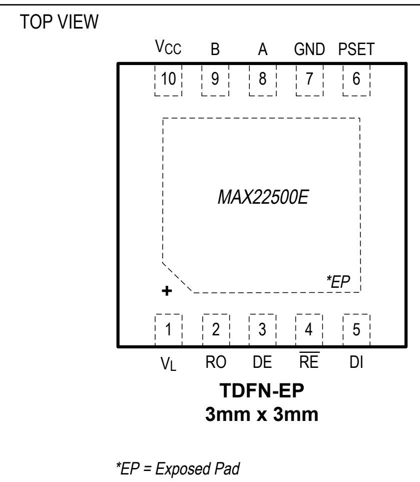




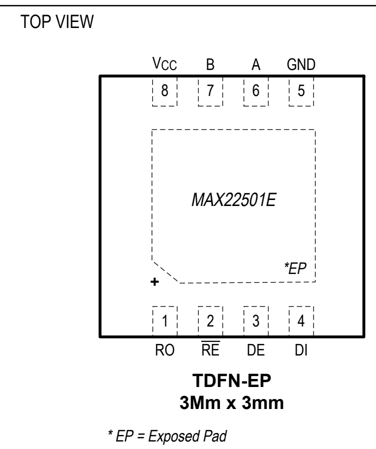


Pin Configurations

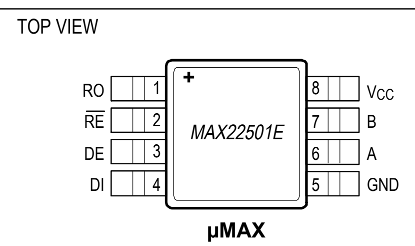
MAX22500E TDFN-EP



MAX22501E TDFN-EP



MAX22501E µMAX



Pin Description

PIN			NAME	FUNCTION
MAX22500E TDFN-EP	MAX22501E TDFN-EP	MAX22501E µMAX		
1	—	—	V_L	Logic Supply Input. V_L defines the interface logic levels on DE, DI and RO. Apply a voltage between 1.6V to 5.5V to V_L. Bypass V_L to ground with a 0.1µF capacitor as close to the device as possible.
2	1	1	RO	Receiver Output. See the Receiving Function Table for more information.
3	3	3	DE	Driver Output Enable. Force DE high to enable driver. Pull DE low to three-state the driver output.
4	2	2	$\overline{RE}$	Receiver Enable. Pull $\overline{RE}$ high to disable and the receiver and tri-state RO. The device is in low-power shutdown when $\overline{RE}$ = high and DE = low.
5	4	4	DI	Driver Input. See the Transmitting Function Table for more information.
6	—	—	PSET	Preemphasis Select Control Input. Connect a resistor from PSET to GND to select the preemphasis duration. See the *Layout Recommendations* in the *Applications Information* section for more information. To disable preemphasis, connect PSET to GND or V_{CC}.
7	5	5	GND	Ground
8	6	6	A	Noninverting Receiver Input/Driver Output
9	7	7	B	Inverting Receiver Input/Driver Output
10	8	8	V_{CC}	Supply Input. Bypass V_{CC} to ground with a 0.1µF ceramic capacitor as close to the device as possible.
EP	EP	—	—	Exposed Pad. Connect to ground.

Functional Diagrams

Half-Duplex

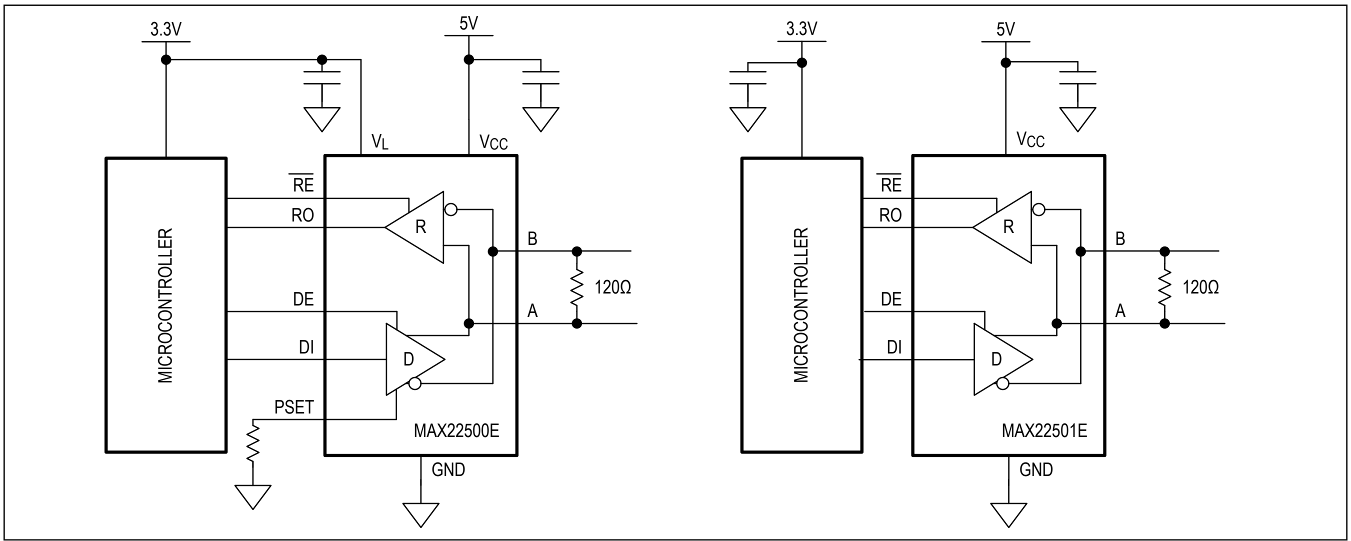


Table 1. Transmitting Function Table

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	A	B
X	1	1	1	0
X	1	0	0	1
0	0	X	High Impedance	High Impedance
1	0	X	Shutdown. A and B are high impedance	

X = Don't care

Table 2. Receiving Function Table

INPUTS				OUTPUTS
$\overline{RE}$	DE	$(V_A - V_B)$	Time from Last A-B Transition	RO
0	X	≥ +200mV	Always	1
0	X	$-200mV < (V_A - V_B) < +200mV$	$< t_{D\_FS}$	Indeterminate RO is latched to previous value
0	X	$-50mV < (V_A - V_B) < +50mV$	$> t_{D\_FS}$	1
0	X	≤ -200mV	Always	0
0	0	Open/Shorted	$> t_{D\_FS}$	1
1	1	X	X	High Impedance
1	0	X	X	Shutdown. RO is high impedance

X = Don't care

Detailed Description

The MAX22500E/MAX22501E ESD-protected RS-485/RS-422 transceivers are optimized for high-speed, half-duplex communications over long cables. Both transceivers feature integrated hot-swap functionality to eliminate false transitions on the driver during power-up or during a hot-plug event. These transceivers also feature fail-safe receiver inputs, guaranteeing a logic-high on the receiver output when inputs are shorted or open for longer than 10μs (typ).

Receiver Threshold Voltages

The MAX22500E and MAX22501E receivers feature large threshold hysteresis of 250mV (typ) for increased differential noise rejection. Additionally, the receivers feature symmetrical threshold voltages. Symmetric thresholds have the advantage that recovered data at the RO output does not have duty cycle distortion. Typically, fail-safe receivers, which have unipolar (non-symmetric) thresholds, show some duty cycle distortion at high signal attenuation due to long cable lengths.

Preemphasis (MAX22500E only)

The MAX22500E features integrated driver preemphasis circuitry, which strongly improves signal integrity at high data rates over long distances by reducing inter-symbol interference (ISI) caused by long cables. Preemphasis is set by connecting a resistor (R_{PSET}) between PSET and ground. Long cables attenuate the high-frequency content of transmitted signals due to the cable's limited bandwidth. This causes signal/pulse distortion at the receiving end, resulting in ISI. ISI causes jitter in data and clock recovery circuits. ISI can be visualized by considering the following cases: If a series of ones (1's) is transmitted, followed by a zero (0), the transmission-line voltage has risen to a high value by the end of the string of ones. It takes longer for the signal to move toward the '0' state because the starting voltage on the line is so far from the zero crossing. Similarly, if a data pattern has a string of zeros followed by a one and then another zero, the one-to-zero transition starts from a voltage that is much closer to the zero-crossing (V_A - V_B = 0) and it takes much less time for the signal to reach the zero crossing. Preemphasis reduces ISI by boosting the differential signal amplitude at every transition edge, counteracting the high frequency attenuation of the cable. When the DI input changes from a logic-low to a logic-high, the differential output (V_A - V_B) is driven high to V_{ODP}. At the end of the preemphasis interval, the differential voltage returns to a lower level (V_{OD}). The preemphasis differential high voltage (V_{ODP}) is typically 1.37 the V_{OD} voltage. If DI switches back to a logic-low state before the preemphasis interval ends, the differential output switches directly from the 'strong' V_{ODP} high to a 'strong' low (-V_{ODP}). Driver behavior is similar when the DI input changes from a logic-high to a logic-low. When this occurs, the differential output is pulled low to -V_{ODP} until the end of the preemphasis interval, at which point V_A - V_B = -V_{ODP}.

Setting the Preemphasis Interval

Connect a resistor (R_{PSET}) between PSET and GND to set the preemphasis time interval on the MAX22500E. An optimum preemphasis interval ranges from 1 to 1.5 unit intervals (bit time). Use the following equation to calculate the resistance needed on PSET to achieve a 1.2 preemphasis interval:

$$R_{PSET} = 400\text{x}10^9 / DR$$

where DR is the data rate and 1Mbps ≤ DR ≤ 100Mbps. Preemphasis only minimally degrades the jitter on the eye diagram when using short cables, making it reasonable to permanently enable preemphasis on systems where cable lengths may vary or change. Figure 10 and Figure 11 are eye diagrams taken at 100Mbps over a 10m Cat-5e cable. Note that the eye varies only slightly as preemphasis is enabled or disabled. Figure 12 and Figure 13 show the driver eye diagrams over a long cable length. The MAX22500E was used as the driver and the eye diagrams were taken at the receiver input after a length of 100m Cat-5e cable. Figure 12 shows the signal at the receiver when the driver preemphasis is disabled. Figure 13 shows the receiver signal when preemphasis is enabled.

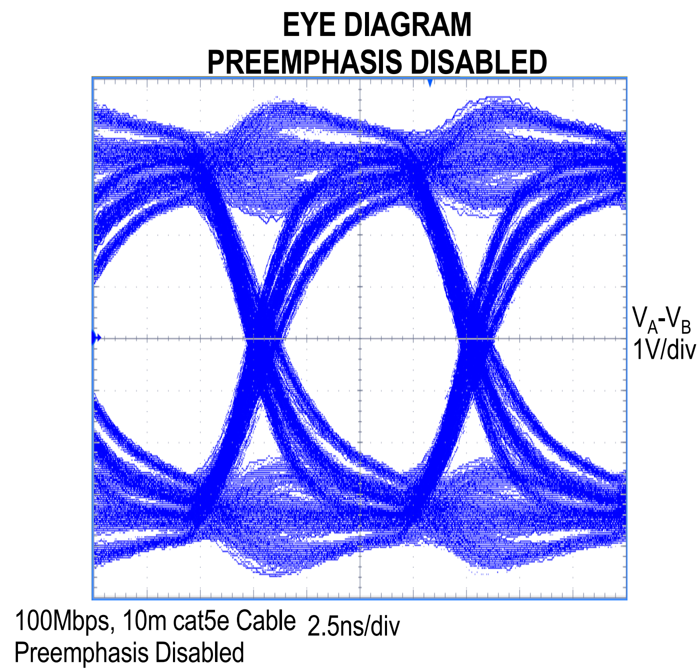


Figure 10. Eye Diagram, 100Mbps Over 10m Cat-5e Cable, Preemphasis Disabled

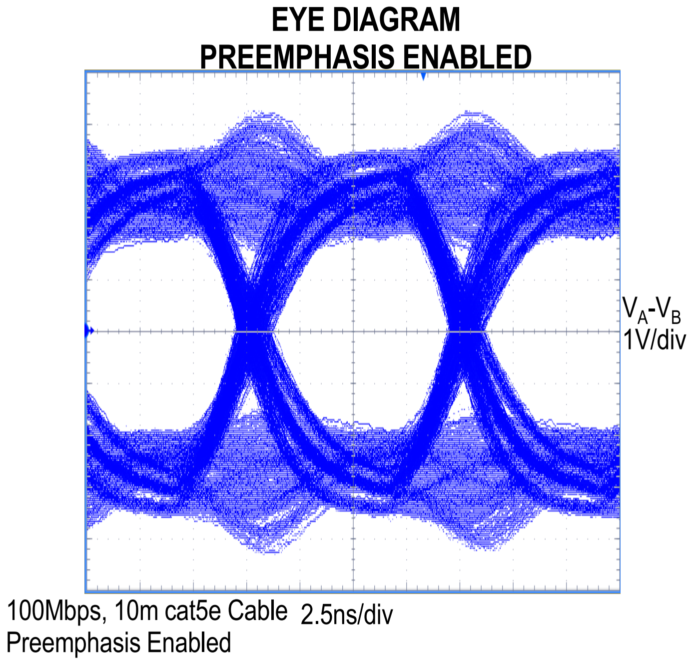


Figure 11. Eye Diagram, 100Mbps Over 10m Cat-5e Cable, Preemphasis Enabled

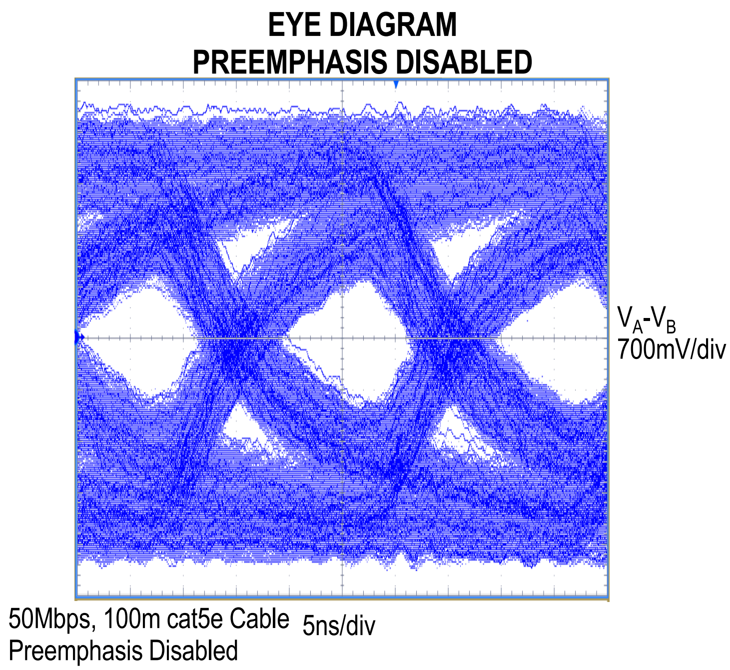


Figure 12. Eye Diagram, 50Mbps Over 100m Cat-5e Cable, Preemphasis Disabled

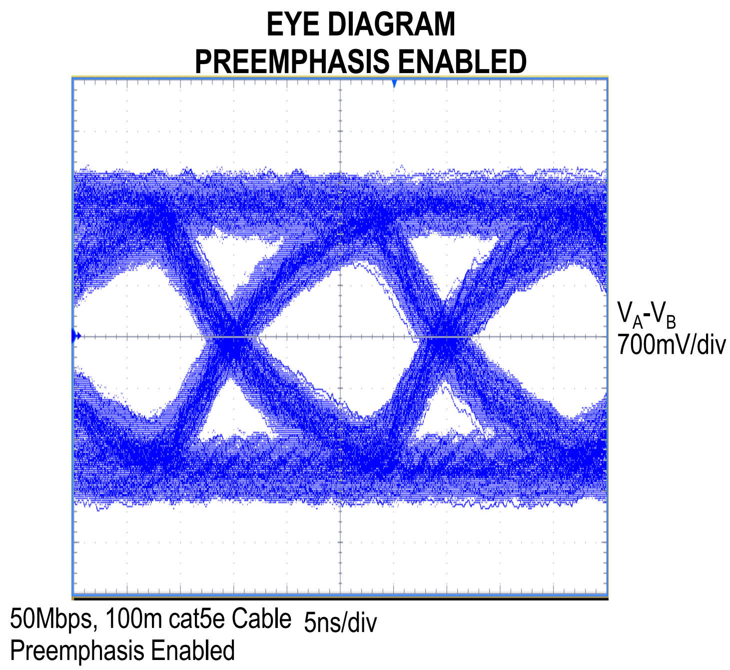


Figure 13. Eye Diagram, 50Mbps Over 100m Cat-5e Cable, Preemphasis Enabled

Fail-Safe Functionality

The MAX22500E/MAX22501E feature fail-safe receiver inputs, guaranteeing a logic-high on the receiver output (RO) when the receiver inputs are shorted or open for longer than 10µs (typ). When the differential receiver input voltage is greater than -50mV [(V_A - V_B) ≥ -50mV] for more than 10µs (typ), RO is logic-high. For example, in the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination resistor, so (V_A - V_B = 0V) > -50mV and RO is guaranteed to be a logic-high after 10µs (typ).

Driver Single-Ended Operation

The A and B outputs on the MAX22500E/MAX22501E can be used in the standard differential operating mode or as single-ended outputs. Because the driver outputs swing rail-to-rail, they can also be used as individual standard TTL logic outputs.

Hot-Swap Inputs

Inserting circuit boards into a hot or powered backplane can cause voltage transients on DE, $\overline{RE}$, and receiver inputs A and B that can lead to data errors. For example, upon initial circuit board insertion, the processor undergoes a power-up sequence. During this period, the high impedance state of the output drivers makes them unable to drive the MAX22500E/MAX22501E enable inputs to a defined logic level. Meanwhile, leakage currents of up to 10µA from the high-impedance output or capacitively coupled noise from V_{CC} or GND could cause an input to drift to an incorrect logic state. To prevent such a condition from occurring, the MAX22500E/MAX22501E features hot-swap input circuitry on DE and $\overline{RE}$ to safeguard against unwanted driver activation during hot-swap situations. When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{RE}$ high for at least 10µs. After the initial power-up sequence, the internal pulldown/pullup circuitry becomes transparent, resetting the hot-swap tolerable inputs.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Low-Power Shutdown Mode

The MAX22500E/MAX22501E feature a low-power shutdown mode to reduce supply current when the transceiver is not needed. Pull the $\overline{RE}$ input high and the DE input low to put the device in low-power shutdown mode. If the inputs are in this state for at least 800ns, the parts are guaranteed to enter shutdown. The MAX22500E/MAX22501E draw 5μA (max) of supply current when the device is in shutdown. The $\overline{RE}$ and DE inputs can be driven simultaneously. The MAX22500E/MAX22501E are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns.

Applications Information

Layout Recommendations

Ensure that the preemphasis set resistor (R_{PSET}) is located close to the PSET and GND pins in order to minimize interference by other signals. Minimize the trace length to the PSET resistor. Additionally, place a ground plane under R_{PSET} and surround it with ground connections/traces to minimize interference from the A and B switching signals. See Figure 14.

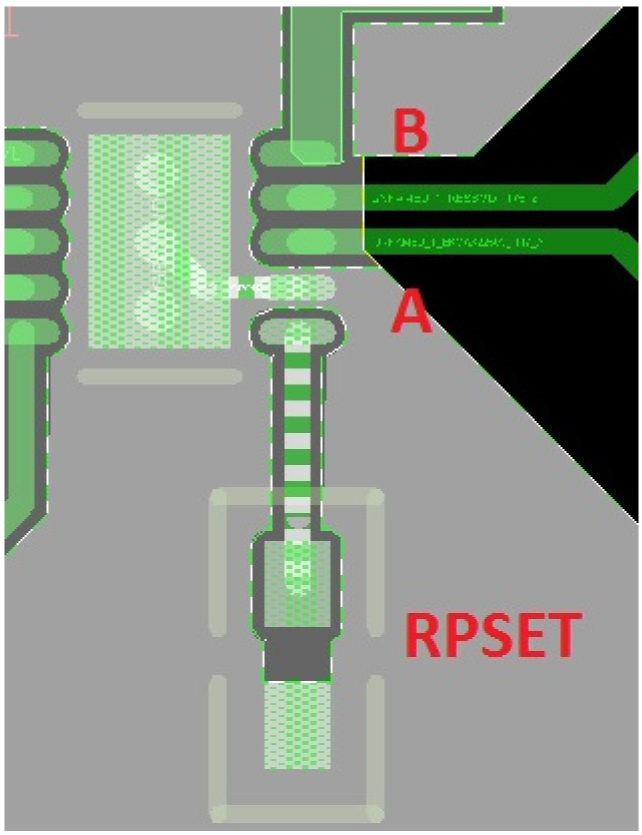


Figure 14. Sample PSET Resistor Placement

Network Topology

The MAX22500E/MAX22501E transceivers are designed for high-speed bidirectional RS-485/RS-422 data communications. Multidrop networks can cause impedance discontinuities which affect signal integrity. Maxim recommends using a point-to-point network topology (Figure 15), instead of a multidrop topology, when communicating with high data rates. Terminate the transmission line at both ends with the cable's characteristic impedance to reduce reflections.

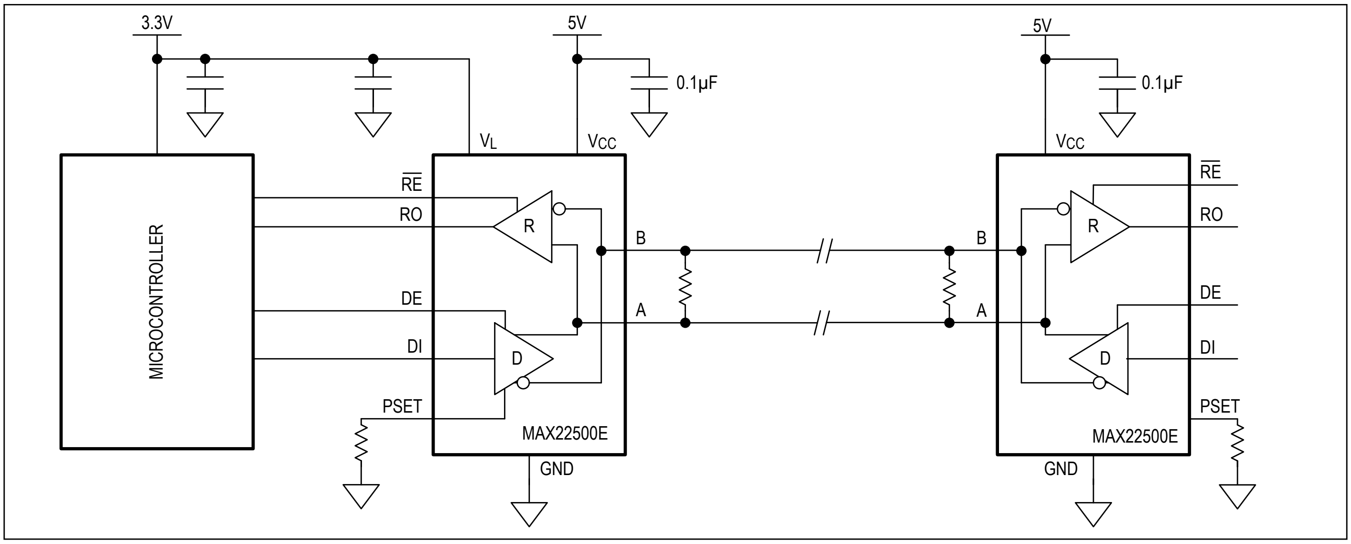


Figure 15. Point-to-Point Half-Duplex Communication for High Speeds

Ordering Information

PART	PREEMPHASIS	LOGIC SUPPLY	PIN-PACKAGE	PIN-PITCH (mm)	PACKAGE CODE
MAX22500EATB+	Y	Y	TDFN10-EP*	0.5	T1033+2
MAX22500EATB+T	Y	Y	TDFN10-EP*	0.5	T1033+2
MAX22501EATA+	N	N	TDFN8-EP*	0.65	T833+2
MAX22501EATA+T	N	N	TDFN8-EP*	0.65	T833+2
MAX22501EAUA+	N	N	µMAX8	0.65	U8+1
MAX22501EAUA+T	N	N	µMAX8	0.65	U8+1

+ Denotes a lead (Pb)-free/RoHS-compliant package.

** EP = Exposed Pad*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	6/20	Added MAX22501EAUA+ and MAX22501EAUA+T to the *Ordering Information* section; updated the *Benefits and Features* section and Table 2; added TOC14; fixed various typos	1, 5–6, 14–16, 25
2	2/21	Updated the *General Description, Electrical Characteristics, Pin Configurations*, and *Pin Description* sections	4, 6, 12–14
3	12/21	Updated the *Hot-Swap Inputs* section and *Simplified Block Diagram*	1, 19