Click here to ask an associate for production status of specific part numbers.

MAX22245, MAX22246

Reinforced, Fast, Low-Power, Two-Channel Digital Isolators

Product Highlights

- **AEC-Q100 Qualification for /V devices**
- Reinforced Galvanic Isolation for Digital Signals
  - 8-SOIC with 8mm of Creepage and Clearance
  - Withstands $5kV_{RMS}$ for 60s (V_{ISO})
  - Continuously Withstands $848V_{RMS}$ (V_{IOWM})
  - Withstands ±12.8kV Surge Between GNDA and GNDB with 1.2/50µs Waveform
  - High CMTI (50kV/µs, typ)
- Low Power Consumption
  - 0.78mW per Channel at 1Mbps with $V_{DD\_}$ = 1.8V
  - 1.47mW per Channel at 1Mbps with $V_{DD\_}$ = 3.3V
  - 3.28mW per Channel at 100Mbps with $V_{DD\_}$ = 1.8V
- Low Propagation Delay and Low Jitter
  - Maximum Data Rate Up to 200Mbps
  - Low Propagation Delay 7ns (typ) at $V_{DD\_}$ = 3.3V
  - Clock Jitter RMS 7.5ps (typ)
- Safety Regulatory Approvals
  - UL According to UL1577
  - cUL According to CSA Bulletin 5A
  - VDE 0884-11 Reinforced Insulation (Pending)

Key Applications

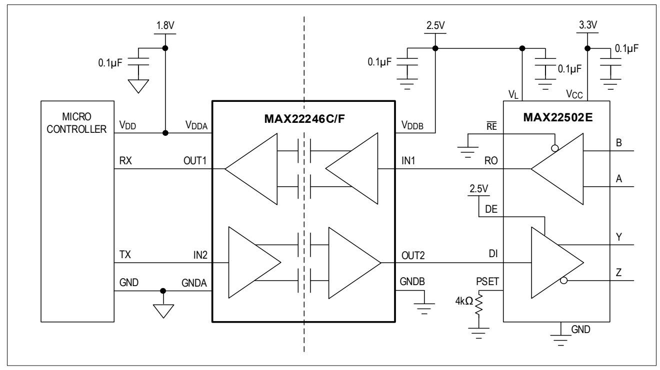
- Automotive
  - Hybrid Electric Vehicle
  - Chargers
  - Battery Management Systems (BMS)
  - Inverters

The MAX22245/MAX22246 are a family of 2-channel reinforced, fast, low-power digital galvanic isolators using Analog Devices' proprietary process technology. All devices feature reinforced isolation for a withstand voltage rating of $5kV_{RMS}$ for 60 seconds. Both automotive and general-purpose devices are rated for operation at ambient temperatures of -40°C to +125°C.

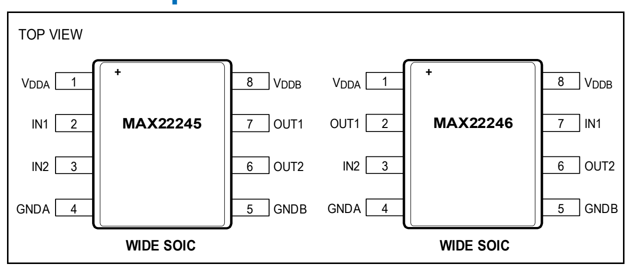
Devices with /V suffix are AEC-Q100 qualified. Refer to the *Ordering Information* for all automotive grade part numbers.

- Industrial
  - Isolated SPI
  - Isolated RS-232, RS-485/RS-422, CAN
  - Fieldbus Communications
  - Motor Drive

Simplified Application Diagram



Pin Description



These devices transfer digital signals between circuits with different power domains, using as little as 0.78mW per-channel at 1Mbps (1.8V supply). The low-power feature reduces system dissipation, increases reliability, and enables compact designs.

Devices are available with a maximum data rate of 25Mbps or 200Mbps, and with outputs that are either default high or default low. The devices feature low propagation delay and low clock jitter, which reduces system latency.

Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX22245 features two channels transferring data in the same direction. The two channels of the MAX22246 transfer data in opposite directions, and this makes the MAX22246 ideal for isolating the Tx and Rx lines of a transceiver.

Ordering Information appears at end of data sheet.

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Absolute Maximum Ratings

V_{DDA} to GNDA.. -0.3V to +6V

V_{DDB} to GNDB.. -0.3V to +6V

IN_ on Side A to GNDA .... -0.3V to +6V

IN_ on Side B to GNDB .... -0.3V to +6V

OUT_ on Side A to GNDA ....-0.3V to (V_{DDA} + 0.3V)

OUT_ on Side B to GNDB ....-0.3V to (V_{DDB} + 0.3V)

Short-Circuit Continuous Current

OUT_ on Side A to GNDA .... ±30mA

OUT_ on Side B to GNDB .... ±30mA

Continuous Power Dissipation (T_A = +70°C)

Wide SOIC (derate 11.35mW/°C above +70°C) ... 908.1mW

Temperature Ratings

Operating Temperature Range.................. -40°C to +125°C

Maximum Junction Temperature ....+150°C

Storage Temperature Range..................... -60°C to +150°C

Lead Temperature (soldering, 10s) ....+300°C

Soldering Temperature (reflow)...............................+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

8 Wide SOIC

PACKAGE CODE	W8MS+7
Outline Number	*21-100415*
Land Pattern Number	*90-100146*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	88.1°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	42.4°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				45		mV
MAX22245 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.31	0.57	mA
			V_{DDA} = 3.3V		0.30	0.56	
			V_{DDA} = 2.5V		0.30	0.56	
			V_{DDA} = 1.8V		0.29	0.41	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		2.38	3.25	
			V_{DDA} = 3.3V		2.32	3.18	
			V_{DDA} = 2.5V		2.29	3.14	
			V_{DDA} = 1.8V		2.22	2.89	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		0.60	1.11	mA
			V_{DDB} = 3.3V		0.59	1.10	
			V_{DDB} = 2.5V		0.59	1.09	
			V_{DDB} = 1.8V		0.58	1.06	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		3.02	3.80	
			V_{DDB} = 3.3V		2.12	2.80	
			V_{DDB} = 2.5V		1.74	2.35	
			V_{DDB} = 1.8V		1.42	1.95	
MAX22246 SUPPLY CURRENT (Note 2)							
Side A Supply Current	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.46	0.84	mA
			V_{DDA} = 3.3V		0.45	0.83	
			V_{DDA} = 2.5V		0.44	0.83	
			V_{DDA} = 1.8V		0.44	0.74	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		2.65	3.50	
			V_{DDA} = 3.3V		2.18	2.95	
			V_{DDA} = 2.5V		1.98	2.72	
			V_{DDA} = 1.8V		1.80	2.40	
Side B Supply Current	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		0.46	0.84	mA
			V_{DDB} = 3.3V		0.45	0.83	
			V_{DDB} = 2.5V		0.44	0.83	
			V_{DDB} = 1.8V		0.44	0.74	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		2.65	3.50	
			V_{DDB} = 3.3V		2.18	2.95	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{DDB} = 2.5V		1.98	2.72	
			V_{DDB} = 1.8V		1.80	2.40	
LOGIC INTERFACE (IN_, OUT_)							
Input High Voltage	V_{IH}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		0.7 x $V_{DD\_}$			V
		1.71V ≤ $V_{DD\_}$ < 2.25V		0.75 x $V_{DD\_}$			
Input Low Voltage	V_{IL}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V				0.8	V
		1.71V ≤ $V_{DD\_}$ < 2.25V				0.7	
Input Hysteresis	V_{HYS}	MAX2224_B/E			410		mV
		MAX2224_C/F			80		
Input Pullup Current	I_{PU}	MAX2224_B/C		-10	-5	-1.5	µA
Input Pulldown Current	I_{PD}	MAX2224_E/F		1.5	5	10	µA
Input Capacitance	C_{IN}	f_{SW} = 1MHz			2		pF
Output Voltage High	V_{OH}	I_{OUT} = -4mA source		$V_{DD\_}$ - 0.4			V
Output Voltage Low	V_{OL}	I_{OUT} = 4mA sink				0.4	V

Dynamic Characteristics MAX2224_C/F

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)			50		kV/µs
Maximum Data Rate	DR_{MAX}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		200			Mbps
		1.71V ≤ $V_{DD\_}$ < 2.25V		150			
Minimum Pulse Width	PW_{MIN}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V				5	ns
		1.71V ≤ $V_{DD\_}$ < 2.25V				6.67	
Propagation Delay (*Figure 1*)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.4	6.2	9.5	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	4.8	7.0	11.2	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.3	8.3	14.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.1	12.3	22.1	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	4.6	6.5	9.9	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	5.0	7.3	11.6	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	5.4	8.5	14.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	7.2	12.1	21.8	
Pulse Width Distortion	PWD	$\|t_{PLH} - t_{PHL}\|$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		0.4	2	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		0.4	2	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		0.3	2	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V		0.0	2	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				3.7	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				6.9	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				12.1	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				4.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				4.9	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				7.0	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				11.8	
Propagation Delay Skew Channel-to-Channel (Same Direction) (*Figure 1*)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2	ns
	t_{SCOHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				2	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	200Mbps			100		ps
Clock Jitter RMS	$t_{JCLK(RMS)}$	500kHz clock input, rising/falling edges			7.5		ps
Rise Time (*Figure 1*)	t_R	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			2.4	
Fall Time (*Figure 1*)	t_F	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			3	

Dynamic Characteristics MAX2224_B/E

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD\_}$ (Note 5)			50		kV/µs
Maximum Data Rate	DR_{MAX}			25			Mbps
Minimum Pulse Width	PW_{MIN}					40	ns
Glitch Rejection				10	17	29	ns
Propagation Delay (*Figure 1*)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.7	22.6	30.7	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	17.0	23.4	32.2	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.7	24.8	35.3	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.6	28.8	42.8	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	16.4	22.7	32.1	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	16.8	23.5	33.8	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	17.3	24.8	36.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	19.0	28.4	43.7	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ $V_{DD\_}$ ≤ 5.5V		0.1	4	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V		0.1	4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V		0.0	4	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V		0.4	4	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				14.0	ns
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.8	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.2	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.9	
	t_{SPHL}	4.5V ≤ $V_{DD\_}$ ≤ 5.5V				13.0	
		3.0V ≤ $V_{DD\_}$ ≤ 3.6V				13.5	
		2.25V ≤ $V_{DD\_}$ ≤ 2.75V				15.4	
		1.71V ≤ $V_{DD\_}$ ≤ 1.89V				21.4	
Propagation Delay Skew Channel-to-Channel (Same Direction) (*Figure 1*)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4	ns
	t_{SCOHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				4	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	25Mbps			250		ps
Rise Time (*Figure 1*)	t_R	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			2.4	
Fall Time (*Figure 1*)	t_F	C_L = 5pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			1	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			3	

Note 1: General purpose devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization. Automotive devices are 100% production tested at T_A = +25°C and T_A = +125°C.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

ESD Protection

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
ESD		Human Body Model, All Pins	±3	kV
		IEC 61000-4-2 Contact, GNDB to GNDA	±7	

Test Circuit and Timing Diagram

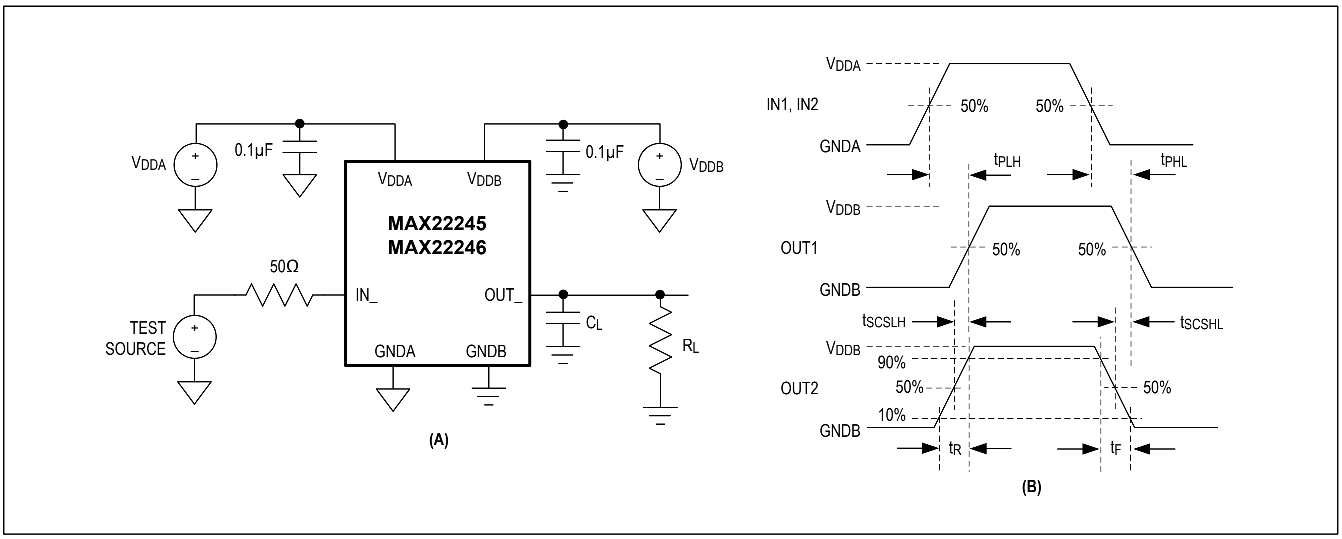


Figure 1. Test Circuit (A) and Timing Diagram (B)

Table 1. Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	3977	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	1200	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	7000	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Note 6) (Note 7)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 12800V_{PEAK} (Note 6) (Note 9)	8000	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V, T_S = 150°C	> 10^9	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (Note 8)	1.5	pF
Minimum Creepage Distance	CPG		8	mm
Minimum Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	> 400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOTM}, V_{IOWM}, V_{IORM} and V_{IOSM} are defined by the IEC 60747-5-5 standard.
Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Capacitance is measured with all pins on field-side and logic-side tied together.
Note 9: Devices are immersed in oil during surge characterization.

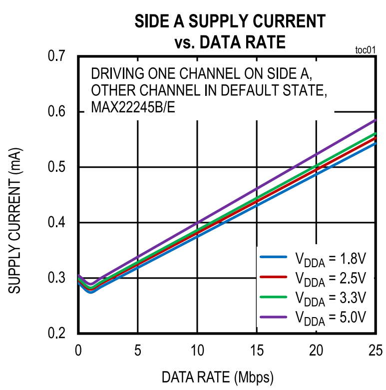
Safety Regulatory Approvals

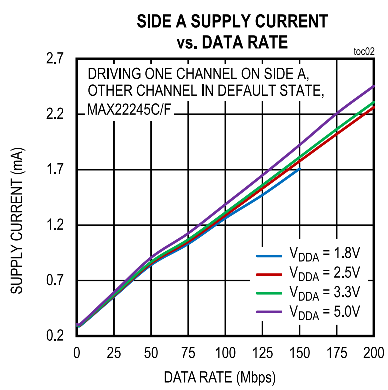
UL
The MAX22245/MAX22246 are certified under UL1577. For more details, refer to File E351759.
Rated up to 5000V_{RMS} isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22245/MAX22246 are certified up to 5000V_{RMS} for single protection. For more details, refer to File E351759.
VDE (Pending)
The MAX22245/MAX22246 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Transient Isolation Voltage 7000V_{PK}, Maximum Repetitive Peak Isolation Voltage 1200V_{PK}.

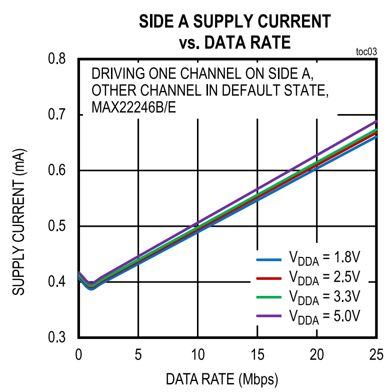
These couplers are suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

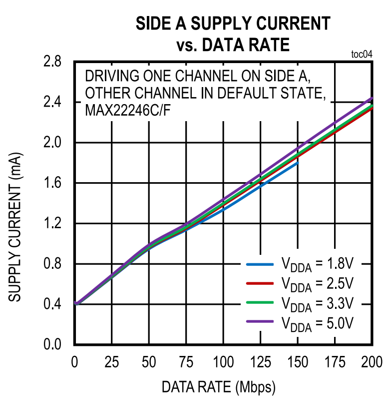
Typical Operating Characteristics

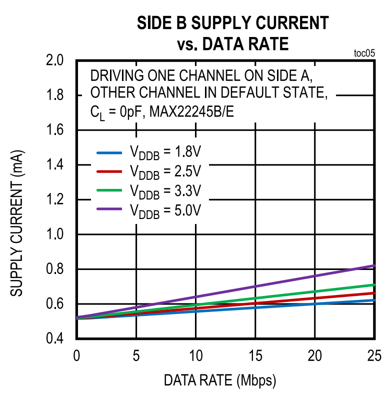
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

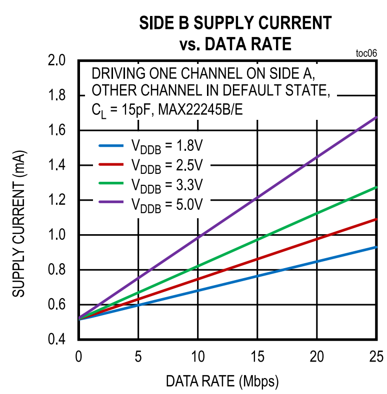




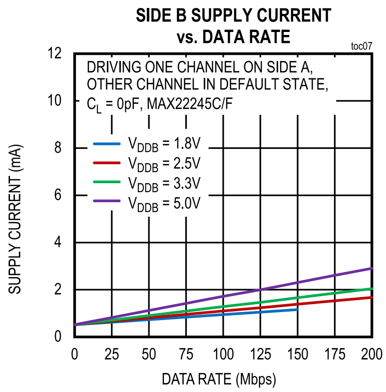


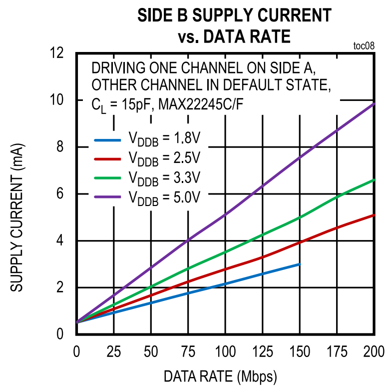


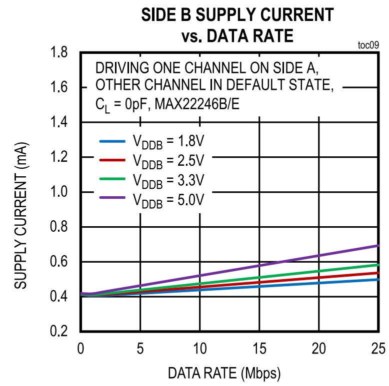


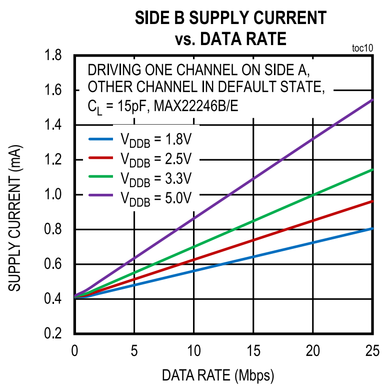


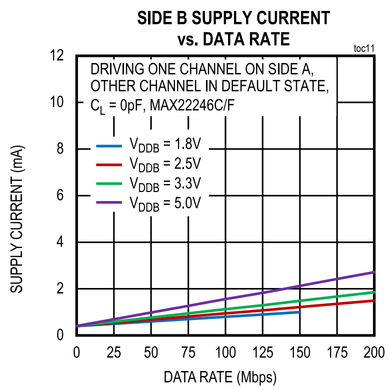
(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

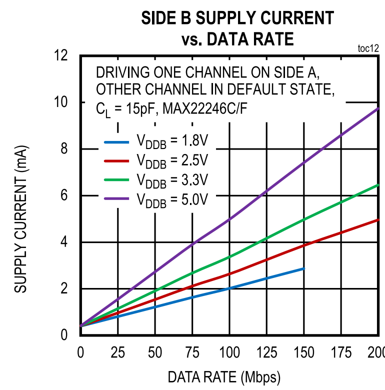


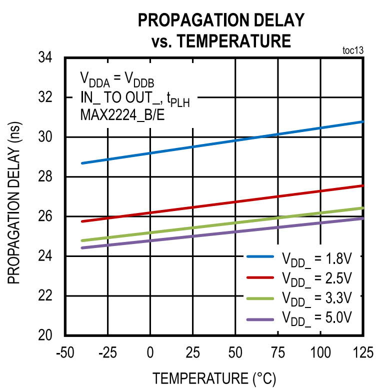


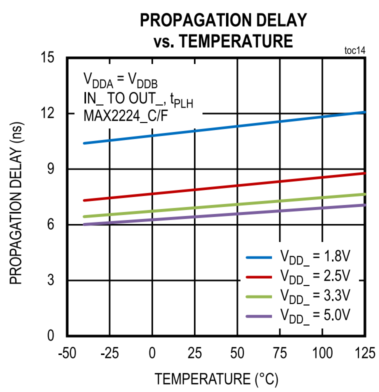


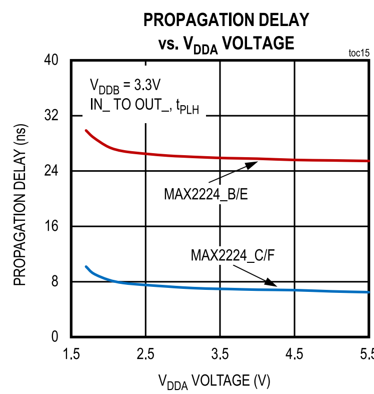






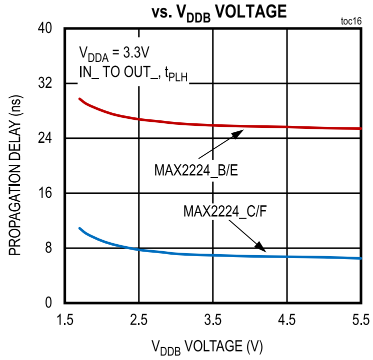




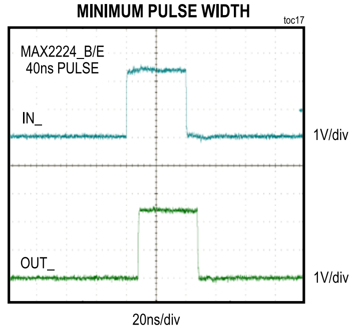


(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

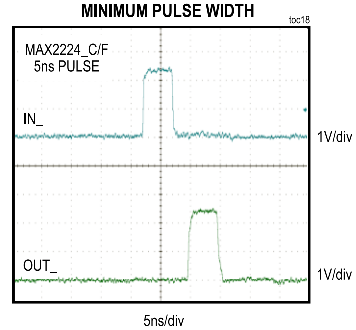
PROPAGATION DELAY vs. V_{DDB} VOLTAGE



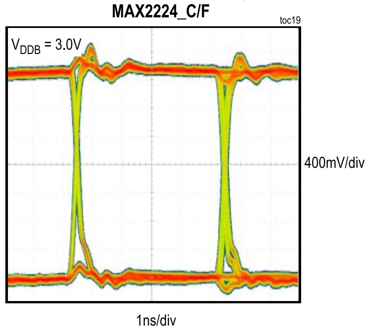
MINIMUM PULSE WIDTH



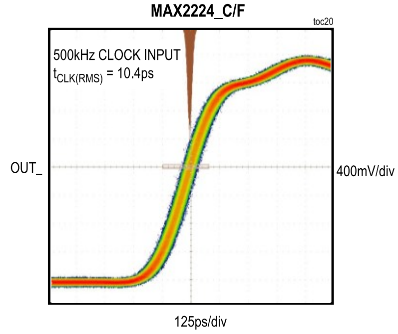
MINIMUM PULSE WIDTH



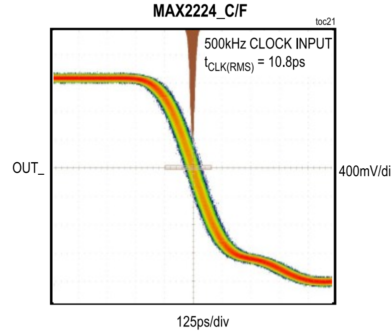
EYE DIAGRAM AT 200Mbps MAX2224_C/F



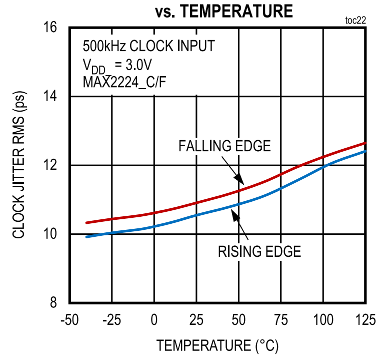
CLOCK JITTER RMS ON RISING EDGE MAX2224_C/F



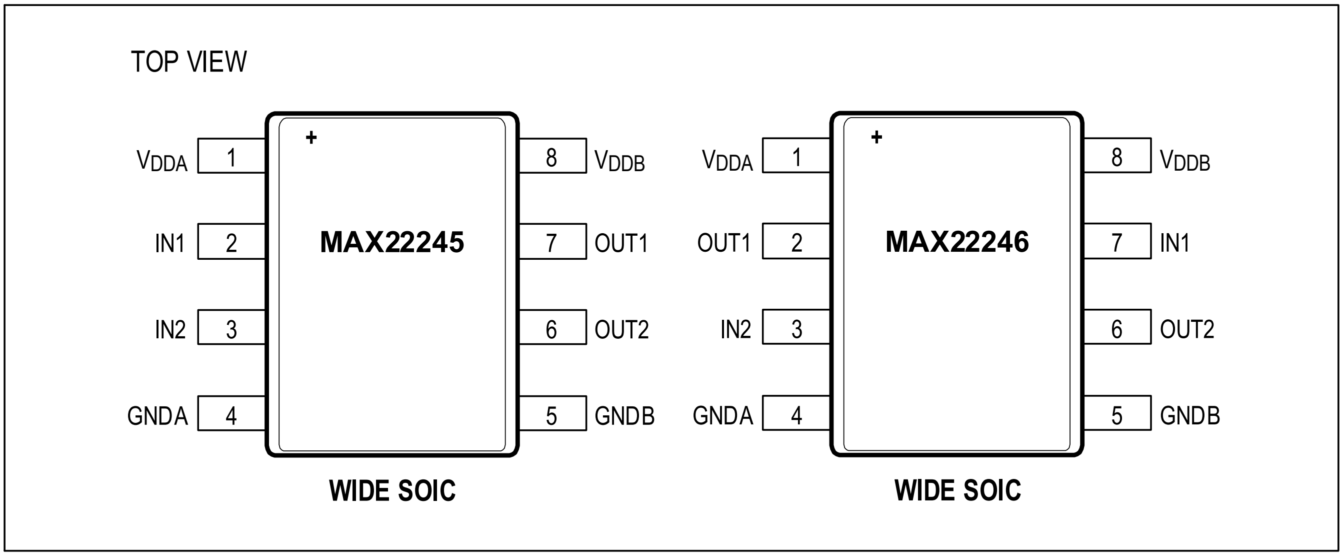
CLOCK JITTER RMS ON FALLING EDGE MAX2224_C/F



CLOCK JITTER RMS vs. TEMPERATURE



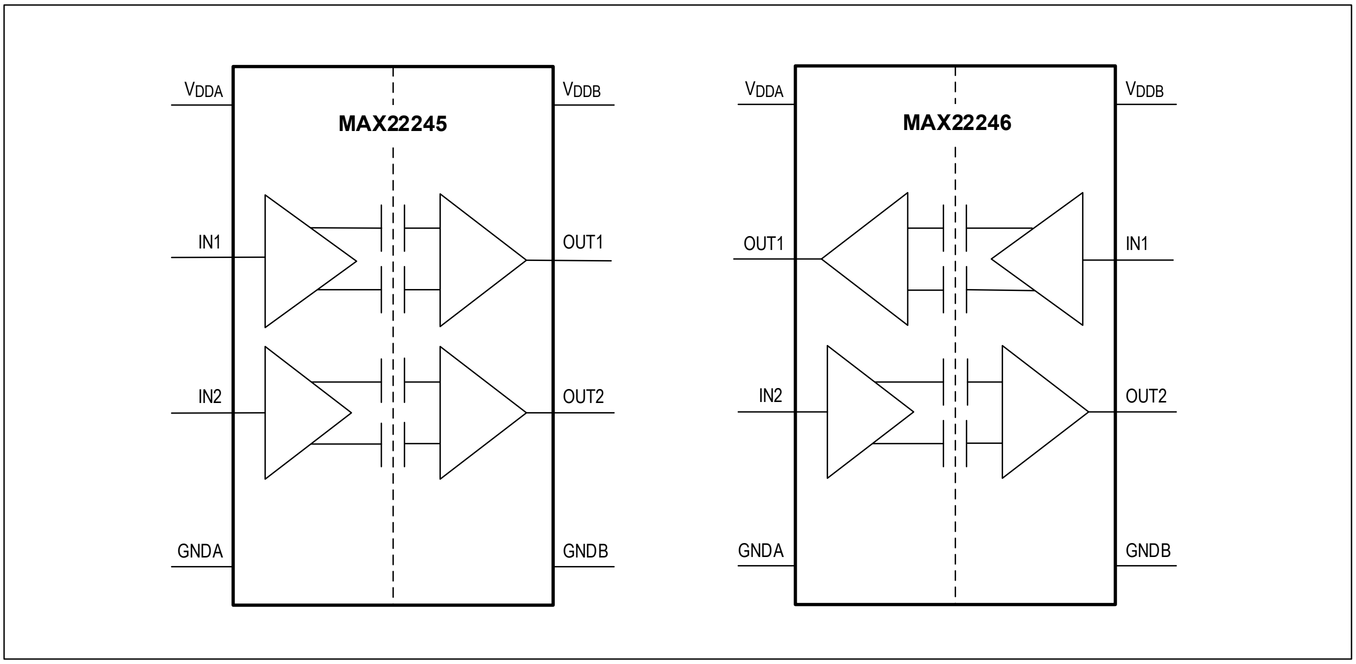
Pin Configurations



Pin Descriptions

PIN		NAME	FUNCTION
MAX22245	MAX22246		
1	1	V_{DDA}	Power Supply Input for Side A. Bypass V_{DDA} to GNDA with a 0.1μF ceramic capacitor as close as possible to the pin.
2	—	IN1	Logic Input 1 on Side A
—	2	OUT1	Logic Output 1 on Side A
3	3	IN2	Logic Input 2 on Side A
4	4	GNDA	Ground Reference for Side A
5	5	GNDB	Ground Reference for Side B
6	6	OUT2	Logic Output 2 on Side B
7	—	OUT1	Logic Output 1 on Side B
—	7	IN1	Logic Input 1 on Side B
8	8	V_{DDB}	Power Supply Input for Side B. Bypass V_{DDB} to GNDB with a 0.1μF ceramic capacitor as close as possible to the pin.

Functional Diagrams



Detailed Description

The MAX22245/MAX22246 are a family of 2-channel reinforced digital isolators. The MAX22245/MAX22246 have an isolation rating of $5kV_{RMS}$. The MAX22245/MAX22246 family offers two unidirectional channel configurations to accommodate any 2-channel design.

The MAX22245 features two channels transferring digital signals in one direction for applications such as isolated digital I/O. The MAX22246 has one channel to transmit data in one direction and the other channel to transmit in the opposite direction, making it ideal for applications such as isolated RS232 or RS485 communication.

Devices are available in an 8-pin wide-body SOIC package with 8mm creepage and clearance and are rated up to $5kV_{RMS}$. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Analog Devices' proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with a maximum data rate of either 25Mbps (B/E versions) or 200Mbps (C/F versions). The MAX2224_B/C feature default-high outputs. The MAX2224_E/F feature default-low outputs. The default is the state the output assumes when the input is not powered or if the input is open circuit. The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX22245/MAX22246 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX22245/MAX22246 provide reinforced galvanic isolation for digital signals that are transmitted between two ground domains. The devices withstand differences of up to $5kV_{RMS}$ for up to 60 seconds, and up to $1200V_{PEAK}$ of continuous isolation.

AEC-Q100 Qualification

Devices with /V suffix are AEC-Q100 qualified. Refer to the *Ordering Information* for all automotive grade part numbers.

Level Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX22245/MAX22246 to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX22245/MAX22246 is unidirectional; it only passes data in one direction, as indicated in the *Functional Diagrams*. Each device features two unidirectional channels that operate independently with guaranteed data rates from DC up to 25Mbps (B/E versions), or from DC to 200Mbps (C/F versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply, all outputs go to their default states regardless of the state of the inputs as seen in *Table 2*. *Figure 2* through *Figure 5* show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Condition

$V_{IN\_}$	V_{DDA}	V_{DDB}	V_{OUTA}	V_{OUTB}
1	Powered	Powered	High	High
0	Powered	Powered	Low	Low
X	Undervoltage	Powered	Default	Default
X	Powered	Undervoltage	Default	Default

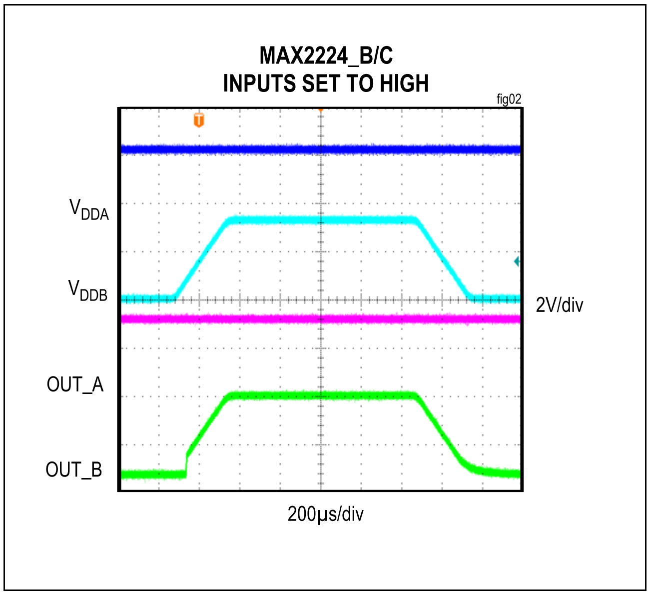


Figure 2. Undervoltage Lockout Behavior MAX2224_ B/C Input High

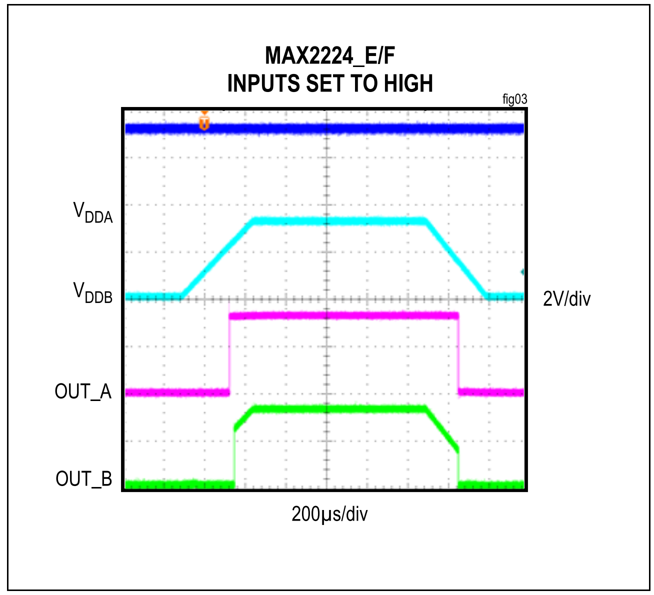


Figure 3. Undervoltage Lockout Behavior MAX2224_ E/F Input High

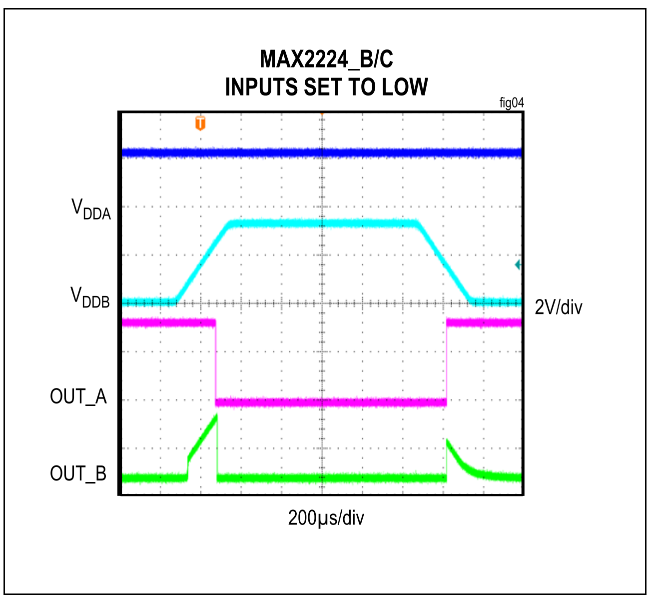


Figure 4. Undervoltage Lockout Behavior MAX2224_ B/C Input Low

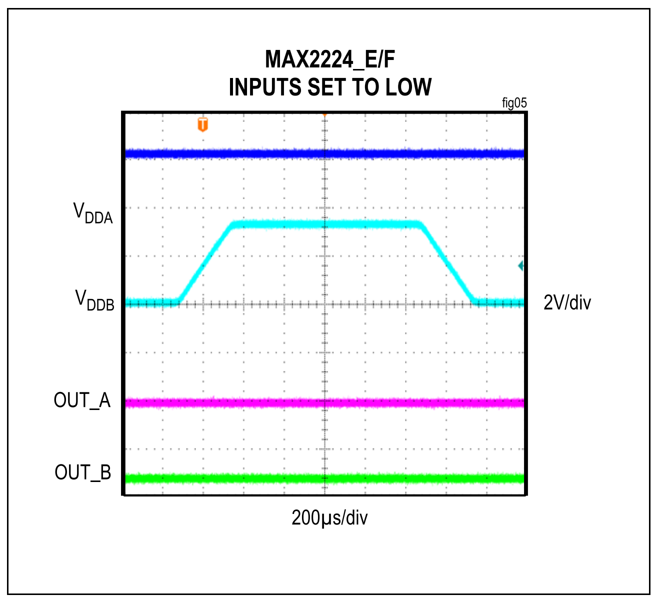


Figure 5. Undervoltage Lockout Behavior MAX2224_ E/F Input Low

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22245/MAX22246 can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. *Table 3* shows the safety limits for the MAX22245/MAX22246.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section and power dissipation calculations are discussed in the *Calculating Power Dissipation* section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 6 and *Figure 7* show the thermal derating curves for safety limiting the power and the current of the device. Ensure that the junction temperature does not exceed 150°C.

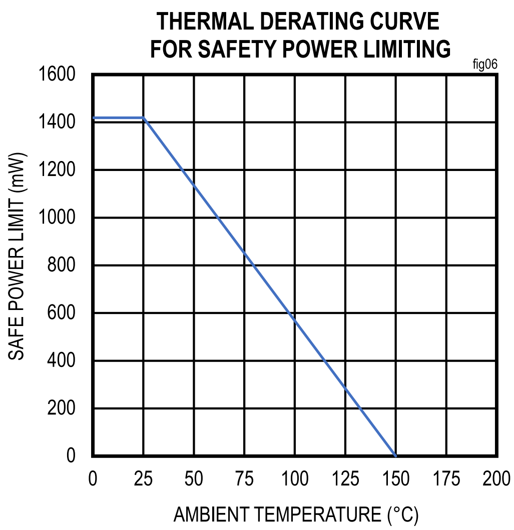


Figure 6. Thermal Derating Curve for Safety Power Limiting

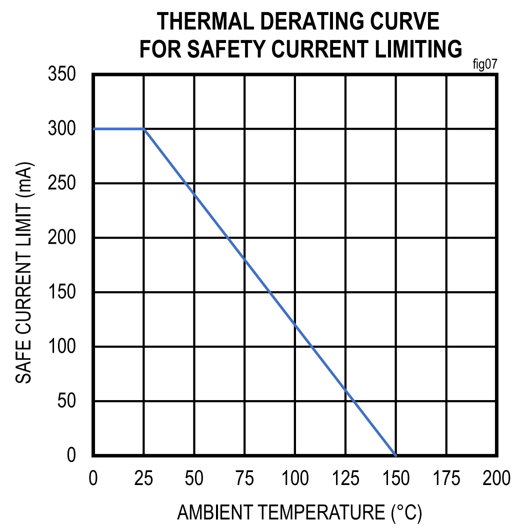


Figure 7. Thermal Derating Curve for Safety Current Limiting

Table 3. Safety Limiting Values for the MAX22245/MAX22246

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C	300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	1418	mW
Maximum Safety Temperature	T_S		150	°C

Applications Information

Power-Supply Sequencing

The MAX22245/MAX22246 do not require special power-supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power-supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX22245/MAX22246 free from ground and signal planes. Any galvanic or metallic connection between the Side A and Side B defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in *Figure 8* and *Figure 9*. Note that the data in *Figure 8* and *Figure 9* are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the no load current (shown in *Figure 8* and *Figure 9*), which is a function of voltage and data rate, and the load current, which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where:

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second/2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where:

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in *Figure 10*): A MAX22246C/F is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 100Mbps with a 15pF capacitive load, and channel 2 operating at 20Mbps and 50% duty cycle with a 10kΩ resistive load. See *Table 4* and *Table 5* for V_{DDA} and V_{DDB} supply-current calculation worksheets.

V_{DDA} must supply:

- Channel 1 is an output channel operating at 2.5V and 100Mbps, consuming 0.84mA, estimated from *Figure 9*.
- Channel 2 is an input channel operating at 2.5V and 20Mbps, consuming 0.35mA, estimated from *Figure 8*.
- I_{CL} on Channel 1 for 15pF capacitor at 2.5V and 100Mbps is 1.875mA.

Total current for side A = 0.84mA + 0.35mA + 1.875mA = 3.065mA (typ)

V_{DDB} must supply:

Channel 1 is an input channel operating at 3.3V and 100Mbps, consuming 1.16mA, estimated from *Figure 8*.

- Channel 2 is an output channel operating at 3.3V and 20Mbps, consuming 0.41mA, estimated from *Figure 9*.
- I_{RL} on Channel 2 for 10kΩ resistor switching at 50% duty cycle and at 3.3V is 0.165mA.

Total current for side B = 1.16mA + 0.41mA + 0.165mA = 1.735mA (typ)

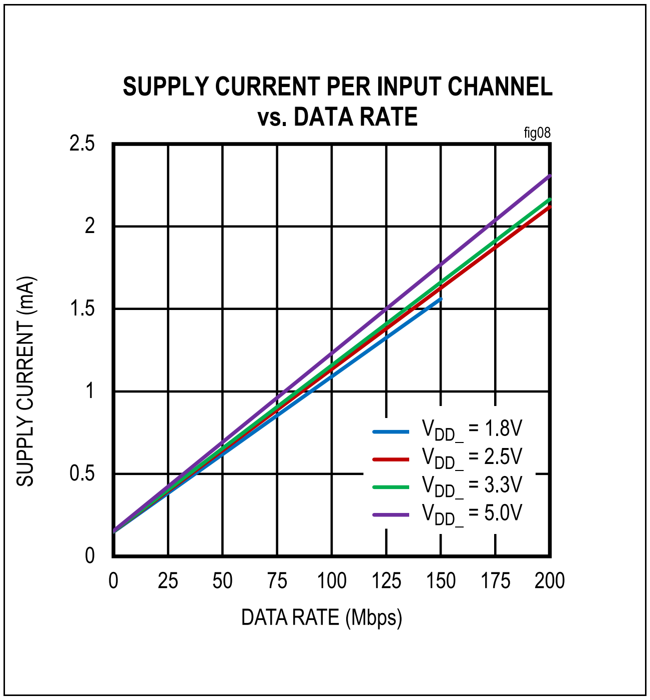


Figure 8. Supply Current per Input Channel (Estimated)

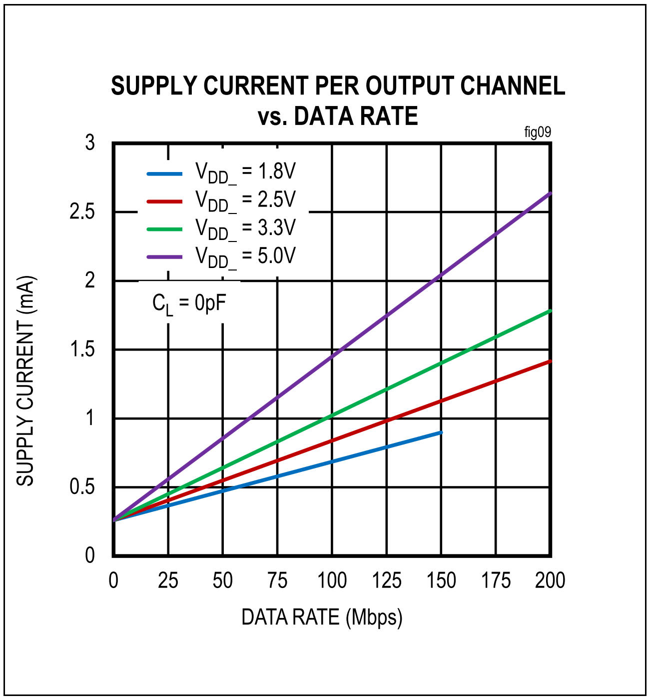


Figure 9. Supply Current per Output Channel (Estimated)

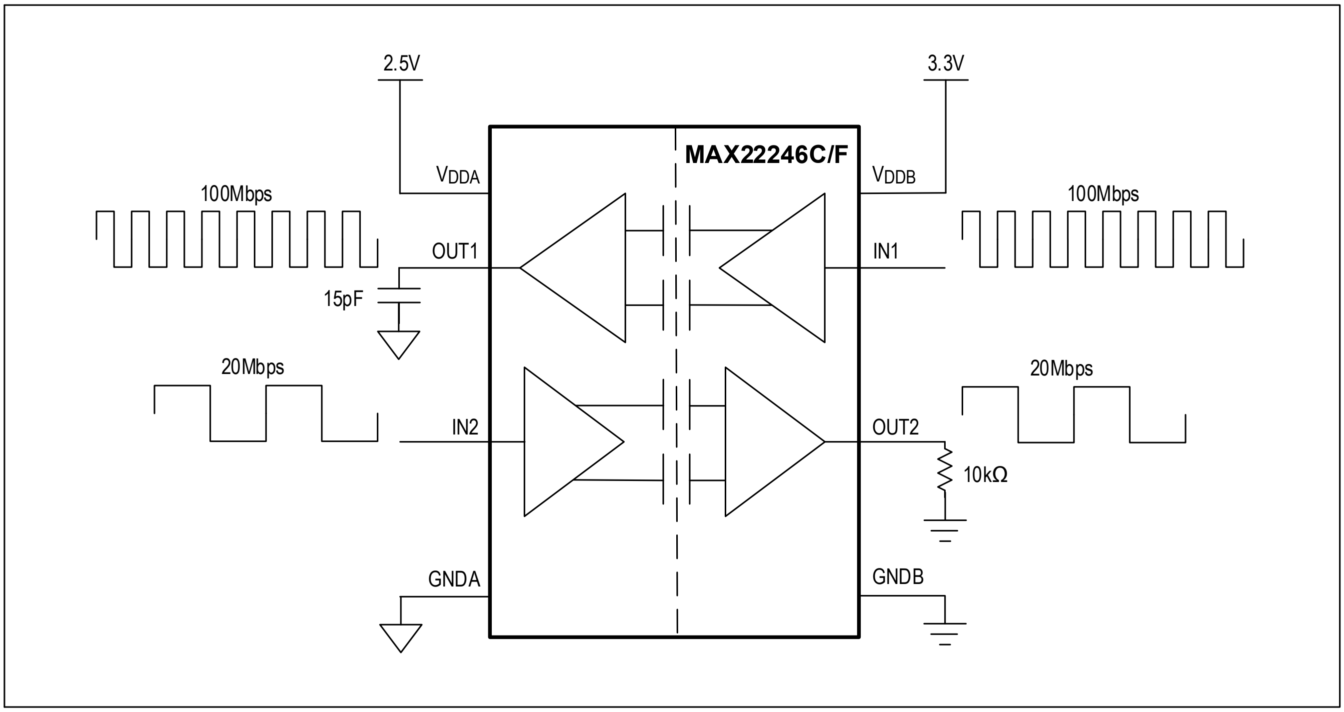


Figure 10. Example Circuit for Supply Current Calculation

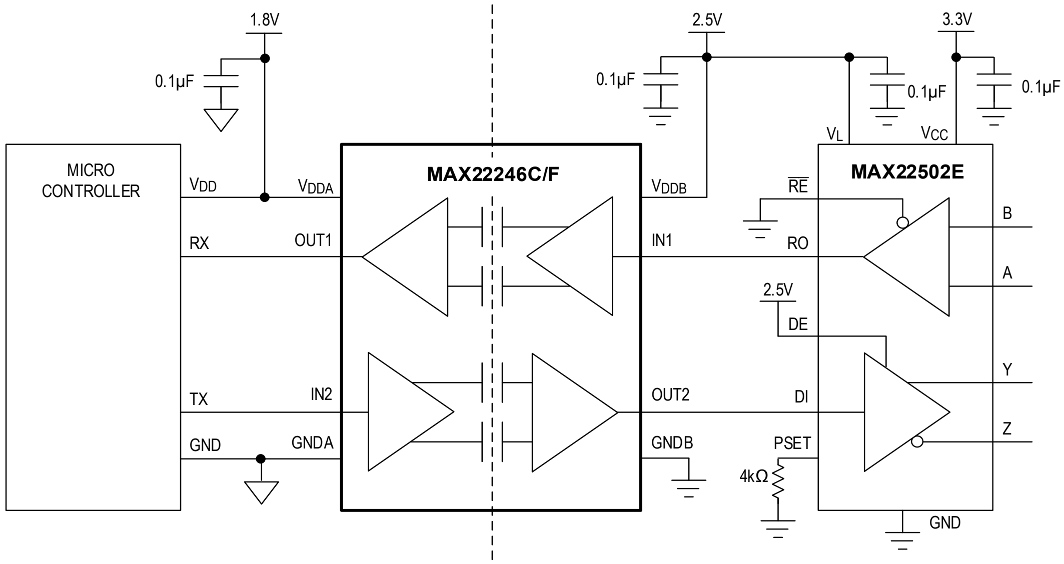
Table 4. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 2.5V					
CHANNEL	**IN/OUT**	**DATA RATE (Mbps)**	**LOAD TYPE**	**LOAD**	**NO LOAD CURRENT (mA)**	**LOAD CURRENT (mA)**
1	OUT	100	Capacitive	15pF	0.84	2.5V x 50MHz x 15pF = 1.875mA
2	IN	20			0.35	
Total: 3.065mA						

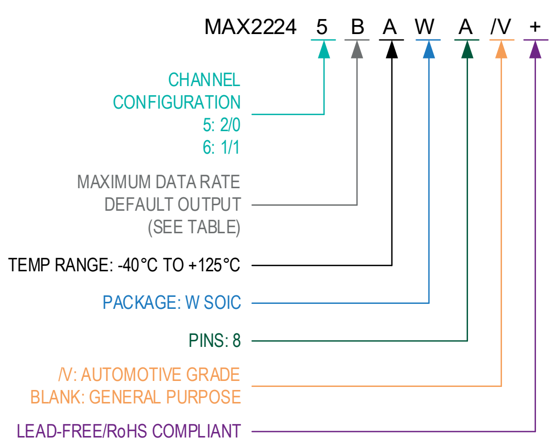
Table 5. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 3.3V					
CHANNEL	**IN/OUT**	**DATA RATE (Mbps)**	**LOAD TYPE**	**LOAD**	**NO LOAD CURRENT (mA)**	**LOAD CURRENT (mA)**
1	IN	100			1.16	
2	OUT	20	Resistive	10kΩ	0.41	3.3V / 10kΩ x 0.5 = 0.165mA
Total: 1.735mA						

Typical Application Circuits



Product Selector Guide



DEVICE CONFIGURATION	MAX DATA RATE	
	25Mbps	200Mbps
DEFAULT-HIGH OUTPUT	B	C
DEFAULT-LOW OUTPUT	E	F

Ordering Information

PART NUMBER	CHANNEL CONFIGURATION	DATA RATE (Mbps)	DEFAULT OUTPUT	ISOLATION VOLTAGE (kV_{RMS})	TEMPERATURE RANGE (°C)	PIN-PACKAGE
GENERAL PURPOSE DEVICES						
MAX22245BAWA+	2/0	25	High	5	-40 to +125	8 Wide SOIC
MAX22245CAWA+*	2/0	200	High	5	-40 to +125	8 Wide SOIC
MAX22245EAWA+*	2/0	25	Low	5	-40 to +125	8 Wide SOIC
MAX22245FAWA+	2/0	200	Low	5	-40 to +125	8 Wide SOIC
MAX22246BAWA+*	1/1	25	High	5	-40 to +125	8 Wide SOIC
MAX22246CAWA+	1/1	200	High	5	-40 to +125	8 Wide SOIC
MAX22246EAWA+*	1/1	25	Low	5	-40 to +125	8 Wide SOIC
MAX22246FAWA+	1/1	200	Low	5	-40 to +125	8 Wide SOIC
AUTOMOTIVE DEVICES						
MAX22245BAWA/V+*	2/0	25	High	5	-40 to +125	8 Wide SOIC
MAX22245CAWA/V+*	2/0	200	High	5	-40 to +125	8 Wide SOIC
MAX22245EAWA/V+*	2/0	25	Low	5	-40 to +125	8 Wide SOIC
MAX22245FAWA/V+	2/0	200	Low	5	-40 to +125	8 Wide SOIC
MAX22246BAWA/V+*	1/1	25	High	5	-40 to +125	8 Wide SOIC
MAX22246CAWA/V+	1/1	200	High	5	-40 to +125	8 Wide SOIC
MAX22246EAWA/V+*	1/1	25	Low	5	-40 to +125	8 Wide SOIC
MAX22246FAWA/V+*	1/1	200	Low	5	-40 to +125	8 Wide SOIC

**Future product—contact Analog Devices for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V Denotes an automotive qualified part.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/20	Initial release	—
1	9/20	Updated Dynamic Characteristics MAX2224_B/E, removed pending on UL certification	1, 5, 10
2	9/20	Removed future asterisk on the MAX22245FAWA+	21
3	12/20	Removed future asterisk on the MAX22245BAWA+, added future asterisk on the MAX22245FAWA+, updated Table 1 Insulation Characteristics and Note 6	9, 21
4	4/21	Added automotive-grade devices; updated front page; updated Package Information; moved Dynamic Characteristics MAX2224_C/F before Dynamic Characteristic MAX2224_B/E; added ESD Protection; updated Typical Operating Characteristics; added Functional Diagrams; updated Unidirectional Channels section; added AEC-Q100 Qualification section; updated Figure 6 and Table 3; updated Calculating Power Dissipation section; updated Figure 8, Figure 9, Table 4 and Table 5; updated Productor Selector Guide and Ordering Information	1-2, 4-7, 9-11, 13-14, 16-21
5	5/21	Updated Product Highlights; Updated Note 1; Updated Table 1 Insulation Characteristics; Updated Safety Regulatory Approvals; Updated Digital Isolation section	1, 7-9, 14
6	6/21	Updated Product Highlights; Updated CMTI test condition in Dynamic Characteristics MAX2224_C/F and Dynamic Characteristics MAX2224_B/E; Updated Product Selector Guide	1, 4, 5, 20
7	10/21	Added ESD Contact specification in *ESD Protection* table, removed future asterisk on the MAX22246FAWA+	7, 21
8	11/21	Updated global conditions in *ESD Protection* table, removed future asterisk on the MAX22246CAWA/V+ in the *Ordering Information*	7, 21
9	09/22	Removed future asterisk on the MAX22245FAWA+, MAX22245FAWA/V+ in the *Ordering Information*	21

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