



# 12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

MAX1420

## General Description

The MAX1420, 3.3V, 12-bit analog-to-digital converter (ADC) features a fully-differential input, pipelined, 12-stage ADC architecture with wideband track-and-hold (T/H) and digital error correction, incorporating a fully-differential signal path. The MAX1420 is optimized for low-power, high dynamic performance applications in imaging and digital communications. The converter operates from a single 3.3V supply, and consumes only 221mW. The fully-differential input stage has a small signal -3dB bandwidth of 400MHz and may be operated with single-ended inputs.

An internal 2.048V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure accommodates an internal reference, or externally applied buffered or unbuffered reference for applications that require increased accuracy and a different input voltage range.

In addition to low operating power, the MAX1420 features two power-down modes: reference power-down and shutdown mode. In reference power-down, the internal bandgap reference is deactivated, which results in a typical 2mA supply current reduction. A full shutdown mode is available to maximize power savings during idle periods.

The MAX1420 provides parallel, offset binary, CMOS-compatible three-state outputs.

The MAX1420 is available in a 7mm x 7mm x 1.4mm, 48-pin TQFP package, and is specified over the commercial (0°C to +70°C) and the extended industrial (-40°C to +85°C) temperature range.

Pin-compatible lower speed versions of the MAX1420 are also available. Please refer to the MAX1421 data sheet for 40Msps and the MAX1422 data sheet for 20Msps.

## Applications

- Medical Ultrasound Imaging
- CCD Pixel Processing
- IR Focal Plane Arrays
- Radar
- IF and Baseband Digitization

Functional diagram appears at end of data sheet.

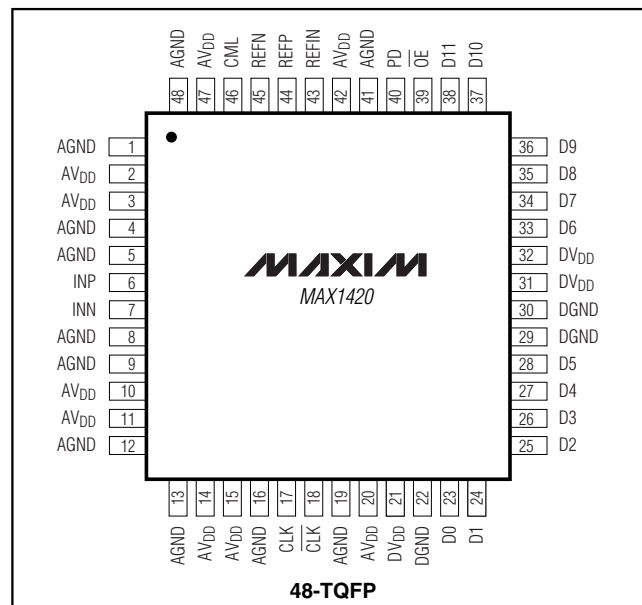
## Features

- ◆ 3.3V Single Power Supply
- ◆ 67dB SNR at  $f_{IN} = 5\text{MHz}$
- ◆ 66dB SNR at  $f_{IN} = 15\text{MHz}$
- ◆ Internal 2.048V Precision Bandgap Reference
- ◆ Differential, Wideband Input T/H Amplifier
- ◆ Power-Down Modes
  - 218mW (Reference Shutdown Mode)
  - 10 $\mu$ W (Shutdown Mode)
- ◆ Space-Saving 48-Pin TQFP Package

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1420CCM	0°C to +70°C	48 TQFP
MAX1420ECM	-40°C to +85°C	48 TQFP

## Pin Configuration



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## ABSOLUTE MAXIMUM RATINGS

AV <sub>DD</sub> , DV <sub>DD</sub> to AGND	-0.3V to +4V
DV <sub>DD</sub> , AV <sub>DD</sub> to DGND	-0.3V to +4V
DGND to AGND	-0.3V to +0.3V
INP, INN, REFP, REFN, REFIN, CML, CLK, CLK	(AGND - 0.3V) to (AV <sub>DD</sub> + 0.3V)
D0–D11, OE, PD	(DGND - 0.3V) to (DV <sub>DD</sub> + 0.3V)
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
48-Pin TQFP (derate 21.7mW/°C above +70°C)	1789mW

Operating Temperature Ranges	
MAX1420CCM	0°C to +70°C
MAX1420ECM	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>AVDD</sub> = V<sub>DVDD</sub> = 3.3V, AGND = DGND = 0, V<sub>IN</sub> = ±1.024V, differential input voltage at -0.5dBFS, internal reference, f<sub>CLK</sub> = 62.5MHz (50% duty cycle); digital output load C<sub>L</sub> = 10pF, ≥+25°C guaranteed by production test, <+25°C guaranteed by design and characterization. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution	RES			12		Bits
Differential Nonlinearity	DNL	T <sub>A</sub> = +25°C, no missing codes	-1		1	LSB
		T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		±0.5		
Integral Nonlinearity	INL	T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>		±2		LSB
Mid-scale Offset	MSO		-3	.75	3	%FSR
Mid-scale Offset Temperature Coefficient	MSOTC			3 x 10 <sup>-4</sup>		%/°C
Gain Error	GE	Internal reference (Note 1)	-5	±0.1	5	%FSR
		External reference applied to REFIN (Note 2)	-5	±0.2	5	
		External reference applied to REFP, CML, and REFN (Note 3)	-1.5		1.5	
Gain Error Temperature Coefficient	GETC	External reference applied to REFP, CML, and REFN (Note 3)		100 x 10 <sup>6</sup>		%/°C
<b>DYNAMIC PERFORMANCE</b> (f <sub>CLK</sub> = 60MHz, 4096-point FFT)						
Signal-to-Noise Ratio	SNR	f <sub>IN</sub> = 5MHz		67		dB
		f <sub>IN</sub> = 15MHz, T <sub>A</sub> = +25°C	62	66		
Spurious-Free Dynamic Range	SFDR	f <sub>IN</sub> = 5MHz		72		dBc
		f <sub>IN</sub> = 15MHz, T <sub>A</sub> = +25°C	64	72		
Total Harmonic Distortion	THD	f <sub>IN</sub> = 5MHz		-70		dBc
		f <sub>IN</sub> = 15MHz, T <sub>A</sub> = +25°C		-69	-62	
Signal-to-Noise and Distortion	SINAD	f <sub>IN</sub> = 5MHz		64.5		dB
		f <sub>IN</sub> = 15MHz, T <sub>A</sub> = +25°C	58.5	63		
Effective Number of Bits	ENOB	f <sub>IN</sub> = 5MHz		10.4		Bits
		f <sub>IN</sub> = 15MHz		10.2		
Two-Tone Intermodulation Distortion	IMD	f <sub>IN1</sub> = 11.566036MHz, f <sub>IN2</sub> = 13.4119138MHz (Note 4)		-74		dBc

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{AVDD} = V_{DVDD} = 3.3V$ ,  $AGND = DGND = 0$ ,  $V_{IN} = \pm 1.024V$ , differential input voltage at  $-0.5dBFS$ , internal reference,  $f_{CLK} = 62.5MHz$  (50% duty cycle); digital output load  $C_L = 10pF$ ,  $\geq +25^\circ C$  guaranteed by production test,  $< +25^\circ C$  guaranteed by design and characterization. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Gain	DG			$\pm 1$		%
Differential Phase	DP			$\pm 0.25$		Degrees
<b>ANALOG INPUTS</b> (INP, INN, CML)						
Input Resistance	$R_{IN}$	Either input to ground		22		$k\Omega$
Input Capacitance	$C_{IN}$	Either input to ground		4		pF
Common-Mode Input Level (Note 5)	$V_{CML}$			$V_{AVDD} \times 0.5$		V
Common-Mode Input Voltage Range (Note 5)	$V_{CMVR}$			$V_{CML} \pm 5\%$		V
Differential Input Range	$V_{IN}$	$V_{INP} - V_{INN}$ (Note 6)		$\pm V_{DIFF}$		V
Small-Signal Bandwidth	$BW_{-3dB}$	(Note 7)		400		MHz
Large-Signal Bandwidth	$FPBW_{-3dB}$	(Note 7)		150		MHz
Overvoltage Recovery	OVR	$1.5 \times FS$ input		1		Clock cycles
<b>INTERNAL REFERENCE</b> (REFIN bypassed with $0.22\mu F$ in parallel with $1nF$ )						
Common-Mode Reference Voltage	$V_{CML}$	At CML		$V_{AVDD} - 0.5$		V
Positive Reference Voltage	$V_{REFP}$	At REFP		$V_{CML} + 0.512$		V
Negative Reference Voltage	$V_{REFN}$	At REFN		$V_{CML} - 0.512$		V
Differential Reference Voltage	$V_{DIFF}$	(Note 6)		$1.024 \pm 5\%$		V
Differential Reference Temperature Coefficient	REFTC			$\pm 100$		ppm/ $^\circ C$
<b>EXTERNAL REFERENCE</b> ( $V_{REFIN} = 2.048V$ )						
REFIN Input Resistance	$R_{IN}$	(Note 8)	5			$k\Omega$
REFIN Input Capacitance	$C_{IN}$			10		pF
REFIN Reference Input Voltage	$V_{REFIN}$			$2.048 \pm 10\%$		V
Differential Reference Voltage	$V_{DIFF}$	(Note 6)	$0.92 \times V_{REFIN}/2$	$V_{REFIN}/2$	$1.08 \times V_{REFIN}/2$	V
<b>EXTERNAL REFERENCE</b> ( $V_{REFIN} = 0$ , reference voltage applied to REFP, REFN, and CML)						
REFP, REFN, CML Input Current	$I_{IN}$		-200		200	$\mu A$
REFP, REFN, CML Input Capacitance	$C_{IN}$			15		pF

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( $V_{AVDD} = V_{DVDD} = 3.3V$ ,  $AGND = DGND = 0$ ,  $V_{IN} = \pm 1.024V$ , differential input voltage at  $-0.5dBFS$ , internal reference,  $f_{CLK} = 62.5MHz$  (50% duty cycle); digital output load  $C_L = 10pF$ ,  $\geq +25^\circ C$  guaranteed by production test,  $< +25^\circ C$  guaranteed by design and characterization. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Reference Voltage Range	$V_{DIFF}$	(Note 6)		1.024 $\pm 10\%$		V
CML Input Voltage Range	$V_{CML}$			1.65 $\pm 10\%$		V
REFP Input Voltage Range	$V_{REFP}$			$V_{CML} + V_{DIFF}/2$		V
REFN Input Voltage Range	$V_{REFN}$			$V_{CML} - V_{DIFF}/2$		V
<b>DIGITAL INPUTS</b> (CLK, $\overline{CLK}$ , PD, OE)						
Input Logic High	$V_{IH}$		0.7 x $V_{DVDD}$			V
Input Logic Low	$V_{IL}$				0.3 x $V_{DVDD}$	V
Input Current		CLK, $\overline{CLK}$		$\pm 330$		$\mu A$
		PD	-20		20	
		OE	-20		20	
Input Capacitance				10		pF
<b>DIGITAL OUTPUTS</b> (D0–D11)						
Output Logic High	$V_{OH}$	$I_{OH} = 200\mu A$	$V_{DVDD} - 0.5$		$V_{DVDD}$	V
Output Logic Low	$V_{OL}$	$I_{OL} = -200\mu A$	0		0.5	V
Three-State Leakage			-10		10	$\mu A$
Three-State Capacitance				2		pF
<b>POWER REQUIREMENTS</b>						
Analog Supply Voltage	$V_{AVDD}$		3.135	3.3	3.465	V
Digital Supply Voltage	$V_{DVDD}$		2.7	3.3	3.63	V
Analog Supply Current	$I_{AVDD}$			67	78	mA
Analog Supply Current with Internal Reference in Shutdown		$V_{REFIN} = 0$		66	76	mA
Analog Shutdown Current		PD = $D_{VDD}$		10	20	$\mu A$
Digital Supply Current	$I_{DVDD}$			8		mA
Digital Shutdown Current		PD = $V_{DVDD}$			20	$\mu A$
Power Dissipation	$P_{DISS}$	Analog power dissipation		221	258	mW

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Dissipation In Shutdown	PD <sub>ISS</sub>	PD = VD <sub>VDD</sub>		10		μW
Power-Supply Rejection Ratio	PSRR	(Note 9)		±1		mV/V
<b>TIMING CHARACTERISTICS</b>						
Maximum Clock Frequency	f <sub>CLK</sub>		60			MHz
Clock High	t <sub>CH</sub>	Figure 6, clock period 16.667ns		8.33		ns
Clock Low	t <sub>CL</sub>	Figure 6, clock period 16.667ns		8.33		ns
Pipeline Delay (Latency)		Figure 6		7		Clock cycles
Aperture Delay	t <sub>AD</sub>	Figure 10		2		ns
Aperture Jitter	t <sub>AJ</sub>	Figure 10		2		ps
Data Output Delay	t <sub>OD</sub>	Figure 6	5	10	14	ns
Bus Enable Time	t <sub>BE</sub>	Figure 5		5		ns
Bus Disable Time	t <sub>BD</sub>	Figure 5		5		ns

**Note 1:** Internal reference, REFIN bypassed to AGND with a combination of 0.22μF in parallel with 1nF capacitor.

**Note 2:** External 2.048V reference applied to REFIN.

**Note 3:** Internal reference disabled.  $V_{REFIN} = 0$ ,  $V_{REFP} = 2.162V$ ,  $V_{CML} = 1.65V$ , and  $V_{REFN} = 1.138V$ .

**Note 4:** IMD is measured with respect to either of the fundamental tones.

**Note 5:** Specifies the common-mode range of the differential input signal supplied to the MAX1420.

**Note 6:**  $V_{DIFF} = V_{REFP} - V_{REFN}$ .

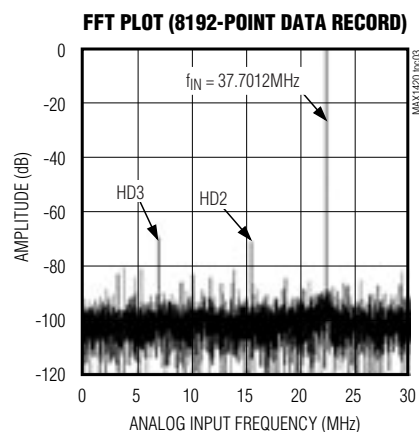
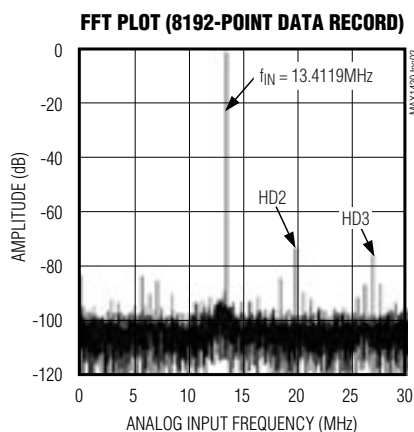
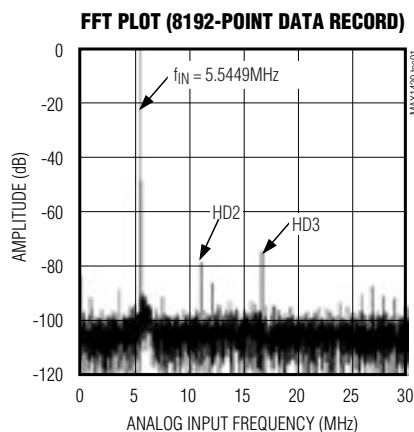
**Note 7:** Input bandwidth is measured at a  $-3dB$  level.

**Note 8:**  $V_{REFIN}$  is internally biased to 2.048V through a 10kΩ resistor.

**Note 9:** Measured as the ratio of the change in mid-scale offset voltage for a  $\pm 5\%$  change in  $V_{AVDD}$ , using the internal reference.

## Typical Operating Characteristics

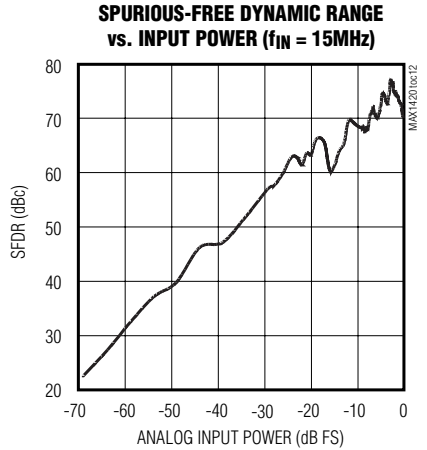
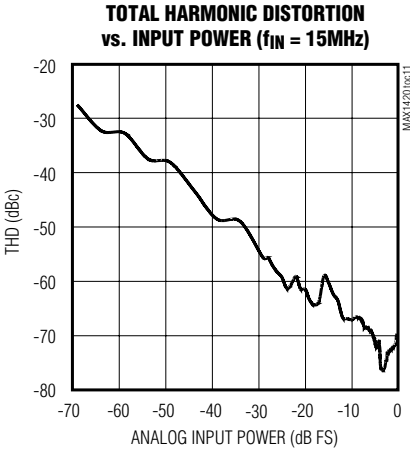
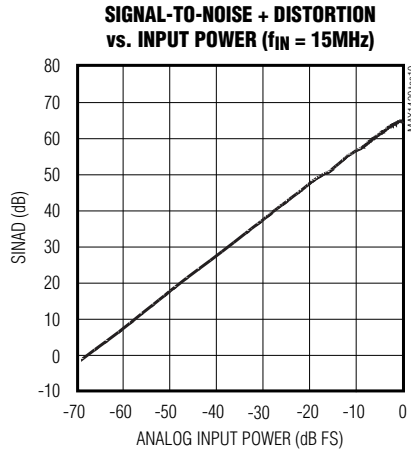
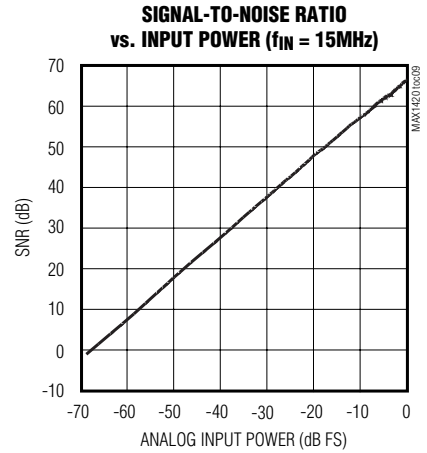
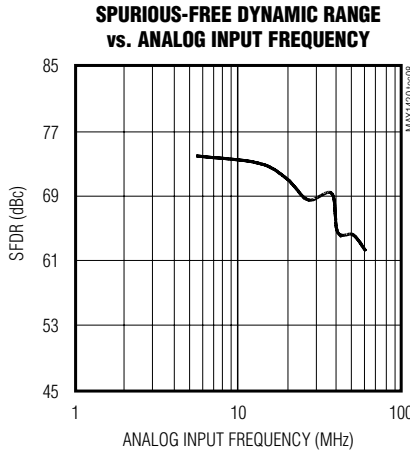
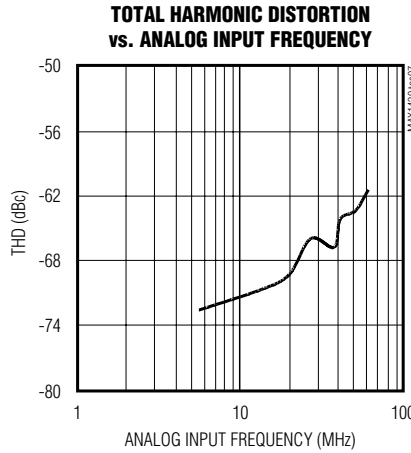
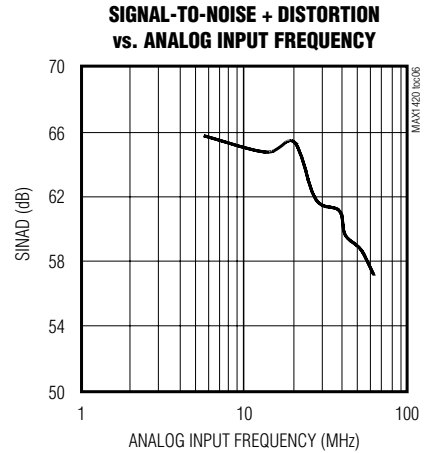
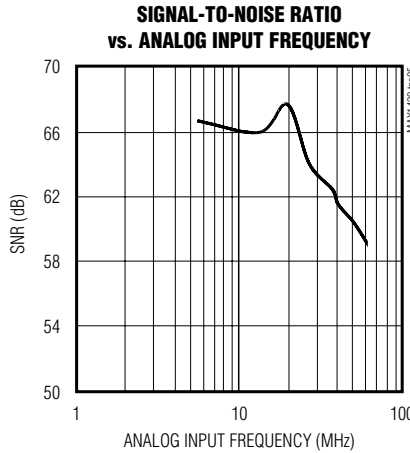
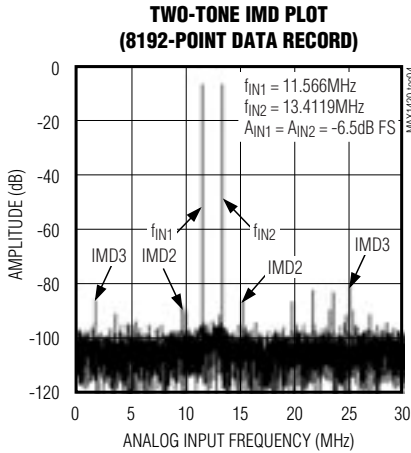
( $V_{AVDD} = V_{DVDD} = 3.3V$ ,  $AGND = DGND = 0$ ,  $V_{IN} = \pm 1.024V$ , differential input drive,  $A_{IN} = -0.5dBFS$ ,  $f_{CLK} = 60.006MHz$  (50% duty cycle), digital output load  $C_L = 10pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)



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## Typical Operating Characteristics (continued)

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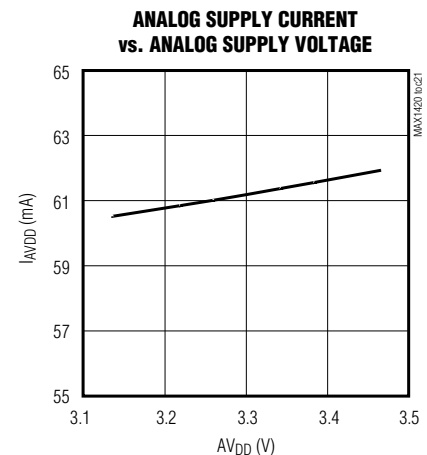
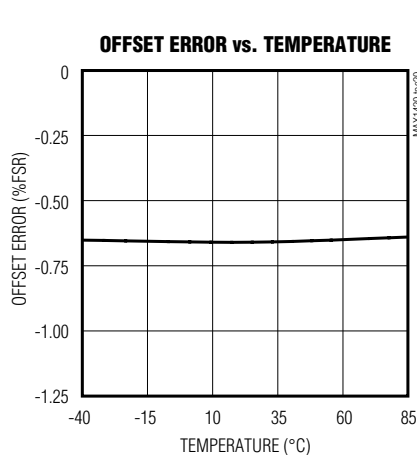
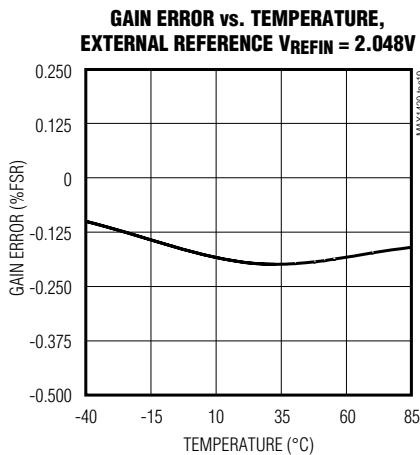
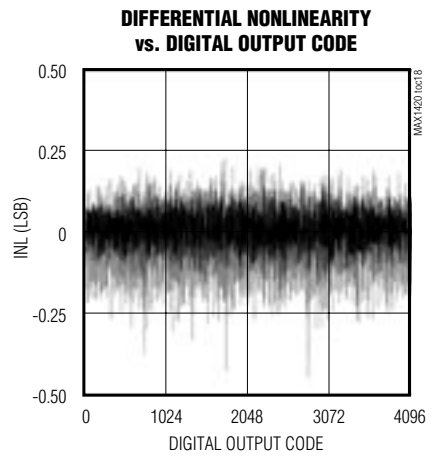
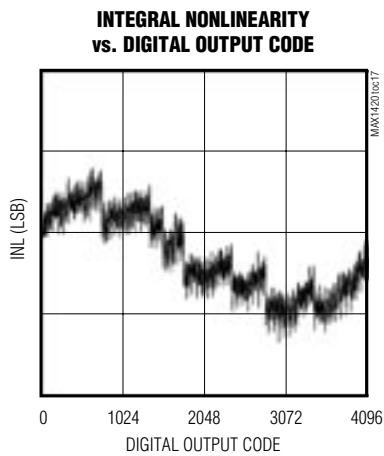
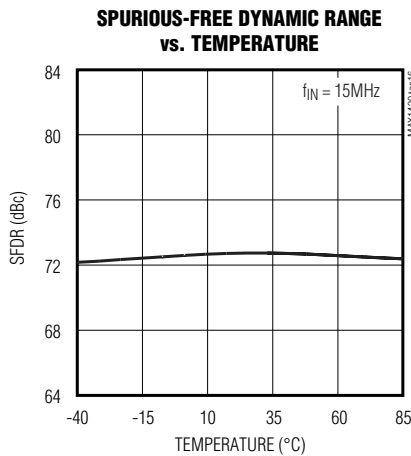
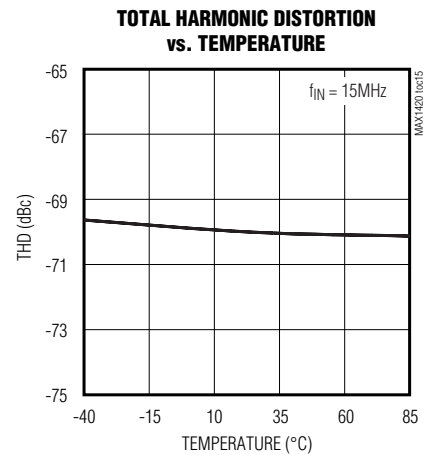
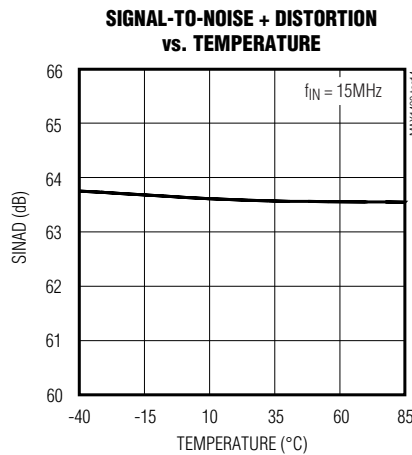
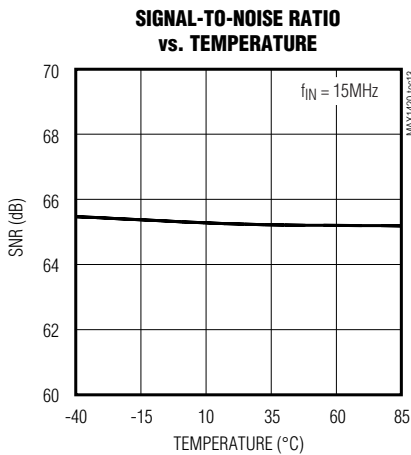


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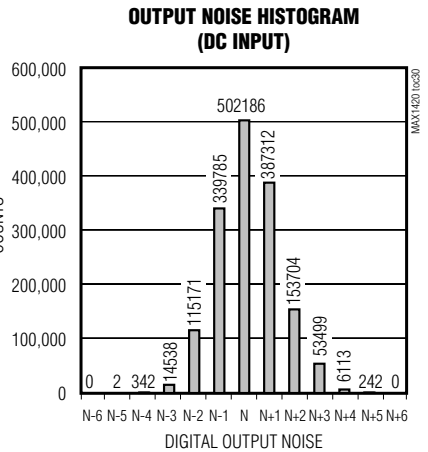
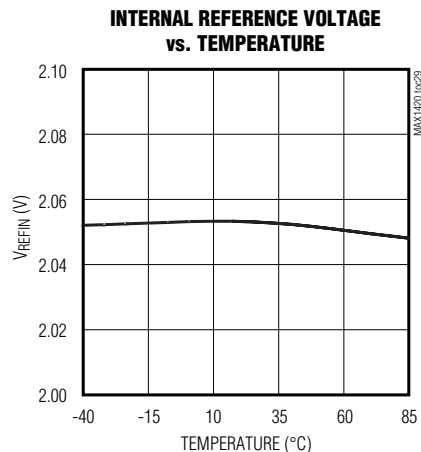
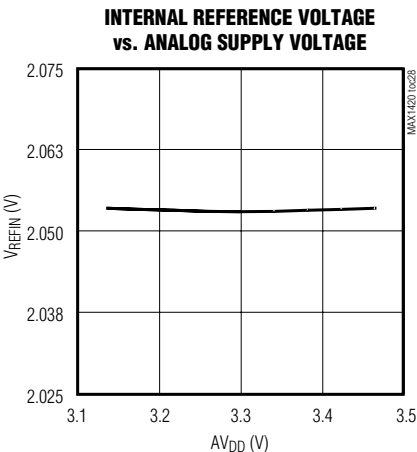
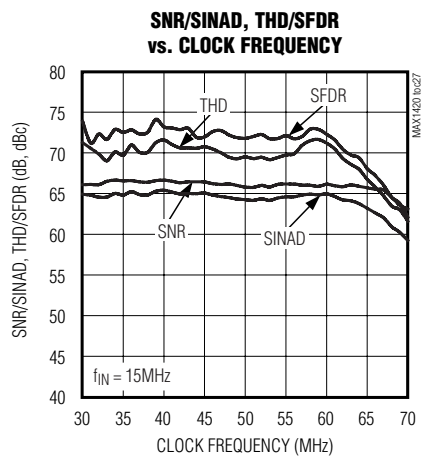
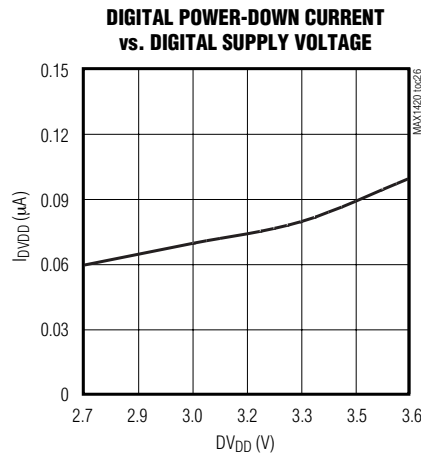
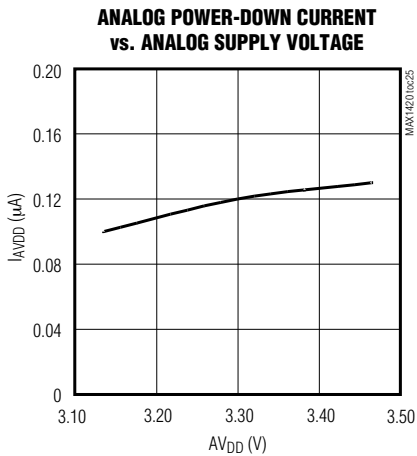
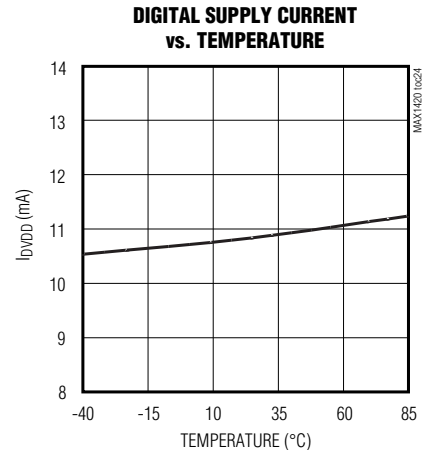
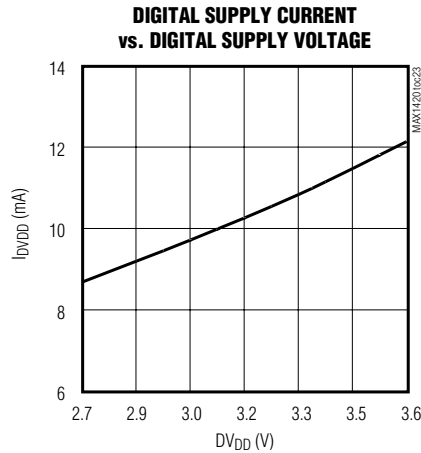
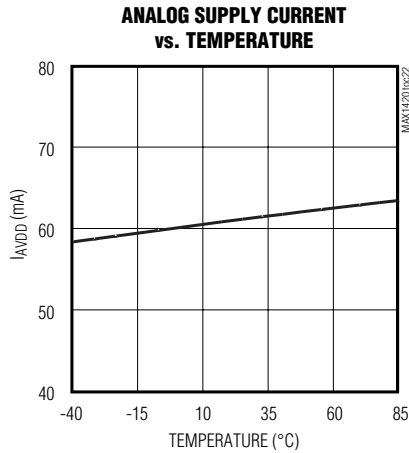
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## Typical Operating Characteristics (continued)

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## Pin Description

**MAX1420**

PIN	NAME	FUNCTION
1, 4, 5, 8, 9, 12, 13, 16, 19, 41, 48	AGND	Analog Ground. Connect all return paths for analog signals to AGND.
2, 3, 10, 11, 14, 15, 20, 42, 47	AVDD	Analog Supply Voltage. For optimum performance, bypass to the closest AGND with a parallel combination of a 0.1 $\mu$ F and a 1nF capacitor. Connect a single 10 $\mu$ F and 1 $\mu$ F capacitor combination between AVDD and AGND.
6	INP	Positive Analog Signal Input
7	INN	Negative Analog Signal Input
17	CLK	Clock Frequency Input. Clock frequency input ranges from 100kHz to 60MHz.
18	$\overline{\text{CLK}}$	Complementary Clock Frequency Input. This input is used for differential clock inputs. If the ADC is driven with a single-ended clock, bypass $\overline{\text{CLK}}$ with a 0.1 $\mu$ F capacitor to AGND.
21, 31, 32	DVDD	Digital Supply Voltage. For optimum performance, bypass to the closest DGND with a parallel combination of a 0.1 $\mu$ F and a 1nF capacitor. Connect a single 10 $\mu$ F and 1 $\mu$ F capacitor combination between DVDD and DGND.
22, 29, 30	DGND	Digital Ground
23–28	D0–D5	Digital Data Outputs. Data bits D0 through D5, where D0 represents the LSB.
33–38	D6–D11	Digital Data Outputs. D6 through D11, where D11 represents the MSB.
39	$\overline{\text{OE}}$	Output Enable Input. A logic “1” on $\overline{\text{OE}}$ places the outputs D0–D11 into a high-impedance state. A logic “0” allows for the data bits to be read from the outputs.
40	PD	Shutdown Input. A logic “1” on PD places the ADC into shutdown mode.
43	REFIN	External Reference Input. Bypass to AGND with a capacitor combination of 0.22 $\mu$ F in parallel with 1nF. REFIN can be biased externally to adjust reference levels and calibrate full-scale errors. To disable the internal reference, connect REFIN to AGND.
44	REFP	Positive Reference I/O. Bypass to AGND with a capacitor combination of 0.22 $\mu$ F in parallel with 1nF. With the internal reference disabled (REFIN = AGND), REFP should be biased to $V_{\text{CML}} + V_{\text{DIFF}} / 2$ .
45	REFN	Negative Reference I/O. Bypass to AGND with a capacitor combination of 0.22 $\mu$ F in parallel with 1nF. With the internal reference disabled (REFIN = AGND), REFN should be biased to $V_{\text{CML}} - V_{\text{DIFF}} / 2$ .
46	CML	Common-Mode Level Input. Bypass to AGND with a capacitor combination of 0.22 $\mu$ F in parallel with 1nF.

# 12-Bit, 60Mps, 3.3V, Low-Power ADC with Internal Reference

## Detailed Description

The MAX1420 uses a 12-stage, fully-differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Each sample moves through a pipeline stage every half-clock cycle, including the delay through the output latch. The latency is seven clock cycles.

A 2-bit (2-comparator) flash ADC converts the held-input voltage into a digital code. The following digital-to-analog converter (DAC) converts the digitized result back into an analog voltage, which is then subtracted from the original held-input signal. The resulting error signal is then multiplied by two, and the product is passed along to the next pipeline stage. This process is repeated until the signal has been processed by all 12 stages. Each stage provides a 1-bit resolution. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes.

## Input Track-and-Hold Circuit

Figure 2 displays a simplified functional diagram of the input track-and-hold (T/H) circuit in both track-and-hold mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully-differential circuit passes the input signal to the two capacitors C2a and C2b through switches S4a and S4b. Switches S2a and S2b set the common mode for the operational transcon-

ductance amplifier (OTA) input, and open simultaneously with S1, sampling the input waveform. The resulting differential voltage is held on capacitors C2a and C2b. Switches S4a and S4b are then opened before S3a, S3b, S4c are closed. The OTA is used to charge capacitors C1a and C1b to the same values originally held on C2a and C2b. This value is then presented to the first stage quantizer and isolates the pipeline from the fast-changing input. The wide input bandwidth T/H amplifier allows the MAX1420 to track and sample/hold analog inputs of high frequencies beyond Nyquist. The analog inputs INP to INN can be driven either differentially or single-ended. Match the impedance of INP and INN and set the common-mode voltage to midsupply ( $AV_{DD}/2$ ) for optimum performance.

## Analog Input and Reference Configuration

The full-scale range of the MAX1420 is determined by the internally generated voltage difference between REFP ( $AV_{DD}/2 + V_{REFIN}/4$ ) and REFN ( $AV_{DD}/2 - V_{REFIN}/4$ ). The MAX1420's full-scale range is adjustable through REFIN, which provides high input impedance for this purpose. REFP, CML ( $AV_{DD}/2$ ), and REFN are internally buffered low impedance outputs.

An internal 2.048V precision bandgap reference sets the full-scale range of the ADC. A flexible reference structure accommodates an internal reference, or externally applied buffered or unbuffered reference, for appli-

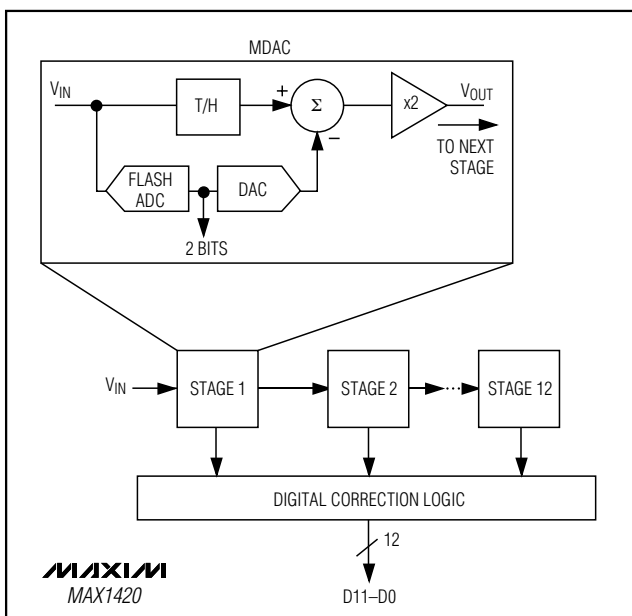


Figure 1. Pipelined Architecture—Stage Blocks

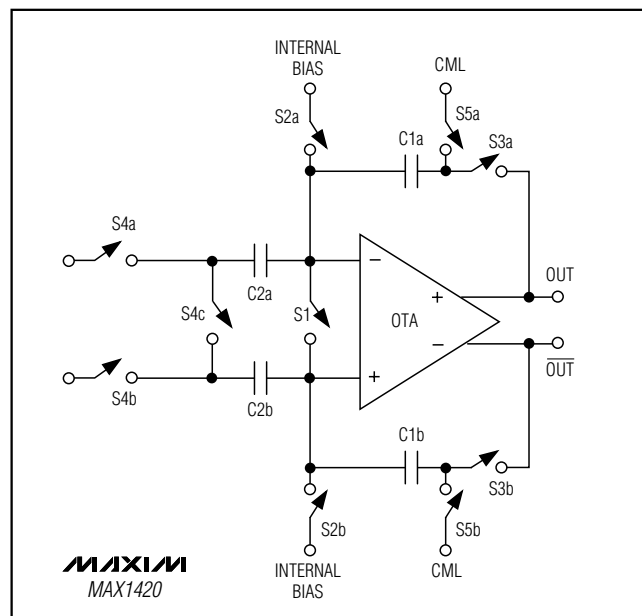


Figure 2. Internal Track-and-Hold Circuit

# 12-Bit, 60MSPS, 3.3V, Low-Power ADC with Internal Reference

**MAX1420**

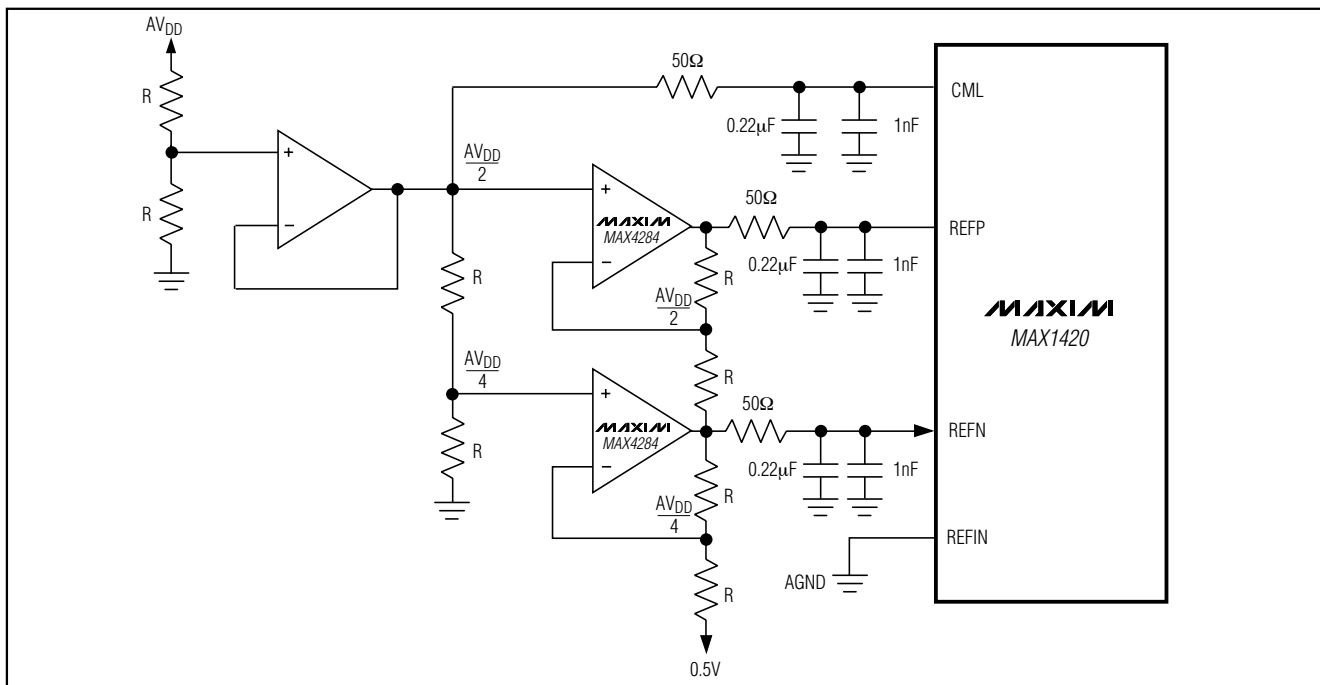


Figure 3. Unbuffered External Reference Drive—Internal Reference Disabled

cations that require increased accuracy and a different input voltage range.

The MAX1420 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, the on-chip 2.048V bandgap reference is active and REF<sub>IN</sub>, REF<sub>P</sub>, CML, and REF<sub>N</sub> are left floating. For stability purposes, bypass REF<sub>IN</sub>, REF<sub>P</sub>, REF<sub>N</sub> and CML with a capacitor network of 0.22μF in parallel with a 1nF capacitor to AGND.

In buffered external reference mode, the reference voltage levels can be adjusted externally by applying a stable and accurate voltage at REF<sub>IN</sub>.

In unbuffered external reference mode, REF<sub>IN</sub> is connected to AGND, thereby deactivating the on-chip buffers of REF<sub>P</sub>, CML, and REF<sub>N</sub>. With their buffers shut down, these nodes become high impedance and can be driven by external reference sources, as shown in Figure 3.

## Clock Inputs (CLK, $\overline{\text{CLK}}$ )

The MAX1420's CLK and  $\overline{\text{CLK}}$  inputs accept both differential and single-ended input operation and accept CMOS-compatible clock signals. If CLK is driven with a single-ended clock signal, bypass  $\overline{\text{CLK}}$  with a 0.1μF capacitor to AGND. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (< 2ns). Sampling occurs on the rising edge of the clock signal, requiring this edge to have the lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the ADC according to the following relationship:

$$\text{SNR}_{\text{dB}} = 20 \times \log_{10} \frac{1}{2\pi \times f_{\text{IN}} \times t_{\text{AJ}}}$$

where  $f_{\text{IN}}$  represents the analog input frequency and  $t_{\text{AJ}}$  is the aperture jitter. Clock jitter is especially critical for high input frequency applications. The clock input should always be considered as an analog signal and routed away from any analog or digital signal lines.

The MAX1420 clock input operates with a voltage threshold set to  $\text{AV}_{\text{DD}}/2$ . Clock inputs must meet the specifications for high and low periods as stated in the *Electrical Characteristics*.

# 12-Bit, 60Mps, 3.3V, Low-Power ADC with Internal Reference

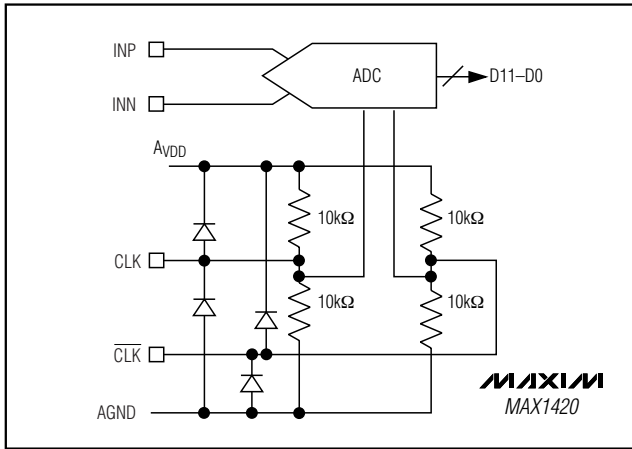


Figure 4. Simplified Clock Input Circuit

Figure 4 shows a simplified model of the clock input circuit. This circuit consists of two 10kΩ resistors to bias the common-mode level of each input. This circuit may be used to AC-couple the system clock signal to the MAX1420 clock input.

### Output Enable ( $\overline{OE}$ ), Power-Down (PD) and Output Data (D0-D11)

In addition to low operating power, the MAX1420 features two power-down modes: reference power-down and shutdown mode. In reference power-down, the internal bandgap reference is deactivated, which results in a typical 2mA supply current reduction. A full shutdown mode is available to maximize power savings during idle periods.

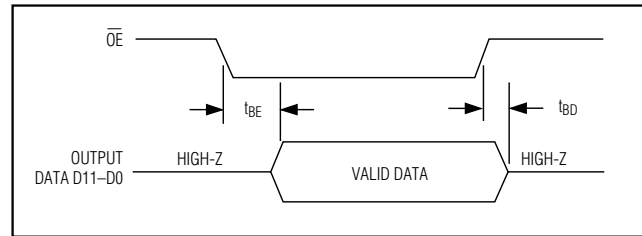


Figure 5. Output Enable Timing

The MAX1420 provides parallel, offset binary, CMOS-compatible three-state outputs. With  $\overline{OE}$  high, the digital outputs enter a high-impedance state. If  $\overline{OE}$  is held low with PD high, the outputs are latched at the last digital output code prior to the power-down. All data outputs, D0 (LSB) through D11 (MSB), are TTL/CMOS logic-compatible. There is a seven clock-cycle latency between any particular sample and its valid output data. The output coding is in offset binary format (Table 1).

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The capacitive load on the digital outputs D0 through D11 should be kept as low as possible ( $\leq 10\text{pF}$ ), to avoid large digital currents that could feed back into the analog portion of the MAX1420, thereby degrading its performance. The use of buffers (e.g., 74LVCH16244) on the digital outputs of the ADC can further isolate the digital outputs from heavy capacitive loads. To further improve the dynamic performance of the MAX1420, add small-series resistors of 100Ω to the digital output paths, close to the ADC.

Figure 5 displays the timing relationship between output enable and data output.

### System Timing Requirements

Figure 6 depicts the relationship between the clock input, analog input, and valid data output. The MAX1420 samples the analog input signal on the rising edge of CLK (falling edge of CLK) and output data is valid seven clock cycles (latency) later.

### Applications Information

Figure 7 depicts a typical application circuit containing a single-ended to differential converter. The internal reference provides an  $AV_{DD}/2$  output voltage for level shifting purposes. The input is buffered and then split to a voltage follower and inverter. A lowpass filter at the input suppresses some of the wideband noise associated

Table 1. MAX1420 Output Code for Differential Inputs

DIFFERENTIAL INPUT VOLTAGE*	DIFFERENTIAL INPUT	OFFSET BINARY
$V_{REF} \times 2047/2048$	+FULL SCALE - 1LSB	1111 1111 1111
$V_{REF} \times 2046/2048$	+FULL SCALE - 2LSB	1111 1111 1110
$V_{REF} \times 1/2048$	+ 1 LSB	1000 0000 0001
0	Bipolar Zero	1000 0000 0000
$-V_{REF} \times 1/2048$	- 1 LSB	0111 1111 1111
$-V_{REF} \times 2046/2048$	-FULL SCALE + 1 LSB	0000 0000 0001
$-V_{REF} \times 2047/2048$	-FULL SCALE	0000 0000 0000

\*  $V_{REF} = V_{REFP} - V_{REFN}$

# 12-Bit, 60Mps, 3.3V, Low-Power ADC with Internal Reference

**MAX1420**

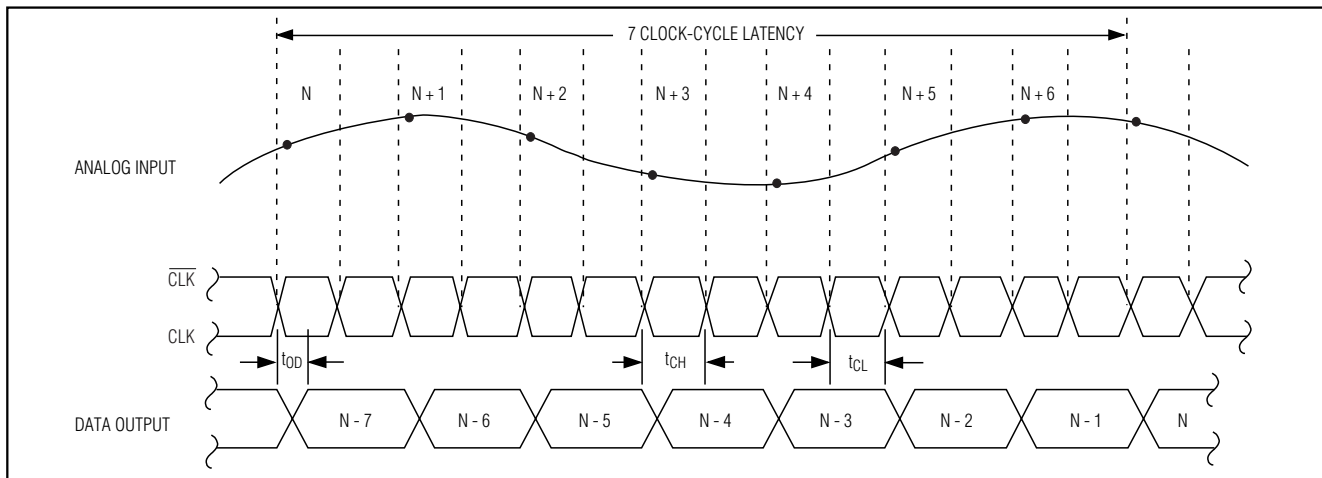


Figure 6. System and Output Timing Diagram

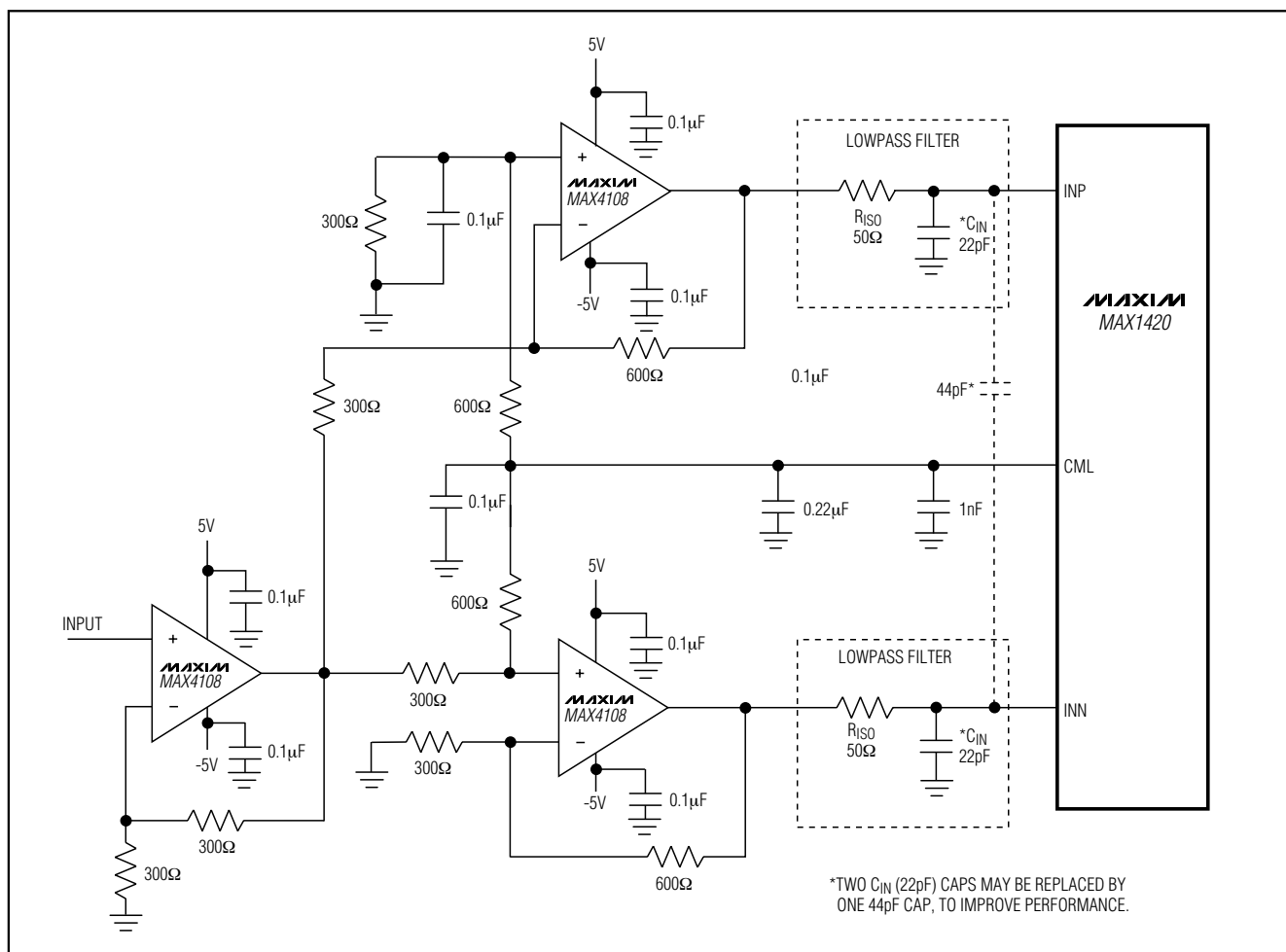


Figure 7. Typical Application Circuit for Single-Ended to Differential Conversion

# 12-Bit, 60MSPs, 3.3V, Low-Power ADC with Internal Reference

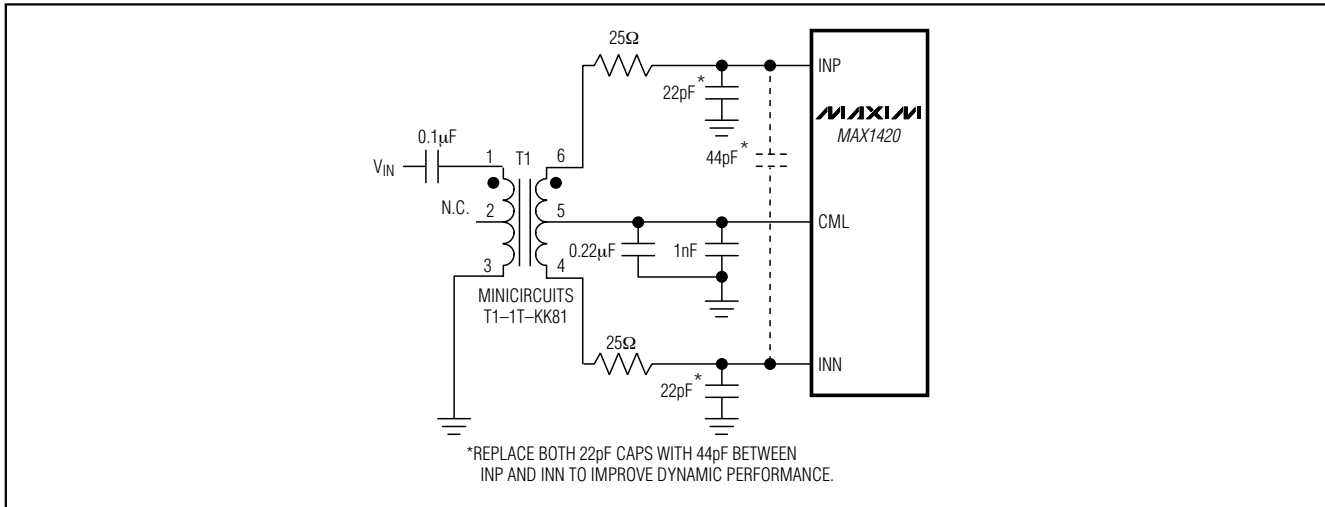


Figure 8. Using a Transformer for AC-Coupling

with high-speed op amps. Select the  $R_{ISO}$  and  $C_{IN}$  values to optimize the filter performance, to suit a particular application. For the application in Figure 7, an isolation resistor ( $R_{ISO}$ ) of  $50\Omega$  is placed before the capacitive load to prevent ringing and oscillation. The  $22\text{pF}$   $C_{IN}$  capacitor acts as a small bypassing capacitor. Connecting  $C_{IN}$  from INN to INP may further improve dynamic performance.

### Using Transformer Coupling

An RF transformer (Figure 8) provides an excellent solution to convert a single-ended signal to a fully differential signal, required by the MAX1420 for optimum performance. Connecting the center tap of the transformer to CML provides an  $AV_{DD}/2$  DC level shift to the input. Although a 1:1 transformer is shown, a 1:2 or 1:4 step-up transformer may be selected to reduce the drive requirements.

In general, the MAX1420 provides better SFDR and THD with fully differential input signals over single-ended input signals, especially for very high input frequencies. In differential input mode, even-order harmonics are suppressed and each input requires only half the signal swing compared to single-ended mode.

### Single-Ended AC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application, using a MAX4108 op amp. This configuration provides high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

## Grounding, Bypassing, and Board Layout

The MAX1420 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side of the board as the ADC, using surface-mount devices for minimum inductance. Bypass REFP, REFN, REFIN, and CML with a parallel network of  $0.22\mu\text{F}$  capacitors and  $1\text{nF}$  to AGND.  $AV_{DD}$  should be bypassed with a similar network of a  $10\mu\text{F}$  bipolar capacitor in parallel with two ceramic capacitors of  $1\text{nF}$  and  $0.1\mu\text{F}$ . Follow the same rules to bypass the digital supply  $DV_{DD}$  to DGND. Multilayer boards with separate ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arrangement to match the physical location of the analog ground (AGND) and the digital ground (DGND) on the ADCs package. Join the two ground planes at a single point, such that the noisy digital ground currents do not interfere with the analog ground plane. Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital signal traces away from sensitive analog traces and remove digital ground and power planes from underneath digital outputs. Keep all signal lines short and free of 90 degree turns.

# 12-Bit, 60Mps, 3.3V, Low-Power ADC with Internal Reference

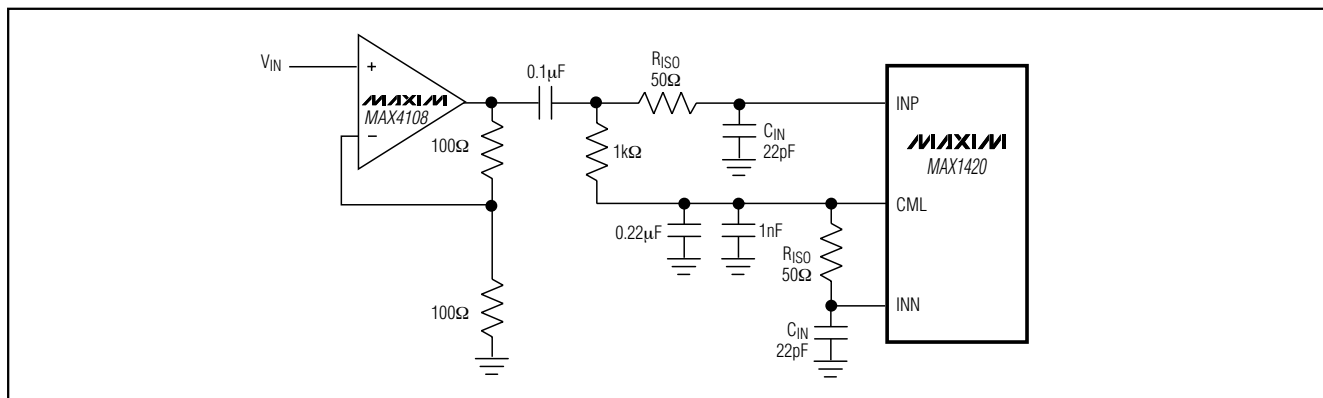


Figure 9. Single-Ended AC-Coupled Input Signal

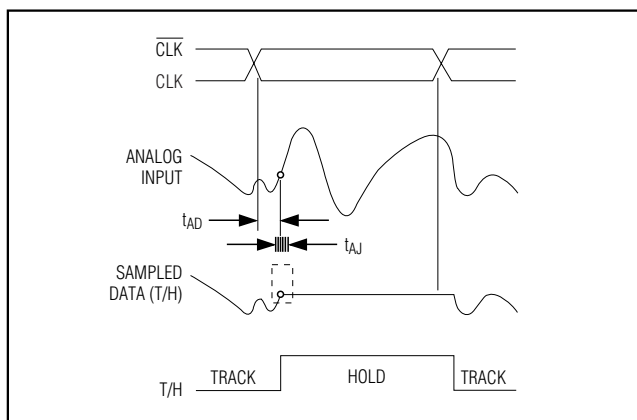


Figure 10. T/H Aperture Timing

## Static Parameter Definitions

### Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight-line. This straight-line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function once offset and gain errors have been nullified. The static linearity parameters for the MAX1420 are measured using the best straight-line fit method.

### Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step-width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes.

## Dynamic Parameter Definitions

### Aperture Jitter

Figure 10 depicts the aperture jitter ( $t_{AJ}$ ), which is the sample-to-sample variation in the aperture delay.

### Aperture Delay

Aperture delay ( $t_{AD}$ ) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 10).

### Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N-bits):

$$SNR_{MAX} = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, e.g., thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first four harmonics, and the DC offset.

### Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

### Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is computed from:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

# 12-Bit, 60MSPS, 3.3V, Low-Power ADC with Internal Reference

### Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the first four harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD_{dB} = 20 \times \log_{10} \left( \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1} \right)$$

where  $V_1$  is the fundamental amplitude, and  $V_2$  through  $V_5$  are the amplitudes of the 2nd- through 5th-order harmonics.

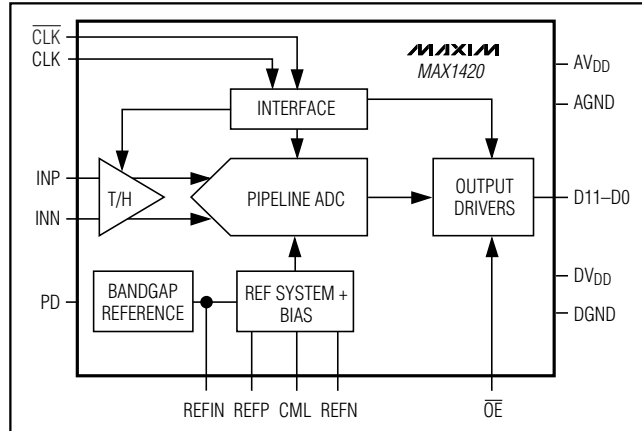
### Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

### Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -6.5dB full scale.

### Functional Diagram





# 12-Bit, 60Msps, 3.3V, Low-Power ADC with Internal Reference

## Package Information

**MAX1420**

JEDEC VARIATION				
	BC		BE	
	32 LEAD	48 LEAD	32 LEAD	48 LEAD
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A <sub>1</sub>	0.05	0.15	0.05	0.15
A <sub>2</sub>	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D <sub>1</sub>	7.00	BSC.	7.00	BSC.
E	8.90	9.10	8.90	9.10
E <sub>1</sub>	7.00	BSC.	7.00	BSC.
e	0.8	BSC.	0.5	BSC.
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°

**NOTES:**

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP

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32/48L, TQFP, EPS

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## MAX1420

### Part Number Table

#### Notes:

1. See the [MAX1420 QuickView Data Sheet](#) for further information on this product family or download the [MAX1420 full data sheet](#) (PDF, 848kB).
2. Other options and links for purchasing parts are listed at: <http://www.maxim-ic.com/sales>.
3. [Didn't Find What You Need?](#) Ask our applications engineers. Expert assistance in finding parts, usually within one business day.
4. Part number suffixes: T or T&R = tape and reel; + = RoHS/lead-free; # = RoHS/lead-exempt. More: See [full data sheet](#) or [Part Naming Conventions](#).
5. \* Some packages have variations, listed on the drawing. "PkgCode/Variation" tells which variation the product uses.

Part Number	Free Sample	Buy Direct	Package: TYPE PINS SIZE DRAWING CODE/VAR *	Temp	RoHS/Lead-Free? Materials Analysis
MAX1420CCM-TD		<input type="checkbox"/>		0C to +70C	RoHS/Lead-Free: <a href="#">No</a>
MAX1420CCM+TD		<input type="checkbox"/>		0C to +70C	RoHS/Lead-Free: <a href="#">Yes</a>
MAX1420CCM+D	<input type="checkbox"/>	<input type="checkbox"/>		0C to +70C	RoHS/Lead-Free: <a href="#">Yes</a>
MAX1420CCM-D		<input type="checkbox"/>	LQFP;48 pin;7x7x1.4 mm Dwg: <a href="#">21-0054F</a> (PDF) Use pkgcode/variation: C48-2*	0C to +70C	RoHS/Lead-Free: <a href="#">No</a> <a href="#">Materials Analysis</a>
MAX1420ECM+D	<input type="checkbox"/>	<input type="checkbox"/>	LQFP;48 pin;7x7x1.4 mm Dwg: <a href="#">21-0054F</a> (PDF) Use pkgcode/variation: C48+2*	-40C to +85C	RoHS/Lead-Free: <a href="#">Yes</a> <a href="#">Materials Analysis</a>
MAX1420ECM-TD		<input type="checkbox"/>		-40C to +85C	RoHS/Lead-Free: <a href="#">No</a>
MAX1420ECM-D	<input type="checkbox"/>	<input type="checkbox"/>	LQFP;48 pin;7x7x1.4 mm Dwg: <a href="#">21-0054F</a> (PDF) Use pkgcode/variation: C48-2*	-40C to +85C	RoHS/Lead-Free: <a href="#">No</a> <a href="#">Materials Analysis</a>

MAX1420ECM+T				-40C to +85C	RoHS/Lead-Free: <a href="#">Yes</a>
MAX1420ECM+				-40C to +85C	RoHS/Lead-Free: <a href="#">Yes</a>
MAX1420ECM+TD				-40C to +85C	RoHS/Lead-Free: <a href="#">Yes</a>

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