FEATURES

- **Fast Settling Output Current 85ns**
- **Full-Scale Current Prematched to ±0.3 LSB**
- **Direct Interface to TTL, CMOS, ECL, PMOS, NMOS**
- **Nonlinearity to ±1/2 LSB Maximum Over Temp.**
- **High Output Impedance and Compliance −10V to +18V**
- **Complementary Current Outputs**
- **Wide Range Multiplying Capability ... 1MHz Bandwidth**
- **Low FS Current Drift ..... ±10ppm/ΔC**
- **Wide Power Supply Range ..... ±4.5V to ±18V**
- **Low Power Consumption ..... 37mW @ ±5V**
- **Low Cost**
- **Available in Die Form**

ORDERING INFORMATION †

NL LSB	PACKAGE: CERDIP 16-PIN	PACKAGE: PLASTIC 16-PIN	OPERATING TEMPERATURE RANGE
±1/2	DAC20CQ	DAC20CP	COM

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

GENERAL DESCRIPTION

The DAC-20 series of 2-digit BCD monolithic multiplying digital to analog converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low "glitch" energy and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full-scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

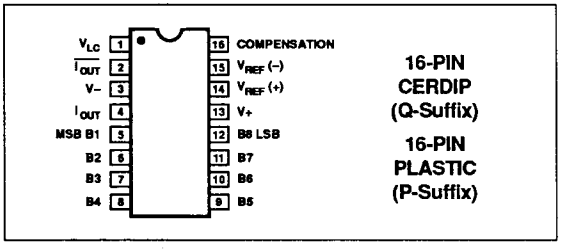
Complementary current outputs with −10V to +18V voltage compliance enable resistive termination, a voltage output without an external op amp.

Both DAC-20 models guarantee full 2-digit monotonicity, some have nonlinearity as tight as ±1/2 LSB over the entire operating temperature range. Nonlinearity is unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

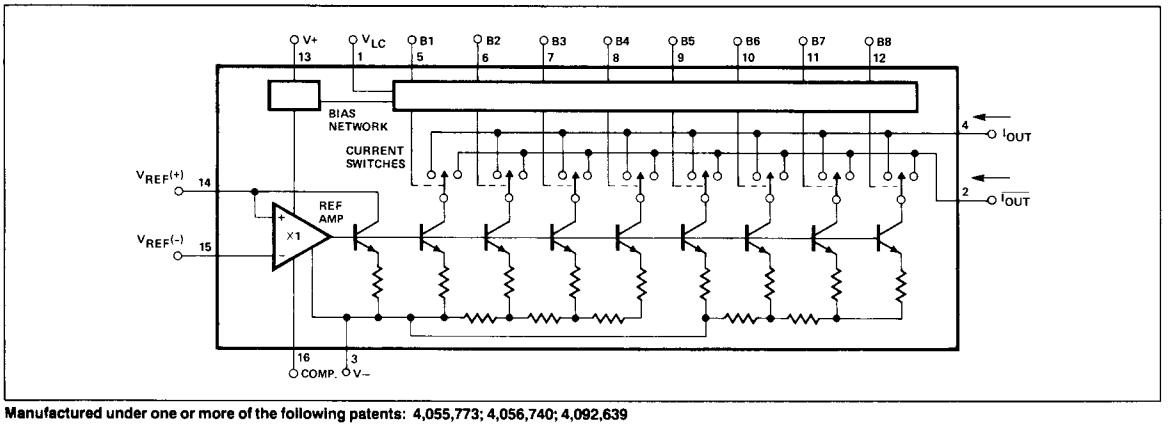
The compact size and low power consumption make the DAC-20 attractive for portable applications.

DAC-20 applications include A/D converters, audio attenuators, analog meter drivers, programmable power supplies, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

PIN CONNECTIONS



EQUIVALENT CIRCUIT



Manufactured under one or more of the following patents: 4,055,773; 4,056,740; 4,092,639

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted)

Operating Temperature Range
DAC-20 CQ, CP ..... 0°C to +70°C
Junction Temperature (T_j) ..... –65°C to +150°C
Storage Temperature Range
Q Package ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Lead Temperature (Soldering, 60 sec) ..... 300°C
V+ Supply to V–Supply 36V
Logic Inputs ..... V– to V– plus 36V
V_{LC} ..... V– to V+
Reference Inputs (V_{14}, V_{15}) ..... V– to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 5.0mA

PACKAGE TYPE	Θ_{JA} (Note 2)	Θ_{JC}	UNITS
16-Pin Hermetic DIP (Q)	100	16	°C/W
16-Pin Plastic DIP (P)	82	39	°C/W

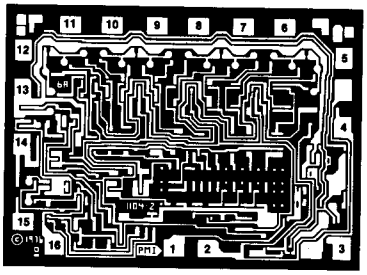
NOTES:
1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, I_{REF} = 2.0mA, 0°C ≤ T_A ≤ 70°C, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20C MIN	DAC-20C TYP	DAC-20C MAX	UNITS
Resolution		BCD 0 to 99 steps	2	—	—	Digits
Monotonicity		BCD 99 steps	2	—	—	Digits
Nonlinearity	NL	0000 0000 to 1001 1001	—	—	±1/2	LSB
Settling Time	t_S	To ±1/2 LSB (±0.5% FS) all bits switched ON or OFF, T_A = 25°C (Note 1)	—	85	150	ns
Propagation Delay Each Bit All bits switched	 t_{PLH} t_{PHL}	T_A = 25°C (Note 1)	—	35	60	ns
Full Tempco	TCI_{FS}	(Note 1)	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V_{OC}	Full-scale current change < 1/2 LSB (< 0.5% FS) R_{OUT} > 20MΩ typical I_{REF} = 1mA	–10	—	+18	V
Full Range Output (Digital Input 1001 1001)	I_{FR4}	T_A = 25°C, I_{REF} = 2mA	1.92	1.98	2.04	mA
Zero-Scale Current	I_{ZS}		—	0.2	5	µA
Output Current Range	I_{OR}	V– = –10V V– = –12V to –18V	2.2 4.2	2 2	— —	mA
Logic Input Levels Logic "0" Logic "1"	 V_{IL} V_{IH}	V_{LC} = 0V	 — 2	 — —	 0.8 —	V
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	V_{LC} = 0V V_{IN} = –10V to +0.8V V_{IN} = 2V to 18V	 — —	 –2 0.002	 ±10 ±10	µA
Logic Input Swing	V_{IS}	V– = –15V	–10	—	+18	V
Logic Threshold Range	V_{THR}	V_S = ±15V (Note 1)	–10	—	+13.5	V
Reference Bias Current	I_{15}		—	–1	–3	µA
Reference Input Slew Rate	dI/dt	(Note 1)	4	8	—	mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V V– = –4.5V to –18V I_{REF} = 1mA	— —	±0.0003 ±0.002	±0.03 ±0.03	$\%\Delta I_{FS}$ / $\%\Delta V$
Power Supply Current	I+ I– I+ I–	V_S = ±5V, I_{REF} = 1mA V_S = ±15V, I_{REF} = 2mA 	— — — —	2.3 –5.0 2.5 –7.8	3.8 –6.5 3.8 –9.1	mA
Power Dissipation	P_d	V_S = ±5V, I_{REF} = 1mA V_S = ±15V, I_{REF} = 2mA	— —	37 152	52 194	mW

NOTE:
1. Guaranteed by design.

DICE CHARACTERISTICS



DIE SIZE 0.086 × 0.064 inch, 5,504 sq. mils
(2.184 × 1.625 mm, 3.55 sq. mm)

1. V_{LC}
2. $\overline{I_{OUT}}$
3. V−
4. I_{OUT}
5. BIT 1 (MSB)
6. BIT 2
7. BIT 3
8. BIT 4
9. BIT 5
10. BIT 6
11. BIT 7
12. BIT 8 (LSB)
13. V+
14. V_{REF} (+)
15. V_{REF} (−)
16. COMP

For additional DICE ordering information, refer to 1990/91 Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 25°C$, unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20G LIMIT	UNITS
Resolution		BCD 0 to 99 steps	2	Digits MIN
Monotonicity		BCD 99 steps	2	Digits MIN
Nonlinearity	NL	FS = 1001 1001	±1/2	LSB MAX
Output Voltage Compliance	V_{OC}	Full-Scale Current Change <1/2 LSB	+18 −10	V MAX V MIN
Full-Scale Current	I_{FS4}	$V_{REF} = 10V$ $R_{14}, R_{15} = 5k\Omega$	2.04 1.92	mA MAX mA MIN
Zero-Scale Current	I_{ZS}		5	μA MAX
Output Current Range	I_{OR}	V− = −10V V− = −12V to −18V	2.1 4.2	mA MIN
Logic "0" Input Level	V_{IL}		0.8	V MAX
Logic "1" Input Level	V_{IH}		2	V MIN
Logic Input Current Logic "0" Logic "1"	 I_{IL} I_{IH}	 $V_{IN} = -10V$ to +0.8V $V_{IN} = 2V$ to 18V	 ±10 ±10	 μA MAX
Logic Input Swing	V_{IS}	V− = −15V	+18 −10	V MAX V MIN
Power Supply Sensitivity	$PSSI_{FS+}$ $PSSI_{FS-}$	V− = −4.5V to −18V V− = −4.5V to −18V $I_{REF} = 1mA$	±0.03 ±0.03	$\%\Delta I_{FS}$ MAX $\%\Delta V$
Power Supply Current	I+ I−	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	3.8 −7.8	mA MAX
Power Dissipation	P_d	$V_S = \pm 18V$ $I_{REF} \leq 2mA$	194	mW MAX

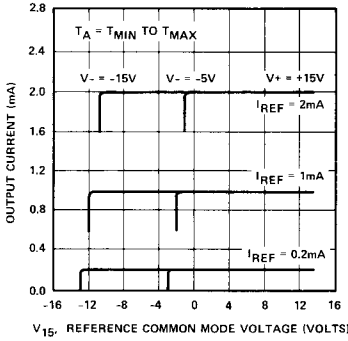
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, unless otherwise noted specified. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-20G TYPICAL	UNITS
Reference Input Slew Rate	dI/dt		8	mA/μs
Propagation Delay	t_{PLH}, t_{PHL}	$T_A = 25°C$, Any Bit	35	ns
Settling Time	t_S	To ±1/2 LSB, All Bits Switched ON or OFF, $T_A = 25°C$	85	ns

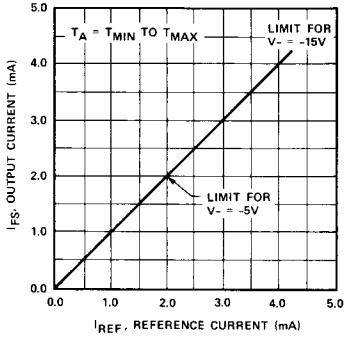
TYPICAL REFERENCE PERFORMANCE CHARACTERISTICS

REFERENCE AMP COMMON-MODE RANGE (DIGITAL INPUT 1001 1001)



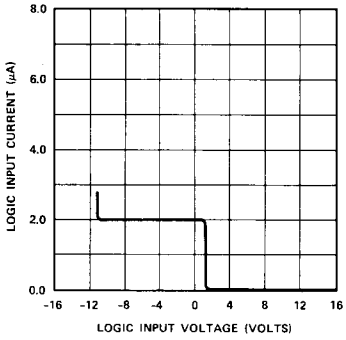
NOTE: POSITIVE COMMON MODE IS ALWAYS (V+) -1.5V; NEGATIVE COMMON MODE RANGE IS V- PLUS (I_{REF} x 800Ω) PLUS 2.5V.

FULL-SCALE CURRENT vs REFERENCE CURRENT (DIGITAL INPUT 1001 1001)

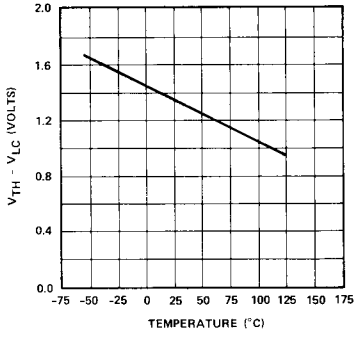


NOTE: THE RECOMMENDED RANGE FOR OPERATION WITH WITH A DC REFERENCE CURRENT IS +0.2mA TO +4.0mA.

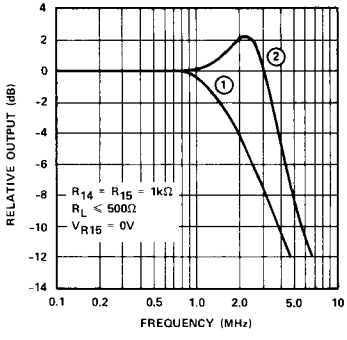
LOGIC INPUT CURRENT vs INPUT VOLTAGE



$V_{TH} - V_{LC}$ vs TEMPERATURE

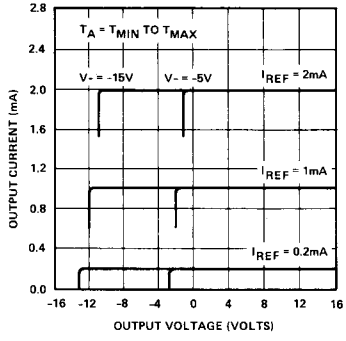


REFERENCE INPUT FREQUENCY RESPONSE (DIGITAL INPUT 1001 1001)

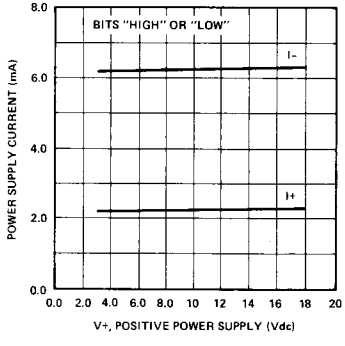


CURVE 1: C_C = 15pF, V_{IN} = 2.0V_{P-P} CENTERED AT +1.0V, LARGE SIGNAL.
CURVE 2: C_C = 15pF, V_{IN} = 50mV_{P-P} CENTERED AT +200mV, SMALL SIGNAL.

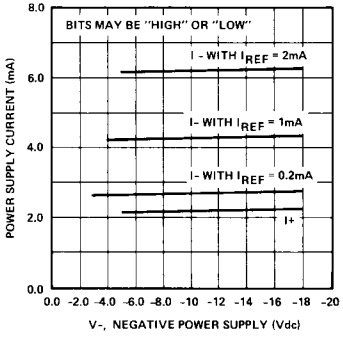
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE) (DIGITAL INPUT 1001 1001)



POWER SUPPLY CURRENT vs V+

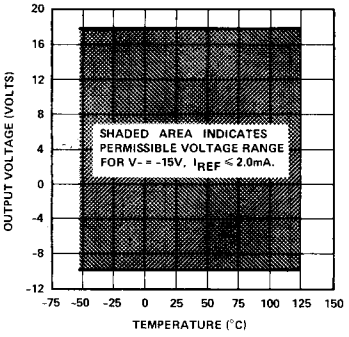


POWER SUPPLY CURRENT vs V-

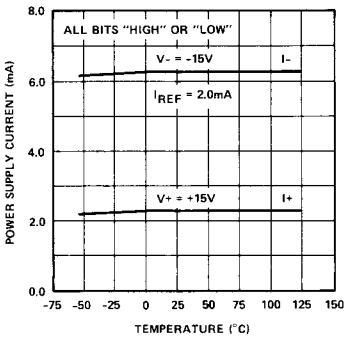


TYPICAL REFERENCE PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



POWER SUPPLY CURRENT vs TEMPERATURE



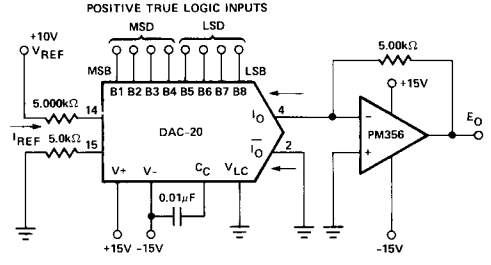
BASIC OUTPUT CONNECTIONS

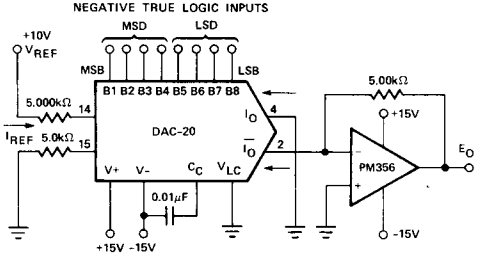
With complementary current outputs, the DAC-20 may be used with either positive true or negative true (complementary) logic. Current appears at the "true" output (I_O) when a "1" is applied to a logic input. As the BCD-coded input increases, the sink current at Pin 4 increases proportionately, in the fashion of a "positive logic" D/A converter. When a "0" is applied to a logic input, that current is turned OFF at Pin 4 and ON at Pin 2 ($\overline{I_O}$) which is used for negative true or "negative logic" D/A converters.

The unused output must be connected to ground or some voltage source capable of sourcing 1.65 times I_{REF}. A detailed discussion of reference input operation begins on the next page.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V- and is independent of the positive supply. Negative compliance is given by V- plus ($I_{REF} \times 800\Omega$) plus 2.5V.

POSITIVE VOLTAGE OUTPUT

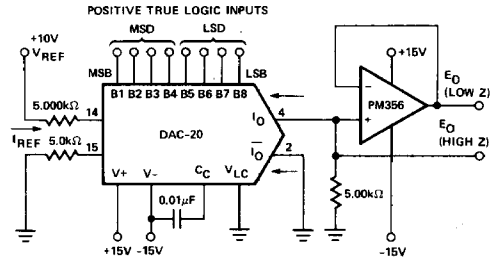


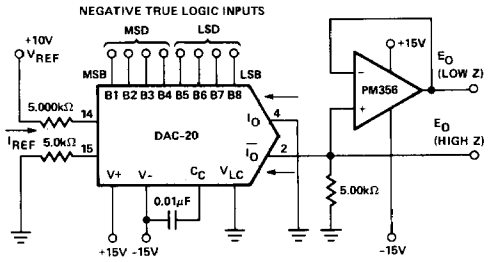


DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	+1.0V
20	0010	0000	0.40mA	+2.0V
30	0011	0000	0.60mA	+3.0V
40	0100	0000	0.80mA	+4.0V
80	1000	0000	1.60mA	+8.0V
99	1001	1001	1.98mA	+9.9V

DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	+1.0V
20	1101	1111	0.40mA	+2.0V
30	1100	1111	0.60mA	+3.0V
40	1011	1111	0.80mA	+4.0V
80	0111	1111	1.60mA	+8.0V
99	0110	0110	1.98mA	+9.9V

NEGATIVE VOLTAGE OUTPUT



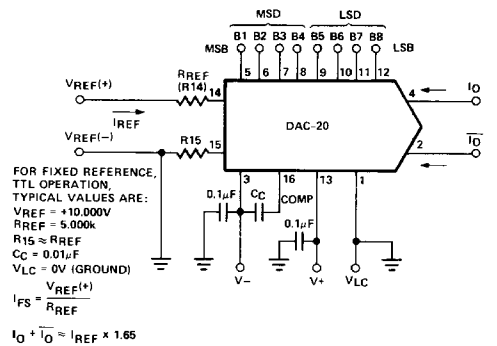


DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	I_O	E_O
0	0000	0000	0	0
10	0001	0000	0.20mA	−1.0V
20	0010	0000	0.40mA	−2.0V
30	0011	0000	0.60mA	−3.0V
40	0100	0000	0.80mA	−4.0V
80	1000	0000	1.60mA	−8.0V
99	1001	1001	1.98mA	−9.9V

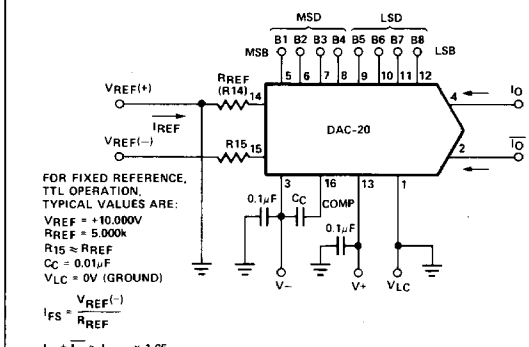
DECIMAL INPUT	BCD INPUT MSD	BCD INPUT LSD	$\overline{I_O}$	E_O
0	1111	1111	0	0
10	1110	1111	0.20mA	−1.0V
20	1101	1111	0.40mA	−2.0V
30	1100	1111	0.60mA	−3.0V
40	1011	1111	0.80mA	−4.0V
80	0111	1111	1.60mA	−8.0V
99	0110	0110	1.98mA	−9.9V

REFERENCE OPERATION

POSITIVE



NEGATIVE



REFERENCE AMPLIFIER SETUP

The DAC-20 is a multiplying converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = 99/100 \times I_{REF}, \text{ where } I_{REF} = I_{14}.$$

In positive reference applications an external positive reference voltage forces current through R_{14} into the $V_{REF}(+)$ terminal (Pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF}(-)$ at Pin 15; reference current flows from ground through R_{14} into $V_{REF}(+)$, as in the positive reference case. This negative reference con-

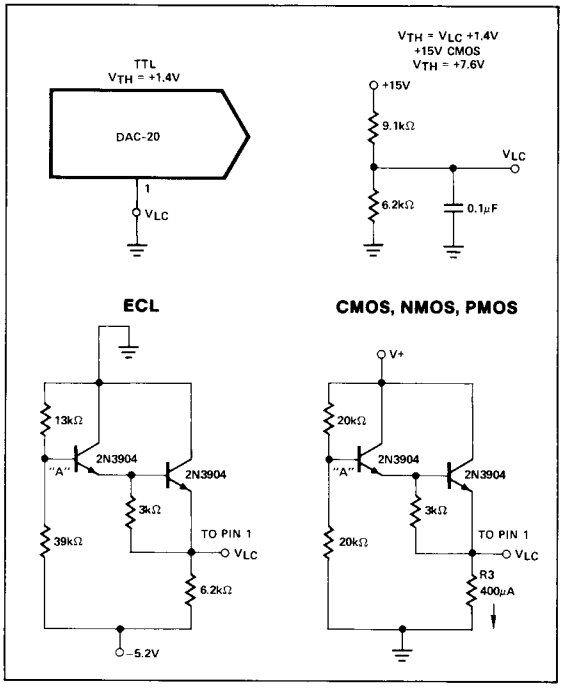
nection has the advantage of a very high impedance presented at Pin 15. The voltage at Pin 14 is equal to and tracks the voltage at Pin 15 due to the high gain of the internal reference amplifier. R_{15}(nominally equal to R_{14}) is used to cancel bias current errors and may be eliminated with only a minor increase in error.

When a DC reference in used, a reference bypass capacitor is recommended. A 5V TTL logic supply is not recommended as reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FR} will eliminate the need for trimming I_{REF}. If required, full-scale trimming may be accomplished by adjusting the value of R_{14}.

The reference amplifier must be compensated by using a capacitor form Pin 16 to V–. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Multiplying Operation."

LOGIC INPUT OPERATION AND INTERFACING



LOGIC THRESHOLD CONTROL

The DAC-20 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage.

For V– = –15V, the logic inputs may swing between –10V and +18V. This enables direct interface with a +15V CMOS logic, even when the DAC-20 is powered from a +5V supply. Minimum logic threshold voltage are given by: V– plus (I_{REF} × 800Ω) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (Pin 1, V_{LC}).

The logic input threshold is 1.4V above V_{LC}. For TTL and DTL interface, simply ground Pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see the figure. Pin 1 will source 100μA typically, so the external circuitry must be designed to accommodate this current. Note that the threshold voltage has the temperature dependence of two forward biased diodes. The two V_{LC} setting circuits shown, include temperature compensation.

Fastest settling times are obtained when Pin 1 sees a low impedance. If Pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

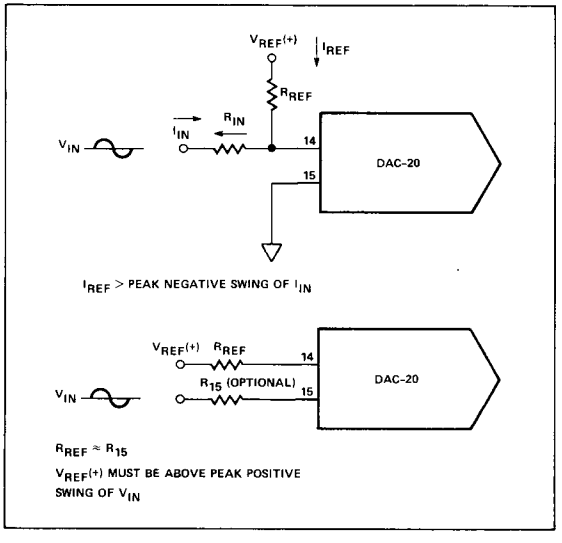
MULTIPLYING OPERATION

The DAC-20 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 2mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 2mA.

Bipolar references may be accommodated by offsetting V_{REF} or Pin 15. The negative common-mode range of the reference amplifier is given by: V_{CM-} = V– plus (I_{REF} × 800Ω) plus 2.5V. The positive common mode range is V+ less 1.5V.

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V–. The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum value of C_C are 15, 37, and 75pF. Larger values of R_{14} require

ACCOMMODATING BIPOLAR REFERENCES

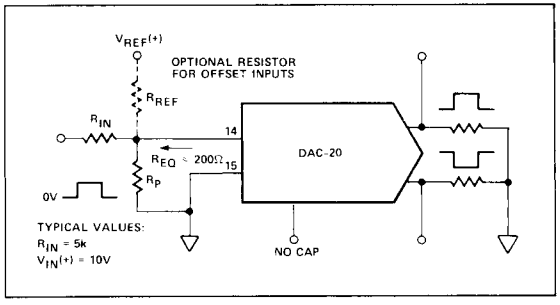


proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If Pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated, which will decrease overall bandwidth and slew rate. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at $4mA/\mu s$ enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accommodated by the alternate compensation scheme shown above. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier for a cutoff ($I_{REF} = 0$) condition. Full-scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at Pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of $16mV/\mu s$, which is relatively independent of R_{IN} and V_{IN} values.

PULSED REFERENCE OPERATION



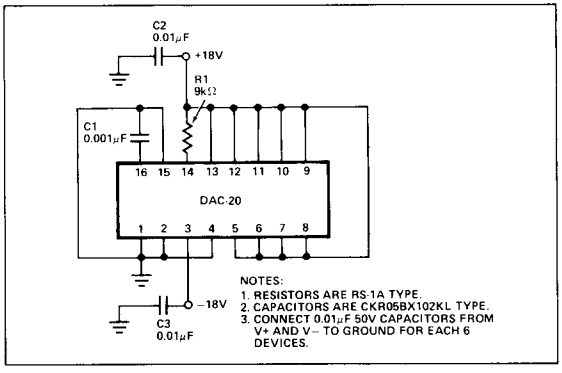
POWER SUPPLY CONSIDERATIONS

The DAC-20 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common-mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible. However, at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC-20 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required: however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power Consumption may be calculated as follows: $P_d = (I+) \times (V+) + (I-) \times (V-)$. A useful feature of the DAC-20 design is that supply current is constant and independent of input logic states; this reduces the size of the power supply bypass capacitors.

BURN-IN CIRCUIT



TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specification of the DAC-20 are guaranteed to apply over the entire rated operating temperature range. Full-scale output current drift is tight, typically ±10ppm/°C, with zero-scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full-scale drift.

SETTLING TIME OPTIMIZATION

The DAC-20 is capable of extremely fast settling times, typically 85ns at $I_{REF} = 2.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The output capacitance of the DAC-20, including the package, is approximately 15pF; therefore the output RC time constant dominates settling time if $R_L > 500\Omega$.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1µF capacitors at the supply pins provide full transient protection.