



# Wide Temperature Range 12-Bit IC D/A Converter

## AD DAC85/AD DAC87

*T-51-09-12*

### 1.1 Scope.

This specification covers the device requirements for a high performance 12-bit hybrid digital-to-analog converter. (The monolithic version is detailed on page 619.)

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD DAC85MILCBI-V/883B
-2	AD DAC85MILCBI-I/883B
-3	AD DAC87CBI-V/883B
-4	AD DAC87CBI-I/883B

### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-H-1000; package outline: DH-24A.

### 1.3 Absolute Maximum Ratings. ( $T_A = +25^\circ\text{C}$ unless otherwise noted)

Positive Supply Voltage $V_{CC}$ to Digital Return . . . . .	+18V
Negative Supply Voltage $V_{EE}$ to Digital Return . . . . .	-18V
Positive Supply Voltage $V_{DD}$ to Digital Return . . . . .	+7V
Digital Input Voltage to Digital Return . . . . .	0V to $V_{DD}$
Output Short Circuit Duration (to Ground Only) . . . . .	25ms
Junction Temperature . . . . .	+175°C
Storage Temperature Range . . . . .	-65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . .	+300°C

### 1.5 Thermal Characteristics.

Thermal Resistance  $\theta_{JC} = 7^\circ\text{C/W}$   
 $\theta_{JA} = 37^\circ\text{C/W}$

## AD DAC85/AD DAC87 — SPECIFICATIONS

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Test	Symbol	Device	Design Limit +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition <sup>1,2</sup>	Units
Logic Levels								
Digital Input High	V <sub>IH</sub>	-1, 2, 3, 4	2.0			2.0		+ V min
Digital Input Low	V <sub>IL</sub>	-1, 2, 3, 4	0.8			0.8		+ V max
Digital Input High Current	I <sub>IH</sub>	-1, 2, 3, 4	1			1	V <sub>IH</sub> = 5.0V	- μA min
			250			250		+ μA max
Digital Input Low Current	I <sub>IL</sub>	-1, 2, 3, 4	10			10	V <sub>IL</sub> = +0.8V	- μA min
			100			100		+ μA max
Gain Error <sup>3</sup>	A <sub>E</sub>	-1, 2	0.3	0.3			Input Bits = 0000 0000 0000 To Input Bits = 1111 1111 1111 Unipolar V <sub>FSR</sub> = 10V	± % FSR max
		-3, 4	0.2			0.2		
Gain Error Drift	TCA <sub>E</sub>	-1, 2	20		20		Input Bits = 0000 0000 0000 Unipolar = 0 to +10V	± ppm/°C max
		-3, 4	25		25		Unipolar = 0 to +10V	
Unipolar Offset	V <sub>OS</sub>	-1, 2	0.15	0.15			Input Bits = 1111 1111 1111 Unipolar V <sub>FSR</sub> = 10V	± % FSR max
		-3, 4	0.10			0.10		
Unipolar Offset Drift	TCV <sub>OS</sub>	-1, 2, 3, 4	3		3		Input Bits = 1111 1111 1111 Unipolar V <sub>FSR</sub> = 10V	± ppm/°C max
Bipolar Offset	B <sub>POE</sub>	-1, 2	0.15	0.15			Input Bits = 1111 1111 1111	± % FSR max
		-3, 4	0.10			0.10		
Bipolar Offset Drift	TCB <sub>POE</sub>	-1, 2, 3, 4	10		10		Input Bits = 1111 1111 1111	± ppm/°C max
Unipolar Zero Error Current Output	I <sub>OS</sub>	-2, 4	3	3			Input Bits = 1111 1111 1111	μA max
Bipolar Zero Error Current Output	I <sub>BPZE</sub>	-2, 4	3	3			Input Bits = 0111 1111 1111	μA max
Bipolar Gain Error Current Output	I <sub>BPGE</sub>	-2, 4	0.96			0.96	Input Bits = 0000 0000 0000	- μA max
			1.04			1.04		- μA min
Bipolar Offset Error Current Output	I <sub>BPOE</sub>	-2, 4	0.96			0.96	Input Bits = 1111 1111 1111	+ μA min
			1.04			1.04		+ μA max
Unipolar Gain Error Current Output	I <sub>OGGE</sub>	-2, 4	2.3995			2.3995	Input Bits = 0000 0000 0000	- μA min
			1.5995			1.5995		- μA max
Bipolar Zero Error	B <sub>PZ</sub>	-1, 2	0.15	0.15			Input Bits = 0111 1111 1111	± % FSR max
		-3, 4	0.10			0.10		
Compliance Voltage	C <sub>V</sub>	-2, 4	2.5					- V min
			10					+ V max
Differential Linearity Error	D <sub>LE</sub>	-1, 2, 3, 4	1/2	1/2			(Abbreviate Codes Test)	± LSB max
Differential Linearity Error T <sub>A</sub> @ T <sub>min</sub> to T <sub>max</sub>	TC <sub>DLE</sub>	-1, 2 -3, 4	1.0			1.0	(Abbreviate Codes Test) (Monotonic Over Temperature Range)	± LSB max
Linearity Error	LE	-1, 2, 3, 4	0.5	0.5			(Abbreviate Codes Test)	± LSB max
Linearity Error T <sub>A</sub> @ T <sub>min</sub> to T <sub>max</sub>	TC <sub>LE</sub>	-1, 2, 3, 4	0.75			0.75	(Abbreviate Codes Test)	± LSB max
Positive Summation Error	E <sub>PPE</sub>	-1, 2, 3, 4	0.50	0.50				± LSB max
Negative Summation	E <sub>NPE</sub>	-1, 2, 3, 4	0.50	0.50				± LSB max
Positive Summation Error Drift	E <sub>PETC</sub>	-1, 2, 3, 4	0.75			0.75		± LSB max
Negative Summation Error Drift	E <sub>NETC</sub>	-1, 2, 3, 4	0.75			0.75		± LSB max
Reference Output Error	V <sub>REF</sub>	-1, 3	126			126	V <sub>REF</sub> = 6.3V	± mV max

Table 1. (Continued on next page)

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Test	Symbol	Device	Design Limit +25°C (-55°C to +125°C)	Sub Group 1	Sub Group 2,3	Sub Group 4	T-51-09-12	
							Test Condition <sup>1,2</sup>	Units
Reference Output Temperature Coefficient	TCV <sub>REF</sub>	-1 -3	(20) (10)		20 10			± ppm/°C max
Settling Time	t <sub>SL</sub>	-1,3	7				Settling Time to ±0.01% FSR for FSR Change (2kΩ  500pF with 10k Feedback Resistor)	µs max
	t <sub>SL</sub>	-1,3	3				Small Signal Change (1LSB) Settling within 1/2LSB	µs max
	t <sub>SL</sub>	-2,4	300				Settling Time to ±0.01% of FSR for FSR Change 10 to 100Ω Load	ns typ
	t <sub>SL</sub>	-2,4	1				For 1kΩ Load	µs typ
+5V Supply Current Drain	+ I <sub>D</sub>	-1,2,3,4	20			20		+ mA max
+15V Supply Current Drain	+ I <sub>CC</sub>	-1,2,3,4	20			20		+ mA max
-15V Supply Current Drain	+ I <sub>BE</sub>	-1,2,3,4	35			35		- mA max
Power Supply Gain Sensitivity Δ Gain	PSRR	-1,3	0.003			0.003	+5V, +15V, -15V; Supplies ±5% Variation	±%/FS%/V <sub>S</sub>
Power Supply Gain Sensitivity Δ Gain T <sub>min</sub> to T <sub>max</sub>	TCPSRR	-1,3	(0.03)				+5V, +15V, -15V; Supplies ±5% Variation	±%/FS%/V <sub>S</sub>

NOTES

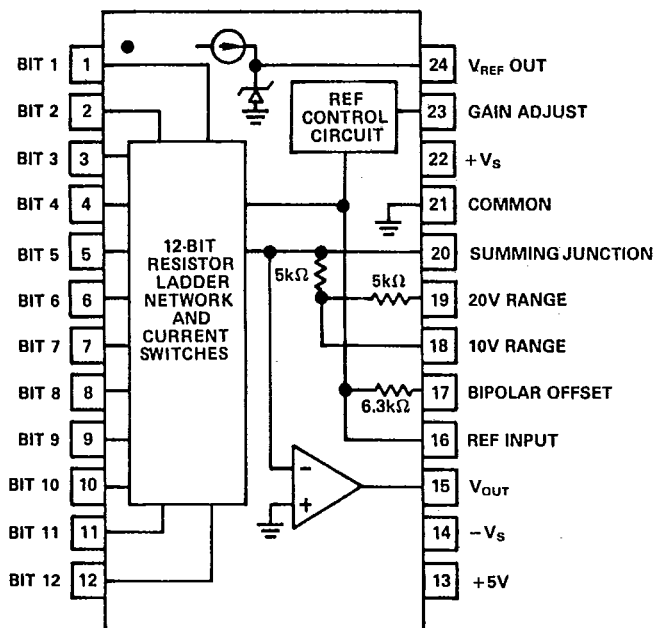
<sup>1</sup>T<sub>A</sub> = +25°C and ±V<sub>S</sub> = ±15V unless otherwise specified.

<sup>2</sup>V<sub>SS</sub> = ±15V, V<sub>D</sub> = +5V unless otherwise noted.

<sup>3</sup>Adjustable to zero.

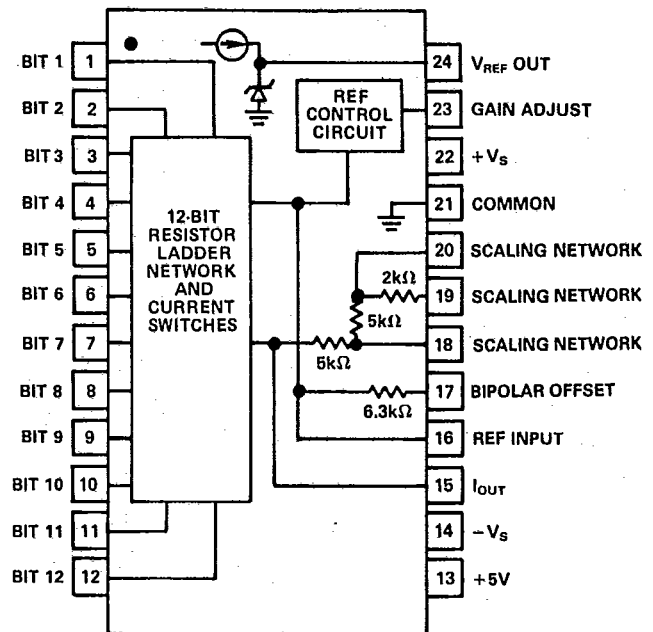
Table 1.

### 3.2.1 Functional Block Diagram and Terminal Assignments.



Device - 1 or 3

Voltage Model Functional Diagram  
and Pin Configuration



Device - 2 or 4

Current Model Functional Diagram  
and Pin Configuration

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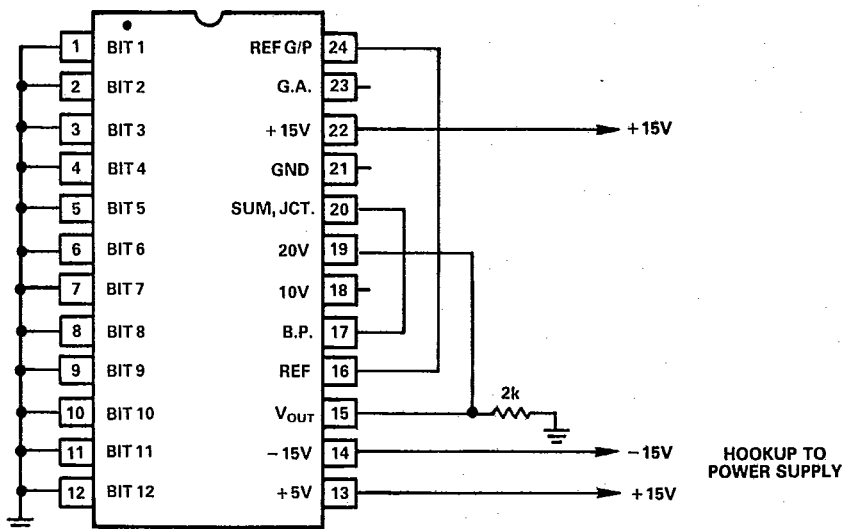
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### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (I).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

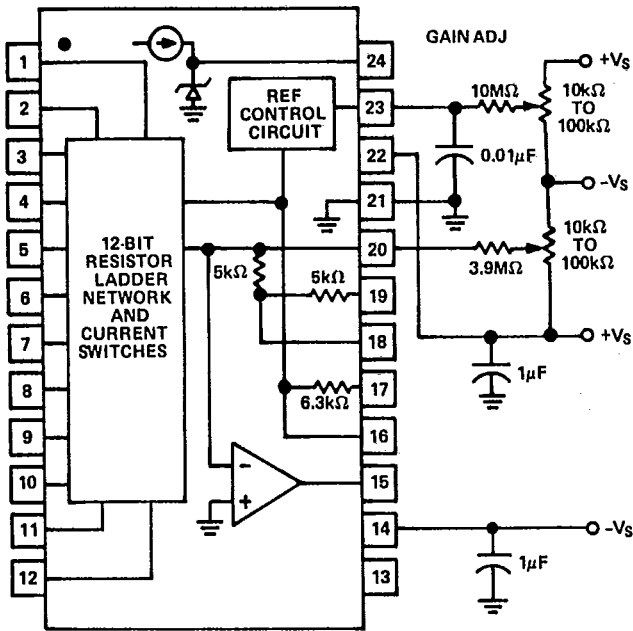


Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
± 10V	COB or CTC	19	20	15	24
± 5V	COB or CTC	18	20	N.C.	24
± 2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

Table 2. Digital Input/Analog Output

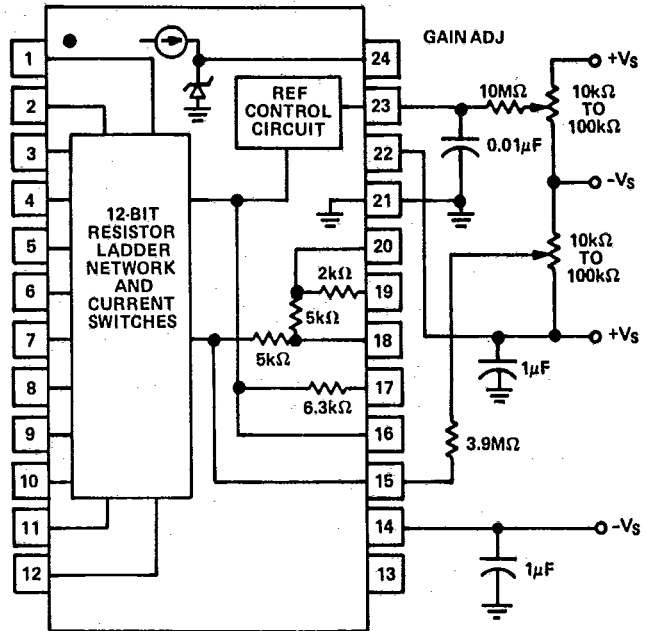
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Device - 1 or 3

External Adjustment and Voltage Supply Connection Diagram



Device - 2 or 4

External Adjustment and Voltage Supply Connection Diagram

Digital Input		Analog Output			
12 Bit Resolution		Voltage*		Current	
MSB	LSB	0 to +10V	± 10V	0 to -2mA	± 1mA
0	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
0	111111111111	+5.0000V	00000V	-1.0000mA	0.0000mA
1	000000000000	+4.9976V	-0.0049V	0.488mA	+1.000mA
1	111111111111	0.0000V	-10.0000V	0.0000mA	0.488μA
1	1LSB	2.44mV	4.88mV	-0.9995mA	+0.0005mA

\*To obtain values for other binary ranges 0 to +5V range: divide 0 to +10 values by 2;  
 ±5V range: divide ±10V range values by 2; ±2.5V range: divide ±10V range values by 4.

Table 3. Output Voltage Range Connections-Voltage