1.1 Scope.

This specification covers the detail requirements for a 12-bit resolution A/D converter with complete microprocessor interface and a high performance reference.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number[1]
– 1	AD674BT(X)/883B
– 2	AD774BT(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
D	D-28	28-Pin Ceramic DIP

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{CC} to Digital Common ..... +16.5 V
V_{EE} to Digital Common ..... −16.5 V
V_{LOGIC} to Digital Common ..... +7 V
Analog Common to Digital Common ..... ±1 V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... −0.5 V to V_{LOGIC} +0.5 V
Analog Inputs (REF IN, BIP OFF, 10 V_{IN}) to Analog Common ..... V_{EE} to V_{CC}
20 V_{IN} to Analog Common ..... ±24 V
REF OUT ..... Indefinite Short to Common
Momentary Short to V_{CC}
Power Dissipation ..... 470 mW
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... +300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 25°C/W
θ_{JA} = 60°C/W

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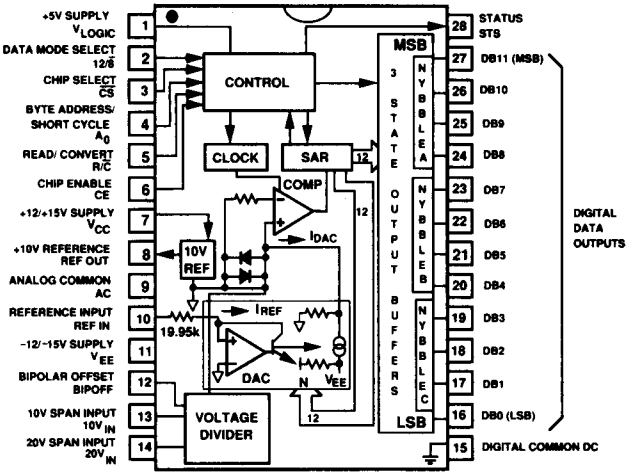
Table 1.

Test	Symbol	Device	Design Limit @+25°C	Sub Group 1	Sub Group 2, 3	Test Condition[1]	Unit
Power Dissipation	P_D	−1, 2	375	375	375	Tristated Outputs	mW max
Input Resistance	R_{IN}	−1, 2	3	3		10 V Span	kΩ min
			7	7			kΩ max
			6	6		20 V Span	kΩ min
			14	14			kΩ max
Internal Reference Output Voltage	V_{REF}	−1, 2	+9.9	+9.9		Bipolar 20 V Span 2.0 mA External Load	V min
			+10.1	+10.1			V max
Logic Input High Voltage CE, $\overline{CS}$, R/$\overline{C}$, A_0	V_{IH}	−1, 2	2.0	2.0	2.0		+V min
Logic Input Low Voltage CE, $\overline{CS}$, R/$\overline{C}$, A_0	V_{IL}	−1, 2	0.8	0.8	0.8		+V max
Logic Input Current CE, $\overline{CS}$, R/$\overline{C}$, A_0	I_{LIN}	−1, 2	10	10	10	V_{IH} = 5.0 V; V_{IL} = 0.0 V	±μA max
Logic Output High Voltage DB11–DB0	V_{OH}	−1, 2	2.4	2.4	2.4	I_{SOURCE} = 500 μA	+V min
Logic Output Low Voltage DB11–DB0, STS	V_{OL}	−1, 2	0.4	0.4	0.4	I_{SINK} = 1.6 mA	+V max
Three-State Output Leakage DB11–DB0	I_{OLT}	−1, 2	10	10	10	Outputs Tristated V_{IH} = 5.0 V	±μA max
Power Supply Current	I_L I_{CC} I_{EE}	−1, 2	7 7 14	7 7 14	7 7 14	Outputs Tristated REF OUT to REF IN Through 50 Ω	mA max
Integral Nonlinearity	INL	−1, 2	1/2	1/2	1	Major Transitions Unipolar 10 V Span Bipolar 20 V Span	±LSB max
Differential Nonlinearity[2]	DNL	−1, 2	12	12	12	All Codes Tested Unipolar 10 V Span Bipolar 20 V Span	Bits min
Power Supply Rejection[3]	PSR	−1, 2	1	1	1	See Note 4 Unipolar 10 V Span	±LSB max
			1/2	1/2	1/2	See Note 5	
			1	1	1	See Note 6	
Unipolar Offset Error	U_{OSE}	−1, 2	2	2		10 V Span	±LSB max
Unipolar Offset Drift	TCU_{OSE}	−1, 2			1	10 V Span	±LSB max
Bipolar Offet Error	B_{POE}	−1, 2	3	3		20 V Span	±LSB max
Bipolar Offset Drift	TCB_{POE}	−1, 2			2	20 V Span	±LSB max
Full-Scale Calibration Error	A_B	−1, 2	0.125	0.125		Bipolar 20 V Span	±% of FSR max
	A_U	−1, 2	0.125			Unipolar 10 V Span	
Full-Scale Calibration Drift	TCA_E	−1, 2			7	Bipolar 20 V Span	±LSB max

Test	Symbol	Device	Design Limit @+25°C	Sub Group 9	Sub Group 10, 11	Test Condition[1]	Unit
Conversion Time	t_C	−1	10	10	10	To 8-Bits	µs max
			15	15	15	To 12-Bits	µs max
		−2	6	6	6	To 8-Bits	µs max
			8	8	8	To 12-Bit	µs max
Converter Start Timing[7]							
STS Delay from CE	t_{DSC}	−1, 2	200	200	225	Timing per Figure 1	ns max
CE Pulse Width	t_{HEC}	−1, 2	50	50	50	Timing per Figure 1	ns min
$\overline{CS}$ to CE Setup	t_{SSC}	−1, 2	50	50	50	Timing per Figure 1	ns min
$\overline{CS}$ Low During CE High	t_{HSC}	−1, 2	50	50	50	Timing per Figure 1	ns min
R/$\overline{C}$ to CE Setup	t_{SRC}	−1, 2	50	50	50	Timing per Figure 1	ns min
R/$\overline{C}$ Low During CE High	t_{HRC}	−1, 2	50	50	50	Timing per Figure 1	ns min
A_0 to CE Setup	t_{SAC}	−1, 2	0	0	0	Timing per Figure 1	ns min
A_0 Valid During CE High	t_{HAC}	−1, 2	50	50	50	Timing per Figure 1	ns min
Read Timing–Full Control Mode[7]							
Access Time	t_{DD}	−1, 2	150	150	150	Load per Figure 3a	ns max
Data Valid After CE Low	t_{HD}	−1, 2	25	25	15	Timing per Figure 2	ns min
Output Float Delay	t_{HL}	−1, 2	150	150	150	Load per Figure 3b	ns max
$\overline{CS}$ to CE Setup	t_{SSR}	−1, 2	50	50	50	Timing per Figure 2	ns min
R/$\overline{C}$ to CE Setup	t_{SRR}	−1, 2	0	0	0	Timing per Figure 2	ns min
A_0 to CE Setup	t_{SAR}	−1, 2	50	50	50	Timing per Figure 2	ns min
$\overline{CS}$ Valid After CE Low	t_{HSR}	−1, 2	0	0	0	Timing per Figure 2	ns min
R/$\overline{C}$ High After CE Low	t_{HRR}	−1, 2	0	0	0	Timing per Figure 2	ns min
A_0 Valid After CE Low	t_{HAR}	−1, 2	50	50	50	Timing per Figure 2	ns min
Stand-Alone Mode Timing[7]							
Data Access Time	t_{DDR}	−1, 2	150	150	150	Timing per Figures 4a and 4b	ns max
Low R/$\overline{C}$ Pulse Width	t_{HRL}	−1, 2	50	50	50	Timing per Figures 4a and 4b	ns min
STS Delay from R/$\overline{C}$	t_{DS}	−1, 2	200	200	225	Timing per Figures 4a and 4b	ns max
Data Valid After R/$\overline{C}$ Low	t_{HDR}	−1, 2	25	25	25	Timing per Figures 4a and 4b	ns min
STS Delay After Data Valid	t_{HS}	−1, 2	30	30	30	Timing per Figures 4a and 4b	ns min
			600	600	600	Timing per Figures 4a and 4b	ns max
High R/$\overline{C}$ Pulse Width	t_{HRH}	−1, 2	150	150	150	Timing per Figures 4a and 4b	ns min

NOTES
[1]V_{CC} = +15 V, V_{EE} = −15 V, V_{LOGIC} = +5 V, 12/$\overline{8}$ connected to V_{LOGIC}, A_0 and $\overline{CS}$ at Logic "0," CE at Logic "1."
10 V Unipolar—50 Ω resistor Pin 8 to Pin 10, 50 Ω resistor Pin 12 to ground. Analog input connected to Pin 13.
20 V Bipolar—50 Ω resistor Pin 8 to Pin 12, 50 Ω resistor Pin 8 to Pin 10. Analog input connected to Pin 14.
See Figures 1, 2, 3 and 4 for timing information.
[2]Minimum resolution for which no missing codes are guaranteed.
[3]Change in the full-scale unipolar 10 V span as power supply voltage is varied from min to max specified value.
[4]Test conditions for PSRR: 13.5 V ≤ V_{CC} ≤ 16.5 V, V_{LOGIC} = 5 V, V_{EE} = −15 V; 11.4 V < V_{CC} ≤ 12.6 V, V_{LOGIC} = 5 V, V_{EE} = −12 V.
[5]4.5 V ≤ V_{LOGIC} ≤ 5.5 V, V_{CC} = 15 V, V_{EE} = −15 V.
[6]−16.5 V ≤ V_{EE} ≤ −13.5 V, V_{LOGIC} = 5 V, V_{CC} = 15 V; −12.6 V ≤ V_{EE} ≤ −11.4 V, V_{LOGIC} = 5 V, V_{CC} = 12 V.
[7]Timing tests are guaranteed from −55°C to +125°C.

3.2.1 Functional Block Diagram and Terminal Assignments.

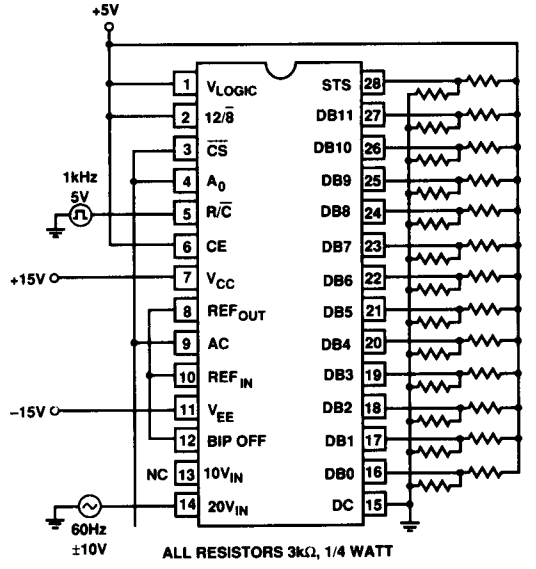


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (57).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 Test Condition (B).



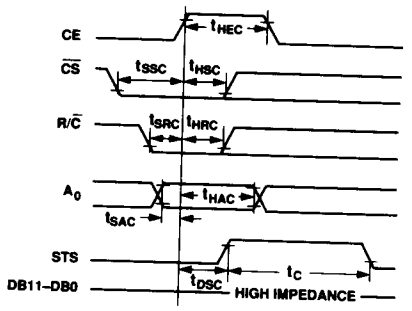


Figure 1. Converter Start Timing

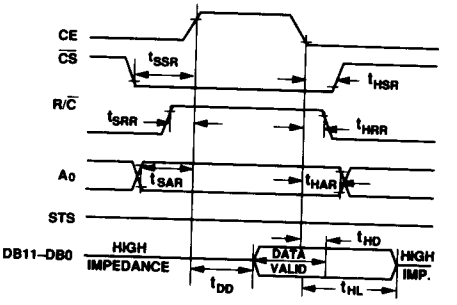
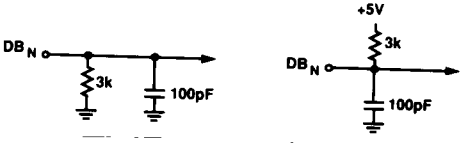


Figure 2. Read Timing



High-Z to Logic 1 High-Z to Logic 0

Figure 3a. Load Circuit for Access Time Test

Logic 1 to High-Z Logic 0 to High-Z

Figure 3b. Load Circuit for Output Float Delay Test

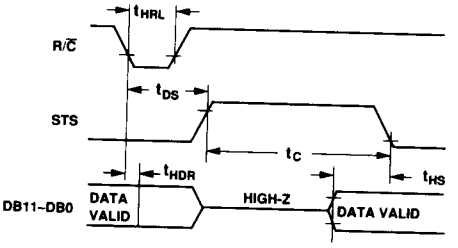


Figure 4a. Stand-Alone Mode Timing Low Pulse for R/C

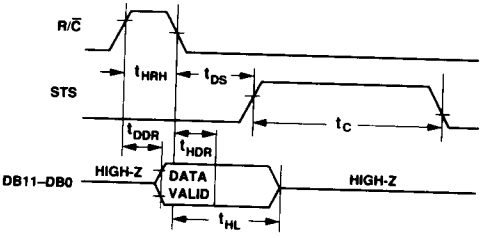


Figure 4b. Stand-Alone Mode Timing High Pulse for R/C

Table 2. AD674B/AD774BA Truth Table

CE	CS	R/C	12/8	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4 LSBs and 4 Trailing Zeroes