1.1 Scope.

This specification covers the detail requirements of 4- and 8-channel high speed 8-bit A/D converters. The AD7824 provides 4 multiplexed analog inputs, while the AD7828 provides 8. A half-flash conversion technique gives a conversion rate of 2.5μs per channel and the parts have a built-in track/hold function capable of digitizing full-scale signals of up to 10kHz on all channels.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number[1]
−1	AD7824TQ/883B and AD7828T(X)883B
−2	AD7824UQ/883B and AD7828U(X)883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-24 for AD7824

(X)	Package	Description
Q	Q-28	28-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} . . . . . 0V, +7V
Digital Input Voltage to GND ($\overline{RD}$, $\overline{CS}$, A0, A1 & A2) . . . . . −0.3V, V_{DD}
Digital Output Voltage to GND (DB0, DB7, RDY & $\overline{INT}$) . . . . . −0.3V, V_{DD}
V_{REF} (+) to GND . . . . . V_{REF} (−), V_{DD}
V_{REF} (−) to GND . . . . . 0V, V_{REF} (+)
Analog Input (Any Channel) . . . . . −0.3V, V_{DD}
Operating Temperature Range . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10sec) . . . . . +300°C
Power Dissipation
Up to +75°C 450mW
Derates above +75°C by . . . . . 6mW/°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24, Q-28 and E-28A
θ_{JA} = 120°C/W for Q-24, Q-28 and E-28A

AD7824/AD7828—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1, 2	8				This is the minimum resolution for which no missing codes are guaranteed.	Bits
Total Unadjusted Error[2]	TUE	−1	1	1	1			± LSB max
		−2	1/2	1	1/2	1/2		
Analog Input Voltage Range	V_{IN}	−1, 2	$V_{REF}(-)$					V min
			$V_{REF}(+)$					V max
Analog Input Leakage Current	I_{IN}	−1, 2	3	3	3		(Any Channel)	± μA max
Analog Input Capacitance		−1, 2	45				0V to +5V	pF typ
Reference Input Resistance	R_{IN}	−1, 2	1	1	1			kΩ min
			4	4	4			kΩ max
Digital Input High Level	V_{IH}	−1, 2	2.4	2.4	2.4		A0, A1 & A2, $\overline{RD}$, $\overline{CS}$	V min
Digital Input Low Level	V_{IL}	−1, 2	0.8	0.8	0.8		A0, A1 & A2, $\overline{RD}$, $\overline{CS}$	V max
Digital Input High Current	I_{IN}	−1, 2	1.0	1.0	1.0		$\overline{CS}$, $\overline{RD}$, A0, A1 & A2	μA max
Digital Input Low Current	I_{IL}	−1, 2	−1.0	−1.0	−1.0		$\overline{CS}$, $\overline{RD}$, A0, A1 & A2	μA max
Digital Input Capacitance	C_{IN}	−1, 2	8.0				$\overline{CS}$, $\overline{RD}$, A0, A1 & A2	pF max
Digital Output High Level	V_{OH}	−1, 2	4.0	4.0	4.0		DB0–DB7, $\overline{INT}$ I_{SOURCE} = 360μA	V min
Digital Output Low Level	V_{OL}	−1, 2	0.4	0.4	0.4		DB0–DB7, $\overline{INT}$ I_{SINK} = 1.6mA	V max
Digital Output Low Level[3]	V_{OL}	−1, 2	0.4	0.4	0.4		RDY; I_{SINK} = 2.6mA	V max
Floating State Leakage Current	I_{OUT}	−1, 2	3.0	3.0	3.0		DB0–DB7	μA max
Digital Output Capacitance	C_{OUT}	−1, 2	8.0					pF max
Slew Rate, Tracking		−1, 2	0.157					V/μs max
Supply Current from V_{DD}	I_{DD}	−1, 2	16.0	20.0	20.0		$\overline{CS}$ = $\overline{RD}$ = 2.4V	mA max
Power Supply Sensitivity		−1, 2	1/4	1/4	1/4		V_{DD} = 5V ± 5%	± LSB max
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CS}	−1, 2	0					ns min
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CSH}	−1, 2	0					ns min
$\overline{CS}$ to RDY Delay. Pull-Up Resistor 5kΩ[4]	t_{RDY}	−1, 2	60				40ns max at +25°C	ns max
Conversion Time, Mode 0	t_{CRD}	−1, 2	2.8	2.0	2.8		2.0μs max at +25°C	μs max
Data Access Time after $\overline{RD}$[5]	t_{ACC1}	−1, 2	120				85ns max at +25°C	ns max
$\overline{RD}$ to INT Delay[4]	t_{INTH}	−1, 2	100				75ns max at +25°C	ns max
Data Hold Time[6]	t_{DH}	−1, 2	70				60ns max at +25°C	ns max
Delay Time Between Conversions	t_P	−1, 2	600				500ns min at +25°C	ns min
Read Pulse Width, Mode 1	t_{RD}	−1, 2	80					ns min
			400					ns max
Data Access Time After INT, Mode 0[5]	t_{ACC2}	−1, 2	70				50ns max at +25°C	ns max
Multiplexer Address Setup Time	t_{AS}	−1, 2	0					ns min
Multiplexer Address Hold Time	t_{AH}	−1, 2	40					ns min

NOTES

[1] V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V unless otherwise specified. Specifications apply for Mode 0. All input control signals are specified with $t_r = t_f$ = 20ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

[2] Total unadjusted error includes offset, full scale and linearity errors.

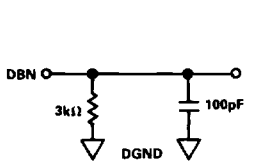
[3] RDY in an open drain output.

[4] C_L = 50pF.

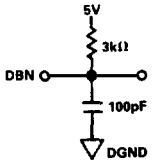
[5] Measured with load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.

[6] Defined as the time required for the date lines to change 0.5V when loaded with the circuits of Figure 2.

Test Circuits

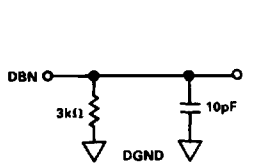


a. High-Z to V_{OH}

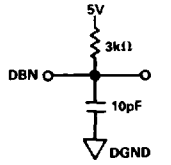


b. High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test



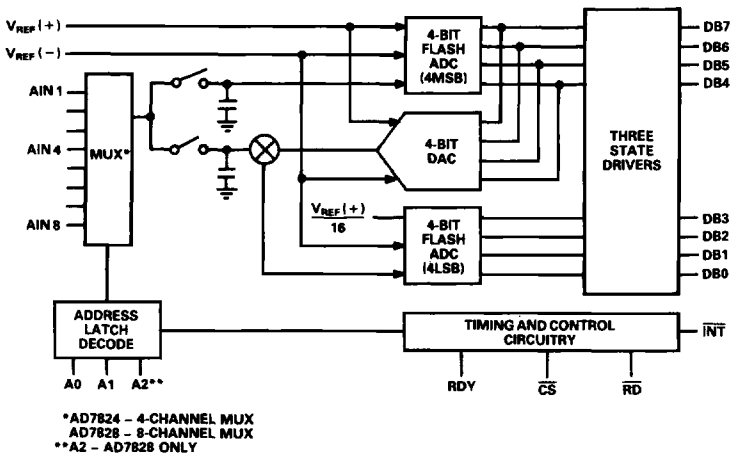
a. V_{OH} to High-Z



b. V_{OL} to High-Z

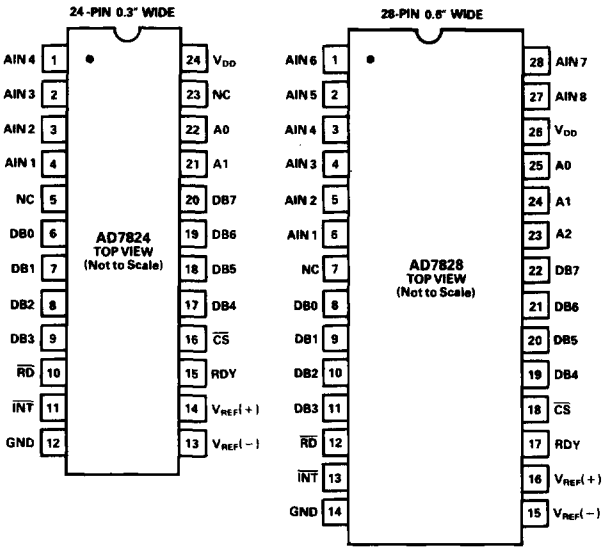
Figure 2. Load Circuits for Data Hold Time Test

3.2.1 Functional Block Diagram and Terminal Assignments.

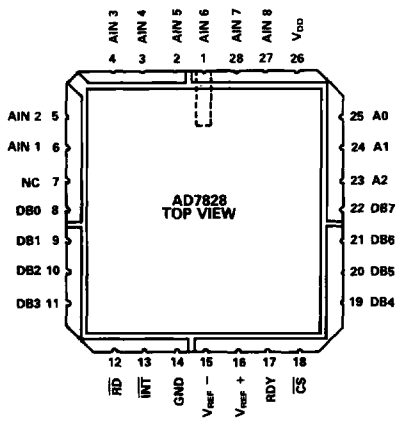


*AD7824 – 4-CHANNEL MUX
AD7828 – 8-CHANNEL MUX
**A2 – AD7828 ONLY

Q Package (Cerdip)



E Package (LCC)

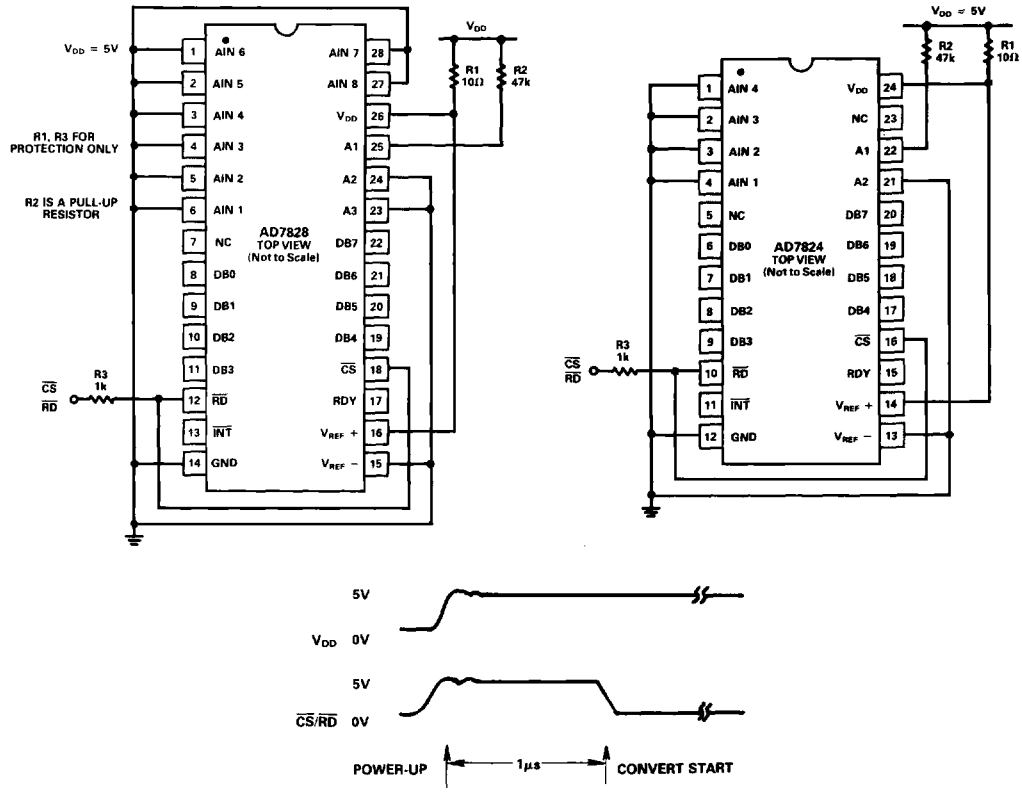


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



AD7824/AD7828 Burn-In Philosophy

After power-up the device performs a conversion on $\overline{CS}$ /$\overline{RD}$ going low. AIN 1 and AIN 4 are tied to ground so the device will output the all zeros code, thus putting the output drive N-channels under maximum stress for the period of burn-in.

The pull-up resistor on the A1 pin will stress this input inverter during burn-in to show up drifts in input logic threshold. Address input A2 is tied to ground causing the initial conversion to occur on channel 2. $\overline{CS}$ and $\overline{RD}$, require 0V to maintain all zeros on the 3-state outputs.

Apart from the conversion on power-up the device is burned-in the static mode taking a maximum I_{DD} of 15mA from the 5V supply.

5.0 Timing and Control.

The AD7824/AD7828 have two digital inputs for timing and control. These are Chip Select ($\overline{CS}$) and Read ($\overline{RD}$). A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which starts a conversion and latches the multiplexer address inputs (see Table 2). There are two modes of operation as outlined by the timing diagrams of Figures 3 and 4. Mode 0 is designed for microprocessors which can be driven into a WAIT state. A READ operation (i.e., $\overline{CS}$ and $\overline{RD}$ are taken low) starts a conversion and data is read when conversion is complete. Mode 1 does not require microprocessor WAIT states. A READ operation initiates a conversion and reads the previous conversion results.

Table 2. Truth Table for Input Channel Selection

AD7824		AD7828			CHANNEL
A1	A0	A2	A1	A0	
0	0	0	0	0	AIN 1
0	1	0	0	1	AIN 2
1	0	0	1	0	AIN 3
1	1	0	1	1	AIN 4
		1	0	0	AIN 5
		1	0	1	AIN 6
		1	1	0	AIN 7
		1	1	1	AIN 8

5.1 Mode 0.

Figure 3 shows the timing diagram for Mode 0 operation. This mode can only be used for microprocessors which have a WAIT state facility, whereby a READ instruction cycle can be extended to accommodate slow memory devices. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which latches the analog multiplexer address inputs and starts a conversion. The data bus (DB7-DB0) remains in the three-state condition until conversion is complete. There are two converter status outputs on the AD7824/AD7828, interrupt ($\overline{INT}$) and ready (RDY) which can be used to drive the microprocessor READY/WAIT input. The RDY is an open drain output (no internal pull-up device) which goes low on the falling edge of $\overline{CS}$ and $\overline{RD}$ and goes high impedance at the end of conversion, when the 8-bit conversion result appears on the data outputs. If the RDY output status is not required, then the external pull-up resistor can be omitted. The $\overline{INT}$ input goes low when conversion is complete and returns high on the rising edge of $\overline{CS}$ or $\overline{RD}$.

5.2 Mode 1.

Mode 1 operation is designed for applications where the microprocessor is not forced into a WAIT state. A READ operation takes $\overline{CS}$ and $\overline{RD}$ low, which latches the multiplexer address inputs and triggers a conversion (see Figure 4). Data from the previous conversion is read from the three-state data outputs (DB7-DB0). This data may be disregarded if not required. The RDY output (open drain output) is low for the duration of the READ operation and goes high impedance on the rising edge of $\overline{CS}$ or $\overline{RD}$. If the RDY output status is not required, then the external pull-up resistor can be omitted. At the end of conversion $\overline{INT}$ goes low. A second READ operation is required to access the new conversion result. This READ operation latches a new address into the multiplexer inputs and starts another conversion. $\overline{INT}$ returns high at the end of the second READ operation, when $\overline{CS}$ and $\overline{RD}$ returns high. A delay of 2.5μs must be allowed between READ operations.

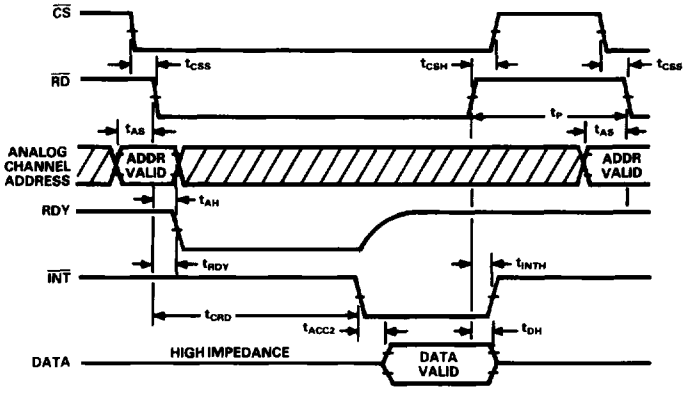


Figure 3. Mode 0 Timing Diagram

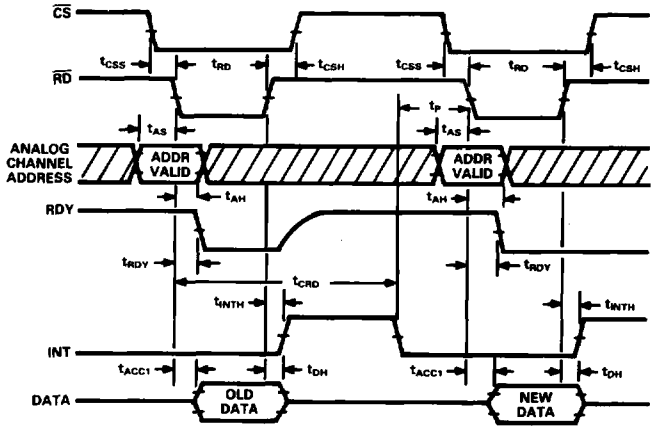


Figure 4. Mode 1 Timing Diagram