ANALOG DEVICES

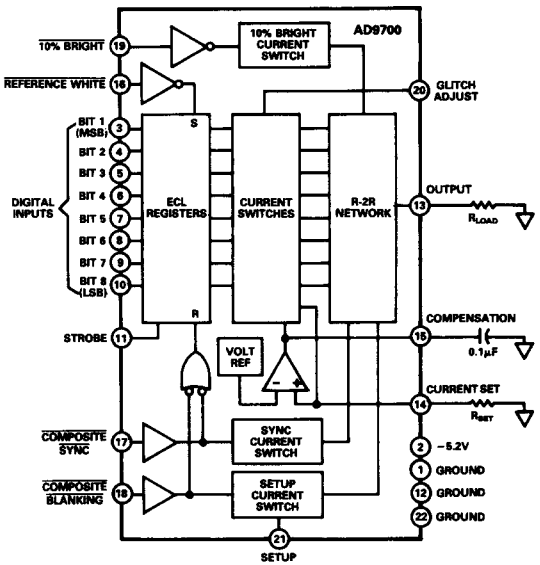
Monolithic Video D/A Converter

AD9700

FEATURES
- Update Rates to 125MHz
- Low Glitch Energy
- Complete Composite Inputs
- On-Chip Reference Voltage
- Single −5.2V Power Supply

APPLICATIONS
- Raster Scan Displays
- Color Graphics
- Automated Test Equipment
- TV Video Reconstruction

AD9700 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9700 digital-to-analog converter is a monolithic device capable of accepting eight bits of digital data at update rates as high as 125MHz. On-chip registers on the data lines help minimize "glitches" in the output signal.

Incorporating the AD9700 into system designs is eased by its blanking, sync, 10% brightness, and reference white control signals. An on-board reference eliminates the need for external circuits, making it considerably easier to design the AD9700 into high-speed applications than it is for converters which do not have this feature.

The unit is housed in a 22-pin package; operates from a single −5.2V power supply; and dissipates only 650mW, making this the smallest, lowest power D/A converter available to design engineers who need true "graphics ready" converters for raster scan, color graphics, and other high-speed systems.

This device is a natural extension of the Analog Devices advanced technology that produced the first hybrid converters which included composite capabilities. Like the earlier HDG-Series D/A converters, the AD9700 is designed to have general output compatibility with EIA Standards RS-170 and RS-343.

Five versions of the AD9700 are available. The AD9700BW (non-hermetic) and AD9700BD (hermetic) are DIP units operating over a temperature range of −25°C to +85°C; the hermetic DIP AD9700SD is for use over a temperature range of −55°C to +125°C. The AD9700BE and AD9700SE are leadless chip carrier (LCC) devices for temperature ranges of −25°C to +85°C and −55°C to +125°C, respectively.

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	AD9700BD/BW[1]	AD9700SD[2]
RESOLUTION	Bits	8	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (adjustable)	mV	2.5	*
Current (adjustable)	μA	67	*
ACCURACY (GS = Gray Scale; FS = Full Scale)			
Linearity	± % GS	0.2	*
Differential Linearity	± % GS, max	0.2	*
Integral Linearity	± % GS, max	0.2	*
Zero Offset (Initial) Voltage	mV (max)	0.3 (0.9)	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C (max)	15	* (30)
Gain	ppm/°C (max)	50	* (125)
Zero Offset	ppm/°C (max)	10	* (15)
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[3]			
Settling Time to 0.4% GS; 0V to 637.5mV GS change			
Voltage	ns (max)	10 (12)	*
Update Rate[4]	MHz (min)	125 (100)	*
Slew Rate	V/μs	300	*
Rise Time	ns	2	*
Glitch Impulse[5]	pV-s	80	*
DIGITAL DATA INPUTS			
Logic Compatibility		ECL[6]	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT			
Logic Compatibility		ECL[6]	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
Setup Time (Data)	ns, min	2.5	*
Hold Time (Data)	ns, min	1.5	*
Propagation Delay	ns (max)	4 (5)	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		ECL[6]	*
Logic Levels			
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS			
Settling Time to 10% of Final Value for:			
10% Bright	ns, max	10	*
Reference White	ns, max	10	*
Composite Sync	ns, max	10	*
Composite Blanking	ns, max	10	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	53.25 (7.5)	*
1k to −5.2V	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*
ANALOG OUTPUT			
GS Current[7]	mA	0 to −17	*
GS Voltage[8]	mV (± 1%)	0 to −637.5	*
Compliance	V	−1.2 to +0.1	*
Internal Impedance	Ω (min/max)	800 (680/920)	*
REFERENCE WHITE[9]			
Current			
Logic "1"	mA (± 5%)	Normal Operation	*
Logic "0"	mA (± 3%)	0 or −1.9	*
Voltage			
Logic "1"	mV (± 3%)	Normal Operation	*
Logic "0"	mV (± 3%)	0 or −71	*
10% BRIGHT[10]			
Current			
Logic "1"	mA (± 5%)	−1.9	*
Logic "0"	mA (± 5%)	0	*
Voltage			
Logic "1"	mV (± 5%)	−71	*
Logic "0"	mV (± 5%)	0	*

Parameter	Units	AD9700BD/BW[1]	AD9700SD[2]
COMPOSITE SYNC[10,11]			
Current			
Logic "1"	mA (±5%)	0	*
Logic "0"	mA (±5%)	−7.6	*
Voltage			
Logic "1"	mV (±5%)	0	*
Logic "0"	mV (±5%)	−285	*
COMPOSITE BLANKING[10,11]			
(Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)			
Current			
Logic "1"	mA (±5%)	0	*
Logic "0"	mA (±5%)	−1.4	*
Voltage			
Logic "1"	mV (±5%)	0	*
Logic "0"	mV (±5%)	−53.25	*
VOLTAGE REFERENCE TOLERANCE			
(Deviation from Nominal −1.26V)	mV (max)	±20 (±60)	*
POWER REQUIREMENTS			
−5.2V ±0.25V	mA (max)	125 (155)[12]	125 (155)[12]
Power Supply Rejection Ratio	%/V	0.025/0.25	*
Power Dissipation	mW (max)	650 (728)	*
TEMPERATURE RANGE			
Operating (Case)	°C	−25 to +85	−55 to +125
Storage	°C	−55 to +150	*
THERMAL RESISTANCE[13]			
Junction to Air, θja (Free Air)	°C/W, max	55	*
Junction to Case, θjc	°C/W, max	15	*
MTBF[14]			
Mean Time Between Failures	Hours	1.95×10^5	*
PACKAGE OPTIONS[15]			
Ceramic (D-22)		AD9700BD AD9700BW	AD9700SD
Cerdip (Q-22)		AD9700BD	AD9700SD
LCC (E-28A)		AD9700BE	AD9700SE

For applications assistance, phone (919) 668-9511.

NOTES
[1]Electrical specifications for AD9700BE same as AD9700BD/BW.
[2]Electrical specifications for AD9700SE same as AD9700SD.
[3]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.
[4]Minimum update rate limited by full-scale settling time for eight bits. Unit can be updated to 125MHz.
[5]Glitch can be reduced with glitch adjustment.
[6]See Figure 2 for operation with TTL logic.
[7]FS current = GS current + video functions = 30mA.
[8]LSB value of 2.5mV used for calibration. This causes Gray Scale output to to be 637.5mV rather than 643mV shown in idealized composite waveform elsewhere in this data sheet; both values are well within the output and EIA Standard RS-170 tolerances. $I_{OUT} = (1.26/R_{SET}) \times 4$ when $R_{SET} = 300\Omega$.
[9]Effect on analog output of logic "0" at Reference White input depends on signal at 10% Bright input (see Table I).
[10]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray Scale analog output at Pin 13.
[11]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White.
[12]Maximums shown are at temperature extremes.
[13]Maximum junction temperature = +150°C.
[14]Calculated using MIL HNBK-217; Ground Fixed; +25°C Ambient.
[15]See Section 14 for package outline information.
*Specifications same as AD9700BD/BW.
Specifications subject to change without notice.

PIN CONFIGURATIONS

MODELS AD9700BD, AD9700BW, and AD9700SD

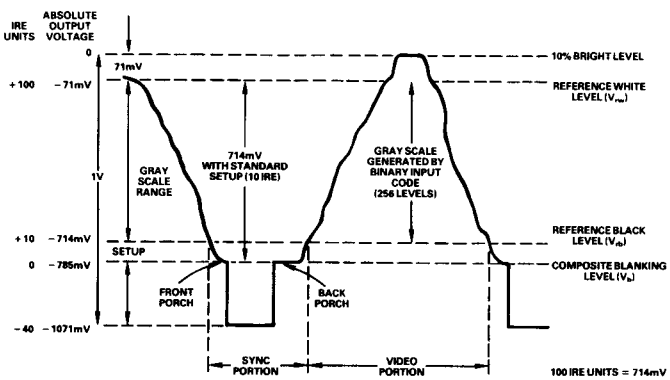
PIN	FUNCTION	PIN	FUNCTION
1	GROUND	12	GROUND
2	−5.2V	13	OUTPUT
3	BIT 1 (MSB)	14	CURRENT SET
4	BIT 2	15	COMPENSATION
5	BIT 3	16	REFERENCE WHITE
6	BIT 4	17	COMPOSITE SYNC
7	BIT 5	18	COMPOSITE BLANKING
8	BIT 6	19	10% BRIGHT
9	BIT 7	20	GLITCH ADJUST
10	BIT 8 (LSB)	21	SETUP
11	STROBE	22	GROUND

NOTE: CONNECT PINS 1, 12, AND 22 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.

MODELS AD9700BE, AD9700SE

PIN	FUNCTION	PIN	FUNCTION
1	GROUND	15	GROUND
2	GROUND	16	OUTPUT
3	GROUND	17	−5.2V
4	−5.2V	18	CURRENT SET
5	BIT 1 (MSB)	19	COMPENSATION
6	BIT 2	20	REFERENCE WHITE
7	BIT 3	21	COMPOSITE SYNC
8	BIT 4	22	NO CONNECTION
9	BIT 5	23	COMPOSITE BLANKING
10	BIT 6	24	10% BRIGHT
11	BIT 7	25	GLITCH ADJUST
12	BIT 8	26	SETUP
13	STROBE	27	−5.2V
14	NC	28	V_{BB}

NOTE: CONNECT PINS 1, 2, 3, AND 15 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.



Idealized Composite Output Waveform

DIGITAL INPUTS VS. ANALOG OUTPUT

Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	10% Bright	Ref. White	Comp. Blanking	Comp. Sync	Analog Output (mV)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.50[1]
X	X	X	X	X	X	X	X	0	1	0	1	−690.75[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.50[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.50[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.50[1]
X	X	X	X	X	X	X	X	0	1	0	0	−975.75[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.50[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.50[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.50[1]
X	X	X	X	X	X	X	X	1	1	0	0	−1046.75[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.50[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.50[4]

NOTES
[1]Setup (Pin 21) grounded (0 IRE units).
[2]Setup (Pin 21) open (7.5 IRE units).
[3]Setup (Pin 21) to −5.2V through 1k (10 IRE units).
[4]Setup (Pin 21) to −5.2V (20 IRE units).

Analog output values shown are based on LSB value of 2.5mV used for ease of calibration; this causes Gray Scale output to be 637.5mV rather than 643mV shown elsewhere in this data sheet in sketch of idealized composite output. Both values are well within the output and EIA Standard RS-170 tolerances.

Table I.

USING AD9700 AS RASTER SCAN D/A

Refer to the block diagram of the AD9700 D/A converter.

The digital input bits represent the Gray Scale value of the 256 (2^8) discrete levels between Reference Black and Reference White in a composite video signal, and are applied to Pins 3 through 10.

The output analog signal (at Pin 13) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, Reference White, Composite Sync, and Composite Blanking; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs and various combinations of control inputs are selected.

Refer to Table I.

As the footnote to this figure points out, the full-scale (−637.5mV) output of the AD9700 is different from the −643mV output of the idealized composite waveform shown elsewhere in this data sheet. The reason for this discrepancy is Analog Devices' use of 2.5mV for the value of the LSB; that choice of LSB weighting eases calibration of the converter. The disparity does not cause any problems in using the device, since both values are well within the tolerances of the output and the RS-170 standard.

Referring again to the block diagram, the Strobe input applied to the AD9700 clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize pertubations or "glitches" in the analog output signal.

The signal applied to the Reference White input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the AD9700 goes to 0V or to −71mV, depending upon whether or not the 10% Bright signal is also operated.

A logic "0" applied to either the Composite Sync or Composite Blanking input will reset the input registers to 00000000. The analog output at Pin 13 will be −922.5mV (−637.5mV plus −285mV) if the Composite Sync input is operated; this is not affected by the value of IRE units at the setup input.

When Composite Blanking is operated, the analog output will go to its full-scale value of −637.5mV plus some additional amount, as determined by the voltage at setup. The −53.25mV example used in the specifications section of the data sheet is based on the setup input floating, which is equivalent to 7.5 IRE units. (For this example, the analog output would be 690.75mV.)

The internal voltage reference shown in the block diagram is a bandgap type. Including this reference within the converter eliminates the need for external circuits, making it markedly easier to design the AD9700 into various applications. The internal precision reference also provides superior power supply rejection and gain tempco.

Details on the connections for using the AD9700 in composite video applications are shown in Figure 1.

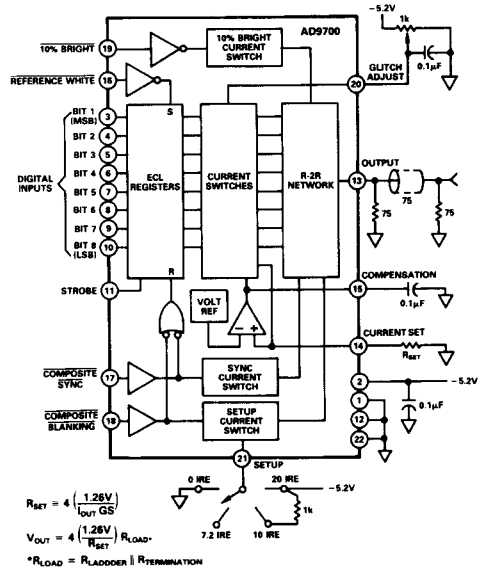


Figure 1. AD9700 D/A Connections

The value of R_{SET} can be established by using the first of the two equations which are part of the connection illustration; in the formula, the 1.26 volts is the reference voltage. When that voltage is divided by the desired Gray Scale current, the value which results is approximately one-fourth the resistance of R_{SET}.

The resistance of R_{SET}, in turn, can be used in the calculation of analog output voltage when the AD9700 is operating as a raster scan D/A converter. The full-scale current of the device is the Gray Scale current plus the video functions, and is specified at 30mA total. The user needs to keep that number in mind to assure that the AD9700 is utilized correctly in circuit designs.

In some instances, the user may be driving a lighter load than the coaxial cable shown in Figure 1 and prefers to operate with lower power dissipation than that in high speed raster scan use. For these situations, the value of R_{SET} can be doubled, which halves the output current while still maintaining a useable current drive from the converter. Power dissipation would be reduced approximately 75mW; the trade-off to obtain this is a decrease in the speed of the AD9700 and a lengthening of settling time.

Ground pins 1, 12, and 22 are shown connected together and to ground near the unit; this is the recommended procedure for obtaining optimum performance, especially in high-speed applications. Inside the AD9700, Pin 1 is register ground; Pin 12 is analog ground; and Pin 22 is digital ground.

For some applications, in addition to by-passing the −5.2V supply with 0.01μF as shown, it may be desirable to by-pass it also with a tantalum capacitor of 3.3 – 10μF. Although this is not generally necessary, it may enhance the converter's performance in some designs.

The circuit connected to Pin 21 setup is used for illustrative purposes to demonstrate the relationships of various IRE units; it is not intended to imply this is the preferred way to obtain these values. At Pin 20, the circuit used for adjusting the glitch can reduce the amount of glitch from its typical 50pV-s to a lesser value for those applications which require it.

USING AD9700 IN TTL MODE

Most applications using the AD9700 for composite video reconstruction will be in ECL systems, but there may be instances where its high-performance characteristics need to be applied in TTL designs.

A method of accomplishing this is illustrated in Figure 2.

Except as shown, all input pull-up resistors which are used are the same value: 2kΩ. If some of the input bit connections are not used because of operating with fewer than eight bits of resolution, the unused input pins should be resistively connected to +5V to prevent undesirable side effects in the performance of the converter.

This same technique of resistively connecting unused inputs to +5V also applies for the Reference White, Composite Sync, and Composite Blanking inputs. If 10% Bright is not used, Pin 19 should be either grounded or left open; no pull-up resistor should be used.

The table which is part of Figure 2 shows the required connections to Pin 21 for the various blanking levels when operating in the TTL mode.

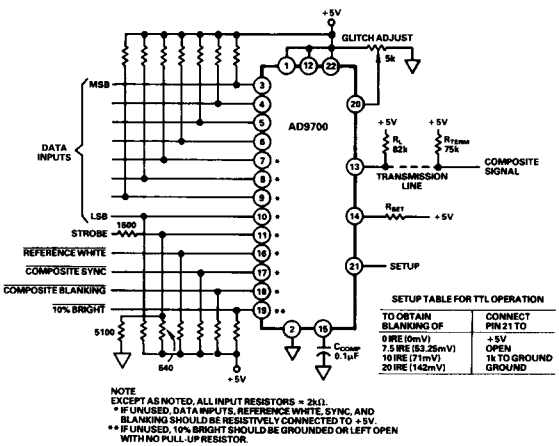


Figure 2. Using AD9700 in TTL Mode

USING AD9700 AS STANDARD D/A

Although designed for use in composite video applications, the AD9700 can also be utilized as a standard D/A converter with remarkable performance. The extremely low glitch energy of the unit makes it especially attractive, because video reconstruction can be accomplished with exceptional spectral purity.

Refer to Figure 3.

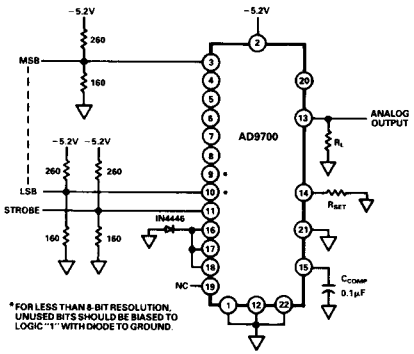


Figure 3. AD9700 as Standard D/A

When used as a standard D/A, the unused control inputs required for video applications are connected to ground; in most cases, this connection is made through a diode. Examples of that are shown on Pins 16, 17, and 18, the inputs for Reference White, Composite Sync, and Composite Blanking, respectively. The 10% Bright input (Pin 19) is left open, and setup (Pin 21) is tied directly to ground.

If fewer than eight bits of digital input will be applied, the unused input pins should be connected to ground via a diode with the same technique used at Pins 16, 17, and 18. If they are tied directly to ground, converter performance may be affected adversely.

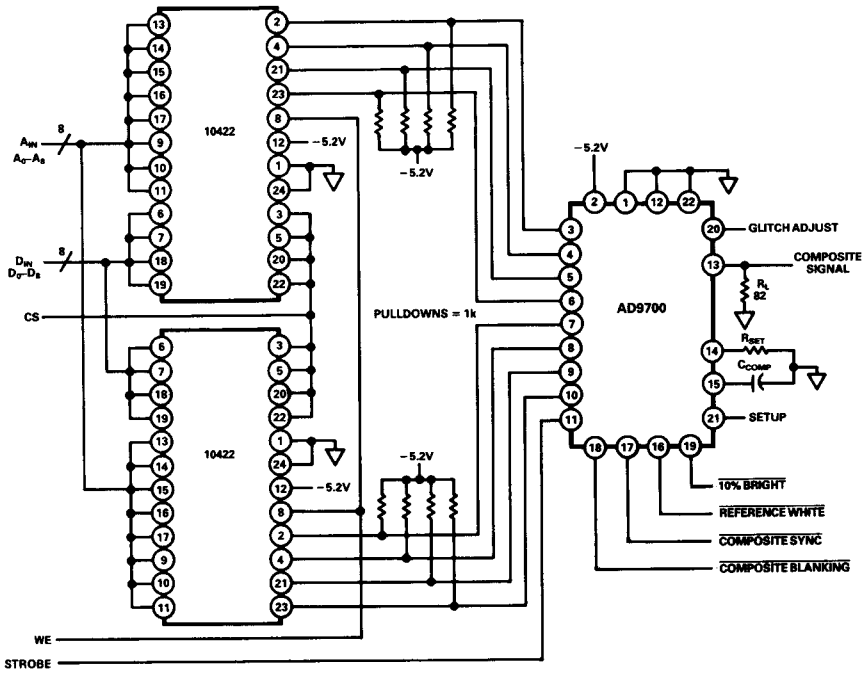


Figure 4. Using the AD9700 with Look-Up Table

USING AD9700 WITH RANDOM ACCESS MEMORY

In many applications, it may be necessary to operate the AD9700 D/A converter with look-up tables (LUT's) for raster scan display applications. One possible way to operate with fast random access memory (RAM) is shown in Figure 4.

If the user is interested in obtaining an RGB video subsystem, the circuit which is shown would be repeated three times. The Address Bus (A_{IN}), Data Bus (D_{IN}), Write enable (WE), and Strobe lines for the three would be connected in parallel. During write operations, the appropriate Chip Select (CS) line would be operated to control which RAM will receive data on the Data Bus.

Data are written into the RAM during an inactive portion of the scan cycle. The full tables can be written during the vertical retrace time; or small blocks of data can be written during the horizontal retrace. Write cycle timing requirements for the 10422 RAM which is illustrated are shown in Figure 5.

The major advantage of the configuration recommended here is realized during the read mode of the RGB system. In the method illustrated in Figure 4, all three D/A converter outputs are updated simply by changing the 8-bit address. Refer to Figure 6.

This illustrates the timing relationships and the intervals for the various operations which occur during the read cycle of the LUT.

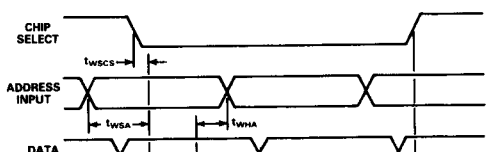


Figure 5. LUT Write Cycle Timing Diagram

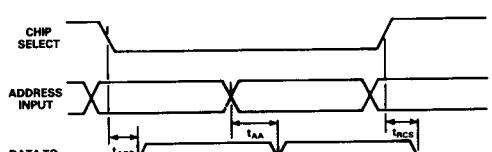


Figure 6. LUT Read Cycle Timing Diagram