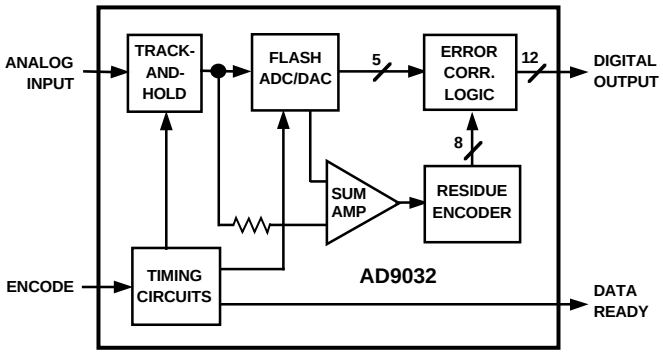
12-Bit 25 MSPS A/D Converter

AD9032

FEATURES
25.6 MSPS Conversion Speeds
On-Board T/H, References, Timing
Low Power: 3.8 W
Single 40-Pin Package
74 dB Spurious-Free Dynamic Range to 12 MHz A_{IN}
Bipolar Input: ±1.024 V

APPLICATIONS
Radar
Signal Intelligence
Digital Spectrum Analyzers
Medical Imaging
Electro-Optics

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9032 is the world's fastest 12-bit analog-to-digital converter (ADC) that includes on-board T/H, voltage references, and timing circuits. The AD9032 uses a subranging converter architecture to achieve sample rates from dc to 25.6 MSPS. Packaged in a single 40-pin hybrid, the AD9032 is pin-compatible with the AD9034, which operates at word rates up to 20 MSPS.

This ECL-compatible ADC requires only +5 V and –5.2 V supplies, an analog input, and a stable ECL clock to obtain the best dynamic performance available in a 12-bit ADC. This kind of performance is achieved with advanced bipolar circuits, custom designed and manufactured by Analog Devices. The latest in monolithic track-and-hold technology ensures accurate sampling of high frequency analog inputs.

Dynamic performance has been optimized to achieve SNR of 64 dB and a spurious-free dynamic range (SFDR) of 74 dB for analog bandwidths up to 12 MHz. All units are tested for dynamic performance at a sample rate of 25.6 MSPS.

The AD9032 is available in either a 40-pin ceramic DIP or leaded flatpack. The two versions operate over an industrial (–25°C to +85°C) or military (–55°C to +125°C) temperature range.

EVALUATION BOARD

An evaluation board which is available for the AD9032 (part number AD9034/PCB) provides an easy and flexible method for evaluating the ADC's performance without (or prior to) developing a user-specified printed circuit board. The evaluation board was originally designed and used for evaluating the AD9034 A/D converter, but is equally useful for the pin-compatible AD9032.

The board includes a reconstruction DAC, analog input amplifier, and digital output interface. Physically, it is 7.25 inches × 6 inches in size and uses the layout and applications information contained in the AD9034 data sheet.

Generous space is provided near the analog input and digital outputs of the evaluation board to support additional signal processing components the user may wish to add. These two prototyping areas include through holes with 100-mil centers to support a variety of component additions.

For additional operating details, a schematic of the evaluation board, and complete layout information, consult the data sheet on the AD9034 A/D converter.

REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 **Fax: 617/326-8703**

AD9032–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS ($+V_S$ = +5 V; $-V_S$ = –5.2 V, Encode = 25.6 MSPS, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	AD9032AD/AZ Typ	AD9032AD/AZ Max	AD9032BD/BZ Min	AD9032BD/BZ Typ	AD9032BD/BZ Max	AD9032TD/TZ Min	AD9032TD/TZ Typ	AD9032TD/TZ Max	Units
RESOLUTION			12			12			12			Bits
DC ACCURACY												
Differential Nonlinearity	+25°C	I		0.65	1.25		0.5	1.0		0.5	1.0	LSB
	Full	VI			1.75			1.5			1.5	LSB
Integral Nonlinearity	+25°C	V		1.0			1.0			1.0		LSB
	Full	V		2.0			2.0			2.0		LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed			Guaranteed		
Offset Error	+25°C	I		5	15		5	15		5	15	mV
	Full	VI			25			25			30	mV
Gain Error	+25°C	I		±0.5	±1.0		±0.5	±1.0		±0.5	±1.0	% FS
	Full	VI			±2.5			±2.5			±2.5	% FS
ANALOG INPUT												
Input Voltage Range	+25°C	I		±1.024			±1.024			±1.024		V
Input Resistance	+25°C	VI	95	100	105	95	100	105	95	100	105	Ω
Input Capacitance	+25°C	IV		7	10		7	10		7	10	pF
Analog Bandwidth	+25°C	IV	150	220		150	220		150	220		MHz
SWITCHING PERFORMANCE[1]												
Conversion Rate	Full	VI	dc		25.6	dc		25.6	dc		25.6	MSPS
Aperture Delay (t_A)	Full	IV	1	3	5	1	3	5	1	3	5	ns
Aperture Uncertainty (jitter)	Full	IV		4	8		4	8		4	8	ps, rms
Output Delay (t_{OD})	Full	IV	9	13	17	9	13	17	9	13	17	ns
Data Ready Delay (t_{DR})	Full	IV	3.5	7.5	10.5	3.5	7.5	10.5	3.5	7.5	10.5	ns
Output Time Skew	Full	IV		1	2		1	2		1	2	ns
ENCODE INPUT												
Logic "1" Voltage	Full	IV	–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	IV			–1.5			–1.5			–1.5	V
Logic "1" Current	Full	VI		150	300		150	300		150	300	µA
Logic "0" Current	Full	VI		150	300		150	300		150	300	µA
Input Capacitance	+25°C	V		10			10			10		pF
Pulse Width (High)	+25°C	IV	10			10			10			ns
Pulse Width (Low)	+25°C	IV	10			10			10			ns
DYNAMIC PERFORMANCE												
Transient Response	+25°C	IV		12	27		12	27		12	27	ns
Overvoltage Recovery Time	+25°C	IV		25	37		25	37		25	37	ns
Harmonic Distortion												
Analog Input @ 1.2 MHz	+25°C	I	70	80		75	82		75	82		dBc
@ 1.2 MHz	Full	VI	67			70			70			dBc
@ 4.3 MHz	+25°C	V		76			77			77		dBc
@ 9.6 MHz	+25°C	I	68	75		72	76		72	76		dBc
@ 9.6 MHz	Full	VI	64			68			64			dBc
@ 12.1 MHz	+25°C	V		72			74			74		dBc
Signal-to-Noise Ratio[2]												
Analog Input @ 1.2 MHz	+25°C	I	63	66		64	67		64	67		dB
@ 1.2 MHz	Full	VI	61			63			61			dB
@ 4.3 MHz	+25°C	V		64			65			65		dB
@ 9.6 MHz	+25°C	I	62	64		62	64		62	64		dB
@ 9.6 MHz	Full	VI	60			61			58			dB
@ 12.1 MHz	+25°C	V		64			64			64		dB
Two-Tone Intermodulation Distortion Rejection[3]	+25°C	V		66			68			68		dBc

Parameter (Conditions)	Temp	Test Level	AD9032AD/AZ Min	AD9032AD/AZ Typ	AD9032AD/AZ Max	AD9032BD/BZ Min	AD9032BD/BZ Typ	AD9032BD/BZ Max	AD9032TD/TZ Min	AD9032TD/TZ Typ	AD9032TD/TZ Max	Units
DIGITAL OUTPUTS (10K ECL)												
Logic "1" Voltage	Full	VI	–1.1			–1.1			–1.1			V
Logic "0" Voltage	Full	VI			–1.5			–1.5			–1.5	V
Output Coding			2s Complement			2s Complement			2s Complement			
POWER SUPPLY												
$+V_S$ Supply Voltage	Full	VI	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	mA
$+V_S$ Supply Current	Full	VI		133	160		133	160		133	160	mA
$-V_S$ Supply Voltage	Full	VI	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	–5.45	–5.2	–4.95	mA
$-V_S$ Supply Current	Full	VI		610	672		610	672		610	672	mA
Power Dissipation	Full	VI		3.8	4.5		3.8	4.5		3.8	4.5	W
Power Supply Rejection Ratio (PSRR)[4]	Full	VI		4.0	10		4.0	10		4.0	10	mV/V

NOTES
[1]Outputs terminated through 510 Ω to –5.2 V; C_L < 4 pF. Typical values are valid for +25°C ambient.
[2]RMS signal to rms noise with analog input signal 1 dB below full scale at specified frequency.
[3]Intermodulation measured with analog input frequencies of 9.3 MHz and 9.6 MHz at 7 dB below full scale.
[4]PSRR is sensitivity of offset error to power supply variations within the 5% limits shown.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_S$ . . . . . +7 V
$-V_S$ . . . . . –7 V
Analog Input . . . . . $-V_S$ to $+V_S$
Digital Inputs . . . . . $-V_S$ to 0 V
Digital Output Current . . . . . 20 mA
Operating Temperature Range
AD9032AD/BD/AZ/BZ . . . . . –25°C to +85°C
AD9032TD/TZ . . . . . –55°C to +125°C
Maximum Junction Temperature[2] +175°C
Lead Temperature (Soldering, 10 seconds) . . . . . +300°C
Storage Temperature Range . . . . . –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the service ability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances: θ_{CA} = 13°C/W; $T_J - T_C$ = 10°C max (worst case die junction temperature rise). See Thermal Management section.

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. Devices are 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/ industrial devices.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9032AD	–25°C to +85°C	40-Pin Ceramic DIP	DH-40A
AD9032AZ*	–25°C to +85°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9032BD	–25°C to +85°C	40-Pin Ceramic DIP	DH-40A
AD9032BZ*	–25°C to +85°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9032TD	–55°C to +125°C	40-Pin Ceramic DIP	DH-40A
AD9032TZ*	–55°C to +125°C	40-Pin Ceramic Leaded Chip Carrier	Z-40
AD9034/PWB	Printed Circuit Board (Only) of Evaluation Circuit		
AD9034/PCB	Complete Evaluation Board, Assembled and Tested (Order AD9032 DIP Separately)		

*Ceramic leaded chip carrier packages are tested and shipped with unformed leads. Consult the factory for availability.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Data Ready Delay (t_{DR})
The delay between the 50% point of the change in output data and the 50% point of the rising edge of DATA READY.

Differential Nonlinearity (DNL)
The deviation of any code width from an ideal 1 LSB step, as determined by a histogram.

Harmonic Distortion
The rms value of the fundamental divided by the rms value of the worst harmonic.

Integral Nonlinearity (INL)
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit, as determined by a histogram.

Output Delay (t_{OD})
The delay between the 50% point of the rising edge of the ENCODE command and the 50% point of the next change in output data.

Output Time Skew
Bit-to-bit time variations among D_0 to D_{11} outputs. Time skew includes HIGH-to-LOW and LOW-to-HIGH transitions of the digital output bits.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 12-bit accuracy after an analog input signal 150% of full scale is reduced to the midscale of the converter.

Power Supply Rejection Ratio
The ratio of a change in power supply voltage which results in a change in input offset voltage.

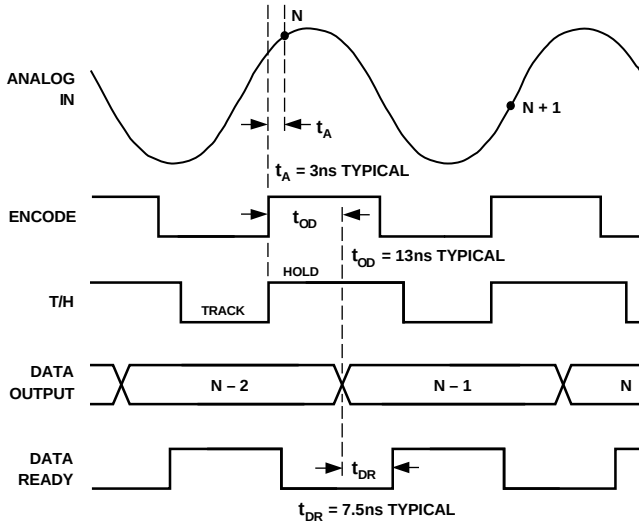
Pulse Width (High and Low)
Rated performance of the ADC is assured when stated restrictions on ENCODE pulse width shown in Specifications table are observed.

Signal-to-Noise Ratio (SNR)
The ratio of the rms signal amplitude to the rms value of "noise," which is defined as the sum of all other spectral components, including harmonics but excluding dc, with an analog input signal 1 dB below full scale.

Spurious Free Dynamic Range (SFDR)
The rms value of the fundamental divided by the rms value of the highest spurious signal. This is generally specified as a function of input signal level.

Transient Response
The time required for the converter to achieve 12-bit accuracy when a full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion (IMD) Rejection
The ratio of the power of either of two input signals to the power of the strongest third-order IMD signal.

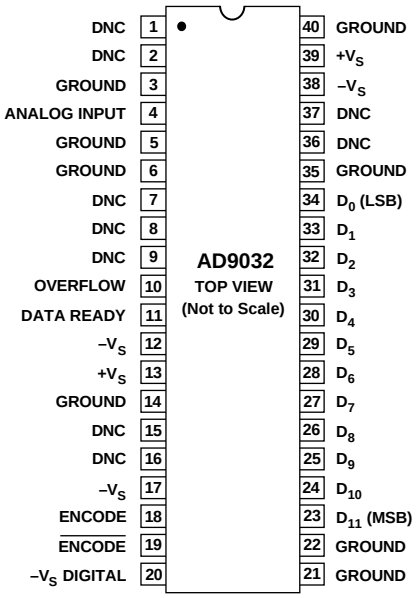


Timing Diagram

PIN DESCRIPTIONS

Pin	Name	Description
1	GAIN ADJUST	Can be used to null out initial gain error of ADC. Normally open.
2	OFFSET ADJUST	Can be used to null out initial offset error of ADC. Normally open.
3, 5, 6, 14, 21, 22, 35, 40	GROUND	All ground pins should be connected together and to low-impedance ground plane near AD9034.
4	ANALOG INPUT	Analog input to ADC, ±1.024 V input range; 100 Ω input resistance; 7 pF input capacitance.
7, 8, 9, 15, 16, 36, 37	DNC	Do not connect. Internal test points.
10	OVERFLOW	ECL-compatible output; normally low. High when analog input > +FS.
11	DATA READY	ECL-compatible output. Rising edge of signal suitable, for externally latching $D_0 - D_{11}$.
12, 17, 20, 38	$-V_S$	–5.2 V supply voltage.
13, 39	$+V_S$	+5.0 V supply voltage.
18	ENCODE	Differential ECL convert command.
19	$\overline{\text{ENCODE}}$	Sampling occurs on rising edge; no internal terminations.
23–34	D_0–D_{11}	ECL-compatible digital outputs; 2s complement coding.

PIN DESIGNATIONS



THEORY OF OPERATION

The AD9032 is a digitally corrected subranging analog-to-digital converter (ADC) optimized for fast sampling rates and dynamic range. Refer to the block diagram on the first page. The AD9032 is a vertically integrated structure consisting of a track-and-hold (T/H) amplifier, a combined flash ADC and digital-to-analog (DAC), a summation amplifier, digital error correction logic, and timing circuits. Reference circuits to generate stable DC voltages and currents that maintain the static accuracy of the device are also included, but are not shown on the block diagram.

Internally, the monolithic T/H (AD9101) provides fast settling and acquisition times while minimizing distortion introduced by the sampling process. The unique design of the sampling bridge allows accurate sampling of high slew rate signals with negligible distortion. The effects of jitter and other aperture errors have been reduced to provide dynamic performance previously unavailable in monolithic and discrete designs.

At the output of the T/H amplifier, the analog input is converted by the first (5-bit) ADC. This 12-bit representation of the input value is stored in the digital error correction logic. It is also converted back to an analog signal by the 14-bit-accurate DAC on the same chip with the ADC. The 32 DAC current sources are steered directly by the outputs of the 32 input comparators on the 5-bit ADC. This minimizes propagation delay through the DAC, and allows the summation of the DAC signal and the held output of the T/H to settle quickly. The hold time of the T/H is optimized to allow sufficient settling time without sacrificing the acquisition time necessary to acquire the next sample.

The residue signal, representing the difference between the 5-bit conversion (DAC output) and the input signal held by the T/H, is amplified by the summation amplifier. During the tracking period of the T/H, this residue signal can be much larger than the input range of the 8-bit ADC and would saturate the output stage of a normal amplifier. To protect the ADC and maintain fast settling times under all conditions, the summation amplifier is a custom design with clamping circuits that prevent saturation, limit the output voltage, and preserve settling time.

The 8-bit flash ADC determines the 7 least significant bits (LSBs) of the 12-bit conversion and generates a correction bit for any small errors created by inaccuracies in the first 5-bit conversion. This 8-bit signal and the 5-bit quantization are combined to obtain a 12-bit-accurate representation of the analog input voltage.

USING THE AD9032

Layout Information

Preserving the accuracy and dynamic performance of the AD9032 requires that designers pay special attention to the layout of the printed circuit board. Signal paths should be impedance matched and properly terminated at or near the package connections. Analog signal paths should be isolated from digital signal paths. Capacitive and inductive coupling of digital signals into analog signal sections can degrade the overall performance of the A/D converter.

Analog Input

The analog input pin of the AD9032 is terminated with a 100 Ω load. The analog input range of the AD9032 is factory trimmed for a ±1.024 V input for compatibility with the AD9034. The signal presented to the monolithic T/H is divided in half to optimize dynamic performance.

When the amplitude, bandwidth, or dc level of the analog input requires external signal conditioning, the selection of the input amplifier is of particular concern. The noise and distortion of the amplifier must be taken into account to preserve the dynamic range of the AD9032. The AD9617 wideband, current feedback amplifier is an excellent choice for most applications.

Timing

Internal timing for the AD9032 is trimmed at the factory to simplify use. Care should be taken to ensure that the encode command to the AD9032 is free from jitter that can degrade dynamic performance. Differential ECL inputs to the AD9032 can be derived from a single-ended source using a fast comparator such as the AD96685. The encode source should be located and terminated as close to the AD9032 as possible.

The ECL-compatible digital outputs are latched to provide valid data for the entire conversion period (less the transition region of latch). This data should be latched into external ECL registers located near the AD9032. External termination resistors are required (510 Ω recommended). The data are latched with either the encode command or the data ready signal provided on the AD9032. The rising edge of the data ready signal occurs typically 7.5 ns after the data changes.

Gain and Offset Adjustment

Gain and offset pins are normally not connected. Rated performance is guaranteed without any external connection to these pins. In most applications, wide variations in input signal range and offset can be accommodated using external amplifiers. However, in those applications where a vernier adjustment is required (such as nulling out factory trim limits), the gain and offset pins will provide sufficient adjustment range.

Both inputs offer a 20 kΩ input resistance that can be driven from a voltage source (DAC, amplifier) or the center tap of a potentiometer. The offset pin provides a 195 mV/V sensitivity to input offset, while the gain pin offers 120 mV/V adjustment of the full-scale input range of the ADC. The adjustment range for offset is limited to 10 mV and for gain is 20 mV without introducing potential dynamic errors or restricting the operating temperature range of the part.

Power Supplies

The unique design of the AD9032 provides excellent dynamic performance without a need for high voltage power supplies. Two supplies (+5 V and –5.2 V) are all that are required to achieve rated performance. Careful layout and decoupling of power supplies used in conjunction with a low impedance analog ground plane will reduce supply-related noise components.

Separate analog and digital supplies are not required. In applications with only limited analog supply current, a separate digital supply source can be used for the –5.2 V supply on Pin 20. This supply typically requires 310 mA (330 mA max) and may be shared with other ECL logic devices when isolated with bypass capacitors and/or ferrite bead inductors (Fair-Rite Products Corporation part # 2743001111, Wallkill, NY). Each power supply pin should be capacitively decoupled to the ground plane through a good high frequency ceramic capacitor (0.1 µF) and a single large value capacitor (tantalum 10 µF).

For optimum performance, "clean" linear supplies ensure that switching noise on the supplies does not introduce distortion products during the encoding process. Recognizing, however, that switching power supplies may be required in power-sensitive applications, decoupling recommendations outlined above are critically important for using switching supplies effectively. Elsewhere in this data sheet, a graph shows the PSRR of the AD9032 as a function of the ripple frequency present on the AD9032 supplies. Clearly, if they must be used, switching power supplies with the lowest possible frequency should be selected.

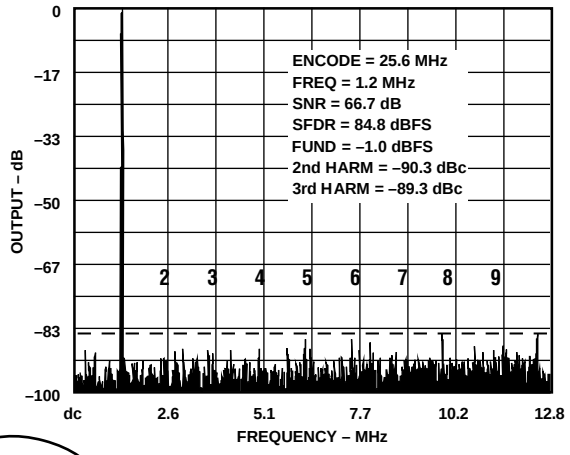
Thermal Management

The AD9032 design minimizes power dissipation; however, the ADC does typically require 3.8 W (4.5 W max) to operate. To ensure long life and reliable operation, the maximum junction temperature in the AD9032 must be limited to +175°C.

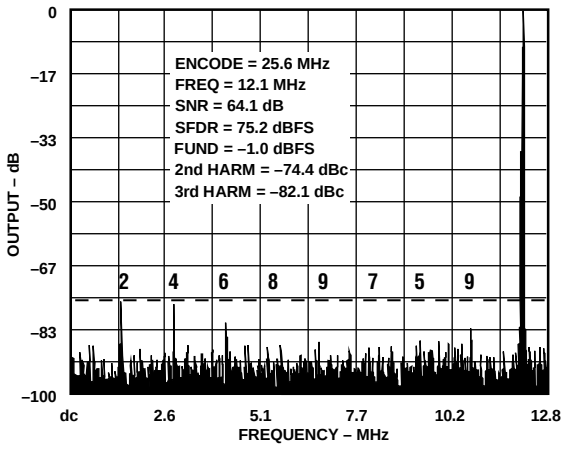
Within the hybrid, the hottest discrete die has a case to junction temperature rise of 10°C (max). Therefore, the case temperature of the AD9032 should not exceed +165°C under worst case operating conditions. Without airflow, the θ_{CA} of the hybrid package is 13°C/W. Assuming maximum power dissipation, this causes a 57°C rise in case temperature over the ambient air temperature. The maximum still air temperature, therefore, is equal to +108°C.

Rated performance of the AD9032 is guaranteed for case operating temperatures of +85°C (AD9032A/B) and +125°C (AD9032T). This equates to a maximum operating ambient temperature of +28°C and +68°C, respectively, in still air. In most applications, airflow is recommended. The following improvements in the thermal characteristics of the system assume that the AD9032 is soldered to a PC board.

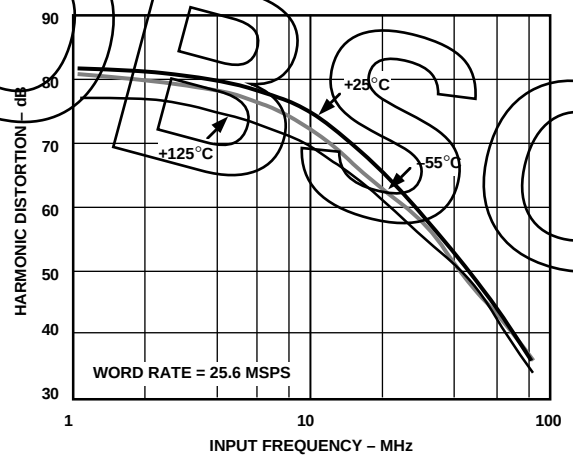
The θ_{CA} of the hybrid is reduced to 5°C/W with 500 LFPM airflow. This will extend the rated performance to ambient operating ranges of +63°C for the AD9032A/B and +103°C for the AD9032T. The addition of a heat sink (Thermalloy #6087B, Dallas, Texas; phone 214-243-0839) will further improve the thermal transfer of the hybrid to 3°C/W (@ 500 LFPM). Using a heat sink with airflow, the total case to ambient temperature rise is only 13°C, which results in a maximum ambient environment of +72°C (AD9032A/B) and +112°C (AD9032T).



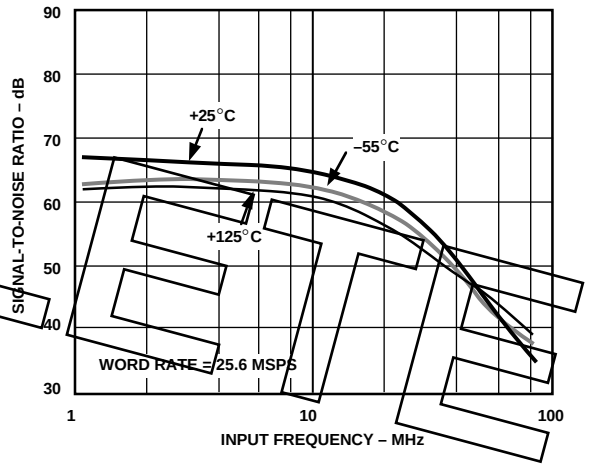
AD9032 A/D Converter FFT



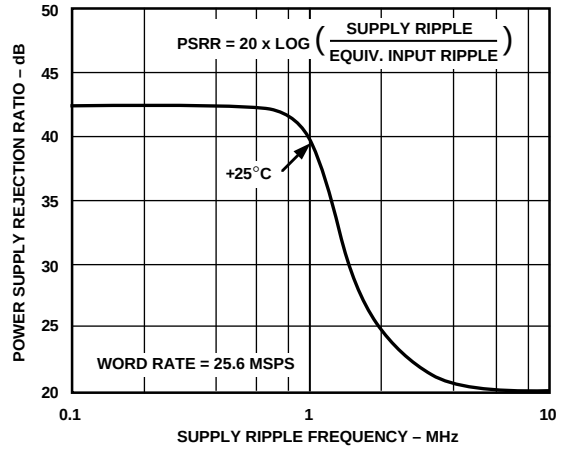
AD9032 A/D Converter FFT



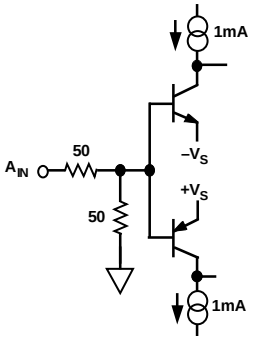
AD9032 Harmonic Distortion vs. Analog Input



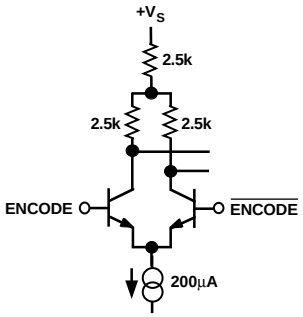
AD9032 SNR vs. Analog Input



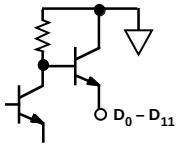
AD9032 PSRR vs. Supply Ripple Frequency



Equivalent Analog Input Circuit



Equivalent Encode Input Circuit

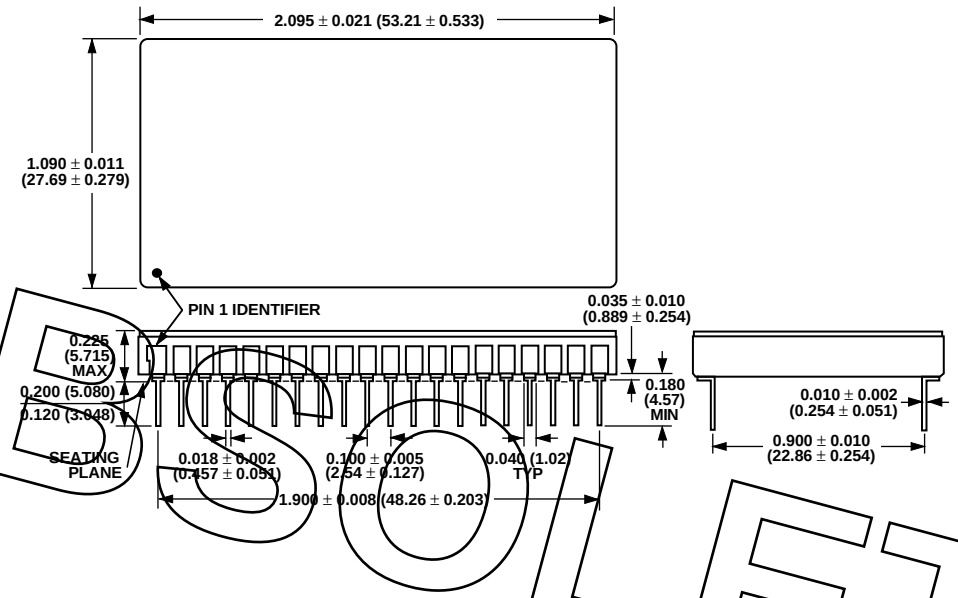


Equivalent Digital Output Circuit

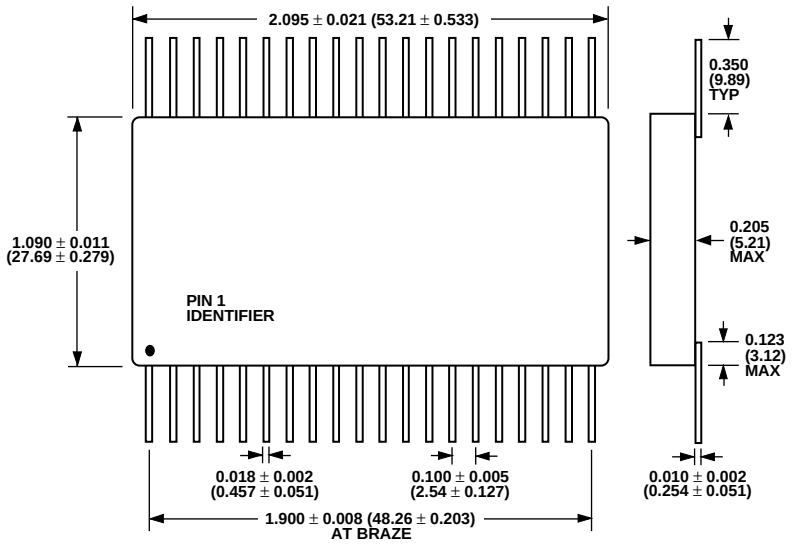
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

DH-40A
40-Lead Bottom Brazed Ceramic DIP



Z-40
40-Lead Leaded Flatpack



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