### 1.1 Scope.

This specification covers the detail requirements for a complete monolithic 12-bit, 5 Msps A/D converter with an on-chip, high performance track-and-hold amplifier (THA) and voltage reference.

### 1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

| Device | Part Number |
|---|---|
| −1 | AD871SD/883B |
| −2 | AD871SE/883B |



### 1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

| (X) | Package | Description |
|---|---|---|
| D | D-28 | 28-Pin Side Brazed Ceramic DIP |
| E | E-44A | 44-Pin LCC |

### 1.3 Absolute Maximum Ratings. ($T_A$ = +25°C unless otherwise noted)

$AV_{DD}$ to AGND ..... −0.5 V to +6.5 V
$AV_{SS}$ to AGND ..... −6.5 V to +0.5 V
$DV_{DD}$, $DRV_{DD}$ to DGND ..... −0.5 V to +6.5 V
AGND to DGND ..... −1 V to +1 V
$AV_{DD}$ to $DV_{DD}$ ..... −6.5 V to +6.5 V
Clock Input, OEN to DGND ..... −0.5 V to $DV_{DD}$ + 0.5 V
Digital Outputs to DGND ..... −0.5 V to $DV_{DD}$ + 0.3 V
REF IN to $AV_{DD}$ ..... $AV_{SS}$ to 0 V
REF IN to $AV_{SS}$ ..... 0 V to $AV_{DD}$
$V_{INA}$, $V_{INB}$, REF IN to AGND ..... −6.5 V to +6.5 V
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature Range (Soldering 10 sec) ..... +300°C

### 1.5 Thermal Characteristics.

Thermal Resistance: $\theta_{JC}$ = 25°C/W for D-28
$\theta_{JA}$ = 60°C/W for D-28
$\theta_{JC}$ = 42°C/W for E-44A
$\theta_{JA}$ = 70°C/W for E-44A

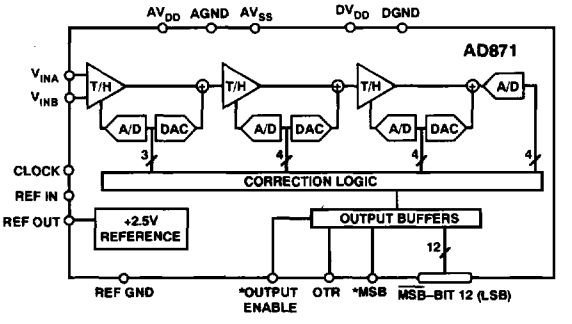
# AD871—SPECIFICATIONS

Table 1.

| Test | Symbol | Device | Design Limit @ +25°C | Sub Group 1 | Sub Group 2, 3 | Test Condition | Units |
|---|---|---|---|---|---|---|---|
| Resolution | RES | −1 | 12 | 12 | 12 | | Bits |
| Differential Nonlinearity[1] | DNL | −1 | 12 | 12 | 12 | All Codes Histogram | Bits |
| Zero Error | $B_{POE}$ | −1 | 0.75 | 0.75 | | | ±% FSR max |
| Gain Error | $A_E$ | −1 | 1.25 | 1.25 | | | ±% FSR max |
| Zero Error Drift | $TCB_{POE}$ | −1 | | | 0.30 | External 2.5 V Reference | ±% FSR max |
| Gain Error Drift | $TCA_{INT}$ | −1 | | | 1.75 | Internal 2.5 V Reference | ±% FSR max |
| Gain Error Drift | $TCA_{EXT}$ | −1 | | | 0.5 | External 2.5 V Reference | ±% FSR max |
| Power Supply Rejection | PSR | −1 | 0.125 | 0.125 | 0.125 | See Note 2 | ±% FSR max |
| Analog Input Range | $V_{IN}$ | −1 | 1 | 1 | 1 | | ±V max |
| Input Resistance | $R_{IN}$ | −1 | 50 | | | | kΩ |
| Input Capacitance | $C_{IN}$ | −1 | 10 | | | | pF |
| Internal Reference Output Voltage | $V_{REF}$ | −1 | 2.46 | 2.46 | 2.46 | | V min |
| | | | 2.54 | 2.54 | 2.54 | | V max |
| Power Dissipation | PD | −1 | 1.3 | 1.3 | 1.3 | | Watts max |
| Power Supply Current | $I_{AVDD}$ | −1 | 88 | 88 | 88 | | mA max |
| | $I_{AVSS}$ | | 150 | 150 | 150 | | |
| | $I_{DVDD}$ | | 21 | 21 | 21 | | |
| | $I_{DRVDD}$[3] | | 2 | 2 | 2 | | |
| Signal-to-Noise and Distortion Ratio | S/(N+D) | −1 | 62 | 62 | 62 | $f_{IN}$ = 1 MHz; $f_S$ = 5 MHz | dB min |
| | | −2 | 60 | 60 | 60 | | |
| Total Harmonic Distortion | THD | −1 | −63 | −63 | −63 | $f_{IN}$ = 1 MHz; $f_S$ = 5 MHz | dB max |
| | | −2 | −60 | −60 | −60 | | |
| Logic Input High Voltage | $V_{IH}$ | −1 | 2.0 | 2.0 | 2.0 | | V min |
| Logic Input Low Voltage | $V_{IL}$ | −1 | 0.8 | 0.8 | 0.8 | | V max |
| Logic Input High Current (CLK, OEN[3]) | $I_{IH}$ | −1 | 10 | 10 | 10 | | ±μA max |
| Logic Input Low Current (CLK, OEN[3]) | $I_{IL}$ | −1 | 10 | 10 | 10 | | ±μA max |
| Logic Output High Voltage ($\overline{MSB}$–Bit 12, OTR) | $V_{OH}$ | −1 | 2.4 | 2.4 | 2.4 | $I_{SOURCE}$ = 500 μA | V min |
| Logic Output Low Voltage ($\overline{MSB}$–Bit 12, OTR) | $V_{OL}$ | −1 | 0.4 | 0.4 | 0.4 | $I_{SINK}$ = 1.6 mA | V min |
| Leakage[3] | $I_Z$ | −1 | 10 | 10 | 10 | Three-State | ±μA max |
| Clock Period | $t_C$ | −1 | 200 | 200 | 200 | | ns min |
| Output Delay | $t_{OD}$ | −1 | 10 | 10 | 10 | | ns min |
| Pipeline Delay | $t_{PD}$ | −1 | 3 | | | | Clock Cycles max |
| Clock Pulse Width High | $t_{CH}$ | −1 | 95 | | | | ns min |
| Clock Pulse Width Low | $t_{CL}$ | −1 | 95 | | | | ns min |
| Clock Duty Cycle | $D_{CYC}$ | −1 | 40 | | | | % min |
| | | | 60 | | | | % max |

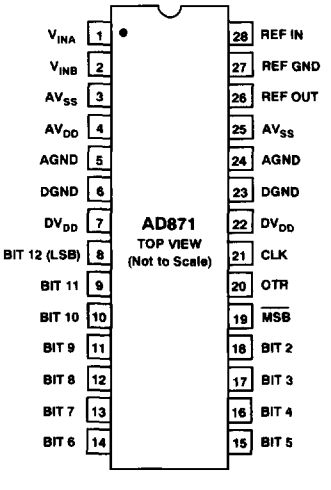
NOTES
[1]Minimum resolution for which "no missing codes" is guaranteed.
[2]Test conditions for PSR: 4.75 V ≤ $AV_{DD}$ ≤ 5.25 V, −5.25 V ≤ $AV_{SS}$ ≤ −4.75 V, 4.75 V ≤ $DV_{DD}$ ≤ 5.25 V.
[3]E-44A package only.

### 3.2.1 Functional Block Diagram and Terminal Assignments.

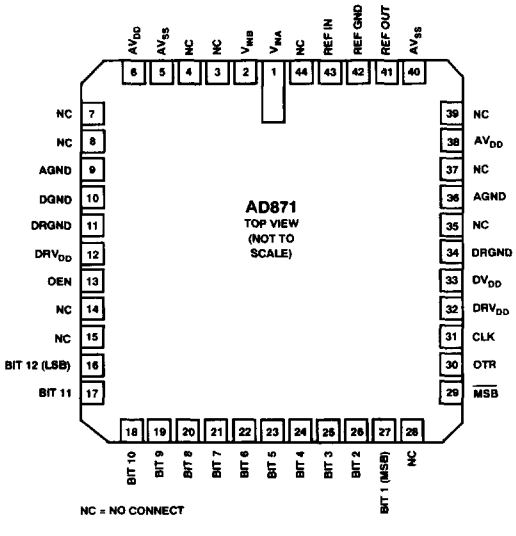



*ONLY AVAILABLE ON 44-PIN SURFACE MOUNT PACKAGE.

**D Package**




**E Package**



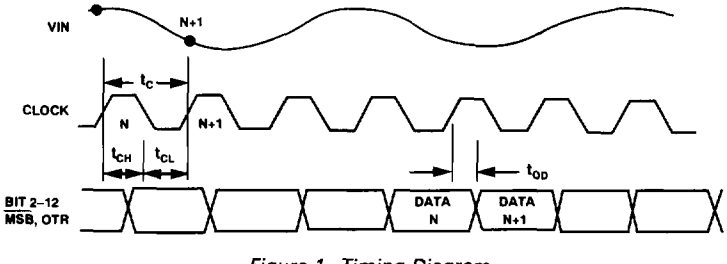




*Figure 1. Timing Diagram*

### 3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (93).

### 4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).