19-2917; Rev 1; 1/04

500mW, Low EMI, Filterless, Class D Audio Amplifier

MAX9712

General Description

The MAX9712 mono class D audio power amplifier provides class AB amplifier performance with class D efficiency, conserving board space, and extending battery life. Using a class D architecture, the MAX9712 delivers up to 500mW into an 8Ω load while offering efficiencies above 85%. A low EMI modulation scheme renders the traditional class D output filter unnecessary.

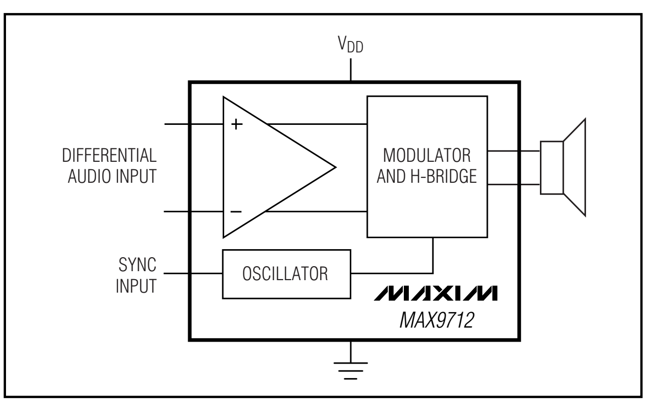
The MAX9712 offers two modulation schemes: a fixed-frequency (FFM) mode, and a spread-spectrum (SSM) mode that reduces EMI-radiated emissions due to the modulation frequency. Furthermore, the MAX9712 oscillator can be synchronized to an external clock through the SYNC input, allowing the switching frequency to be user defined. The SYNC input also allows multiple MAX9712s to be cascaded and frequency locked, minimizing interference due to clock intermodulation. The device utilizes a fully differential architecture, a full-bridged output, and comprehensive click-and-pop suppression. The gain is internally set to +4V/V, further reducing external component count.

The MAX9712 features high 72dB PSRR, a low 0.01% THD+N, and SNR in excess of 90dB. Short-circuit and thermal-overload protection prevent the device from damage during a fault condition. The MAX9712 is available in 10-pin TDFN (3mm × 3mm × 0.8mm), 10-pin µMAX, and 12-bump UCSP™ (1.5mm × 2mm × 0.6mm) packages. The MAX9712 is specified over the extended -40°C to +85°C temperature range.

Applications

Cellular Phones	MP3 Players
PDAs	Portable Audio

Simplified Block Diagram



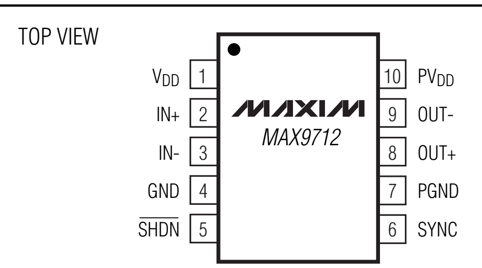
Features

- ♦ **Filterless Amplifier Passes FCC Radiated Emissions Standards with 100mm of Cable**
- ♦ **Unique Spread-Spectrum Mode Offers 5dB Emissions Improvement Over Conventional Methods**
- ♦ **Optional External SYNC Input**
- ♦ **Simple Master-Slave Setup for Stereo Operation**
- ♦ **85% Efficiency**
- ♦ **Up to 500mW into 8Ω**
- ♦ **Low 0.01% THD+N**
- ♦ **High PSRR (72dB at 217Hz)**
- ♦ **Integrated Click-and-Pop Suppression**
- ♦ **Low Quiescent Current (4mA)**
- ♦ **Low-Power Shutdown Mode (0.1µA)**
- ♦ **Short-Circuit and Thermal-Overload Protection**
- ♦ **Available in Thermally Efficient, Space-Saving Packages**
  - **10-Pin TDFN (3mm × 3mm × 0.8mm)**
  - **10-Pin µMAX**
  - **12-Bump UCSP (1.5mm × 2mm × 0.6mm)**

Ordering Information

PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX9712ETB	-40°C to +85°C	10 TDFN	AAI
MAX9712EUB	-40°C to +85°C	10 µMAX	—
MAX9712EBC-T	-40°C to +85°C	12 UCSP-12	ABN

Pin Configurations



TDFN/µMAX

Pin Configurations continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

500mW, Low EMI, Filterless, Class D Audio Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND 6V
PV_{DD} to PGND 6V
GND to PGND ....-0.3V to +0.3V
All Other Pins to GND.................................-0.3V to (V_{DD} + 0.3V)
Continuous Current Into/Out of PV_{DD}/PGND/OUT_ ....±600mA
Continuous Input Current (all other pins)..........................±20mA
Duration of OUT_ Short Circuit to GND or PV_{DD}........Continuous
Duration of Short Circuit Between OUT+ and OUT- ..Continuous

Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951.2mW
10-Pin µMAX (derate 5.6mW/°C above +70°C).........444.4mW
12-Bump UCSP (derate 6.1mW/°C above +70°C)........484mW
Junction Temperature...+150°C
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Bump Temperature (soldering)
Reflow ....+235°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = $\overline{SHDN}$ = 3.3V, GND = PGND = 0V, SYNC = GND (FFM), R_L = 8Ω, R_L connected between OUT+ and OUT-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	V_{DD}	Inferred from PSRR test		2.5		5.5	V
Quiescent Current	I_{DD}				4	5.2	mA
Shutdown Current	I_{SHDN}				0.1	5	µA
Turn-On Time	t_{ON}				30		ms
Input Resistance	R_{IN}	T_A = +25°C		14	20		kΩ
Input Bias Voltage	V_{BIAS}	Either input		0.73	0.83	0.93	V
Voltage Gain	A_V			3.8	4	4.2	V/V
Output Offset Voltage	V_{OS}	T_A = +25°C	MAX9712EUB/MAX9712ETB		±11	±40	mV
			MAX9712EBC		±15	±65	
		$T_{MIN} \le T_A \le T_{MAX}$	MAX9712EUB/MAX9712ETB			±65	
			MAX9712EBC			±95	
Common-Mode Rejection Ratio	CMRR	f_{IN} = 1kHz, input referred			72		dB
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{DD} = 2.5V to 5.5V		50	70		dB
		200mV_{P-P} ripple	f_{RIPPLE} = 217Hz		72		
			f_{RIPPLE} = 20kHz		55		
Output Power	P_{OUT}	THD+N = 1%	R_L = 16Ω, V_{DD} = 5V		700		mW
			R_L = 8Ω		450		
			R_L = 6Ω		250		
Total Harmonic Distortion Plus Noise	THD+N	f_{IN} = 1kHz, either FFM or SSM	R_L = 8Ω, P_{OUT} = 125mW		0.01		%
			R_L = 6Ω, P_{OUT} = 125mW		0.01		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = $\overline{SHDN}$ = 3.3V, GND = PGND = 0V, SYNC = GND (FFM), R_L = 8Ω, R_L connected between OUT+ and OUT-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

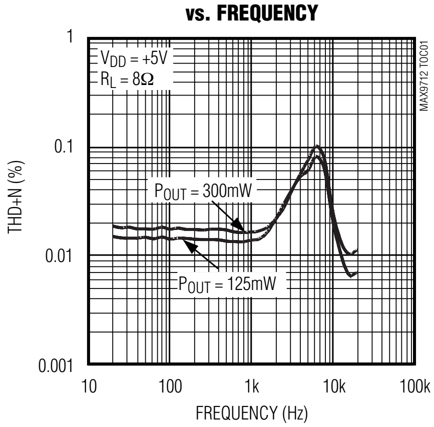
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	SNR	V_{OUT} = 1.8V_{RMS}	BW = 22Hz to 22kHz	FFM		88		dB
				SSM		86		
			A-weighted	FFM		91		
				SSM		89		
Oscillator Frequency	f_{OSC}	SYNC = GND			980	1100	1220	kHz
		SYNC = float			1280	1450	1620	
		SYNC = V_{DD} (SSM mode)				1220 ±120		
SYNC Frequency Lock Range					800		2000	kHz
Efficiency	η	P_{OUT} = 300mW, f_{IN} = 1kHz				85		%
DIGITAL INPUTS ($\overline{SHDN}$, SYNC)								
Input Thresholds		V_{IH}			2			V
		V_{IL}					0.8	
$\overline{SHDN}$ Input Leakage Current							±1	µA
SYNC Input Current							±5	µA

Note 1: All devices are 100% production tested at +25°C. All temperature limits are guaranteed by design.
Note 2: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 6Ω, L = 47µH. For R_L = 8Ω, L = 68µH. For R_L = 16Ω, L = 136µH.
Note 3: PSRR is specified with the amplifier inputs connected to GND through C_{IN}.

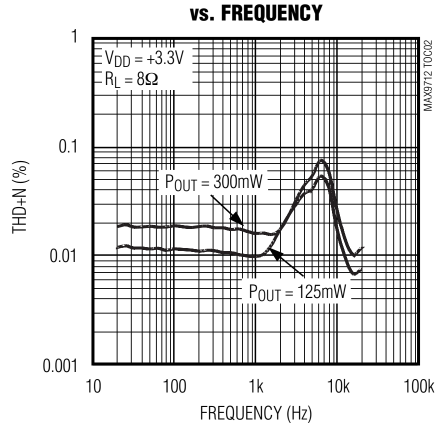
Typical Operating Characteristics

(V_{DD} = 3.3V, V_{SYNC} = GND, T_A = +25°C, unless otherwise noted.)

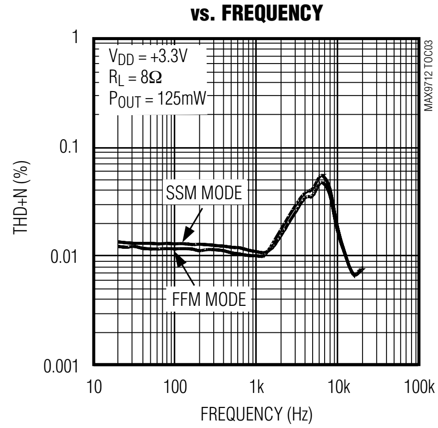
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

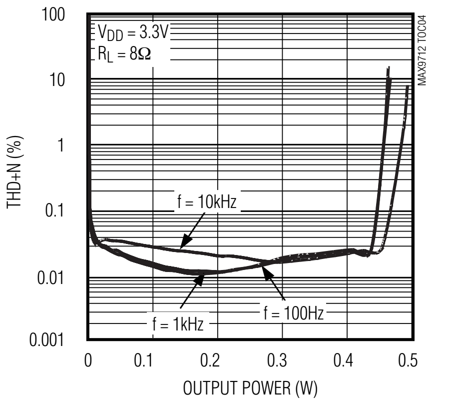


500mW, Low EMI, Filterless, Class D Audio Amplifier

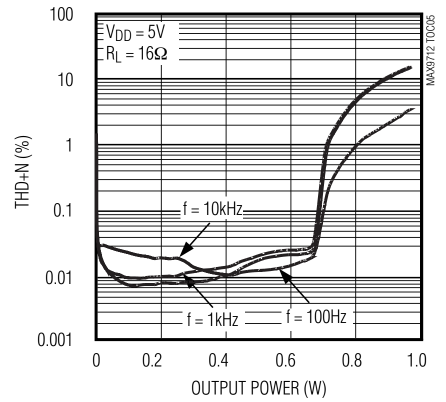
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SYNC} = GND, T_A = +25°C, unless otherwise noted.)

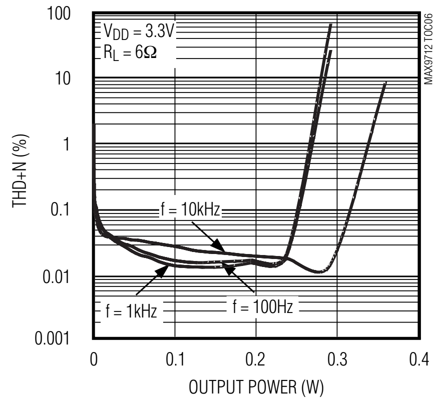
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



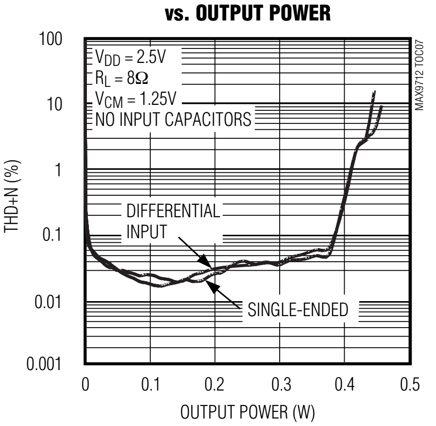
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



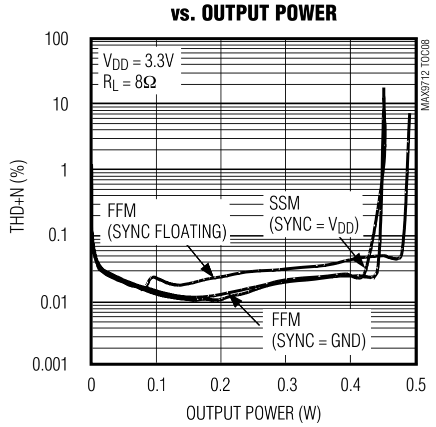
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



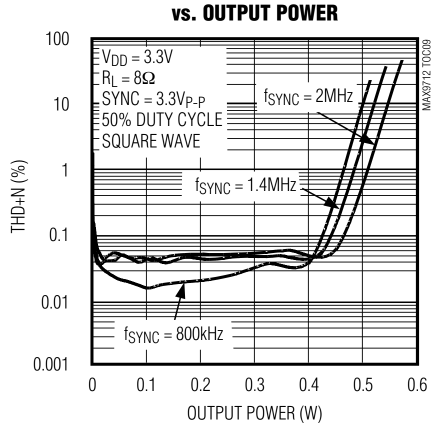
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



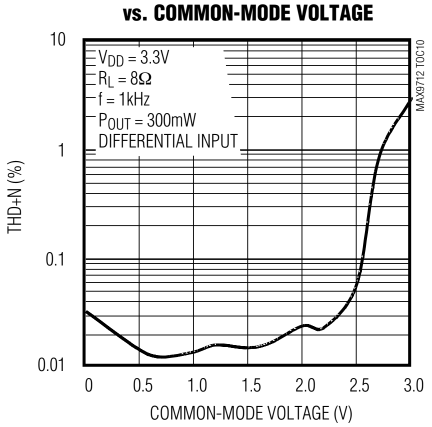
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



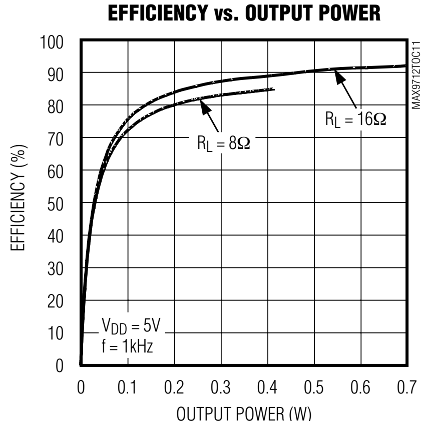
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



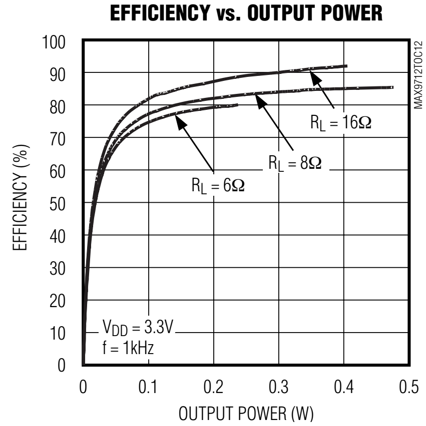
TOTAL HARMONIC DISTORTION PLUS NOISE vs. COMMON-MODE VOLTAGE



EFFICIENCY vs. OUTPUT POWER



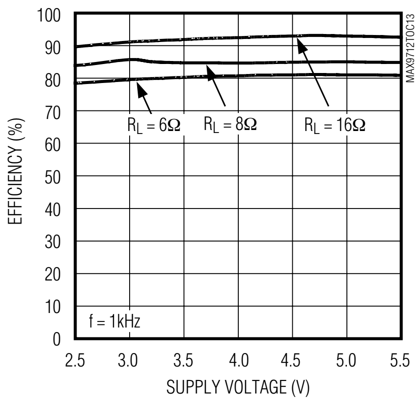
EFFICIENCY vs. OUTPUT POWER



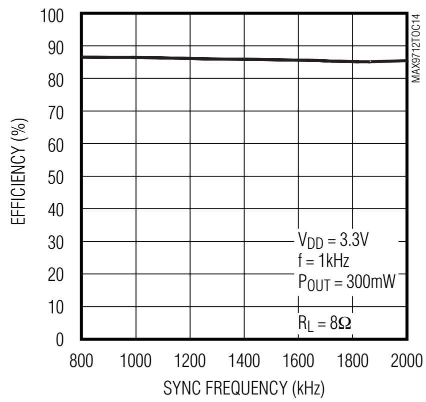
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SYNC} = GND, T_A = +25°C, unless otherwise noted.)

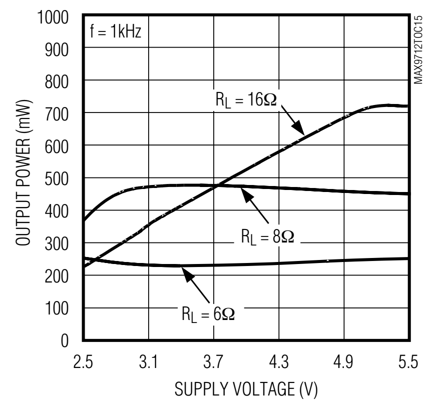
EFFICIENCY vs. SUPPLY VOLTAGE



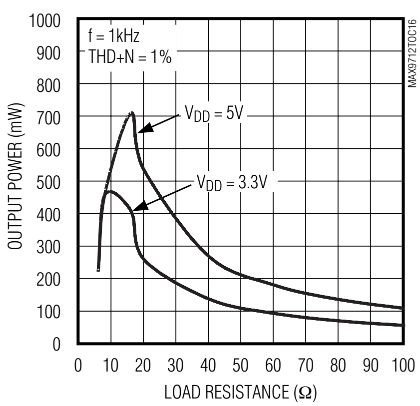
EFFICIENCY vs. SYNC INPUT FREQUENCY



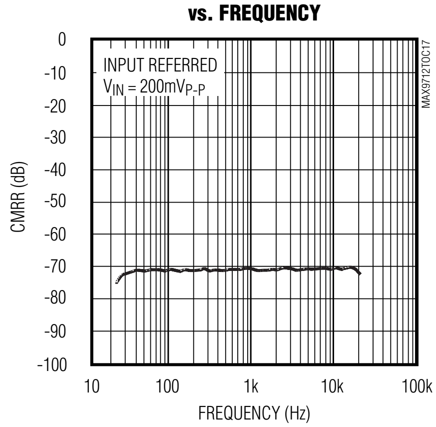
OUTPUT POWER vs. SUPPLY VOLTAGE



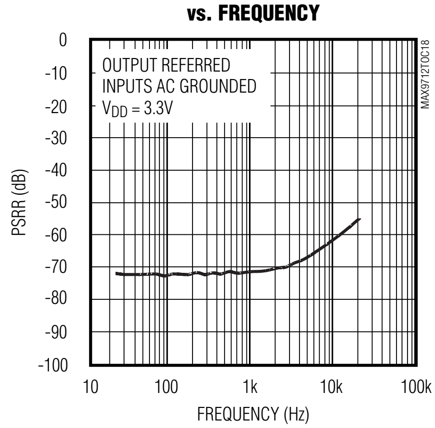
OUTPUT POWER vs. LOAD RESISTANCE



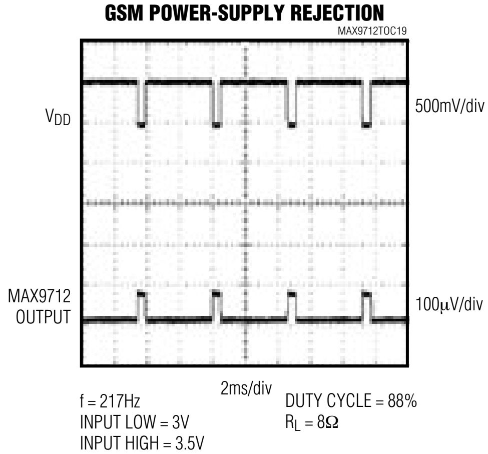
COMMON-MODE REJECTION RATIO vs. FREQUENCY



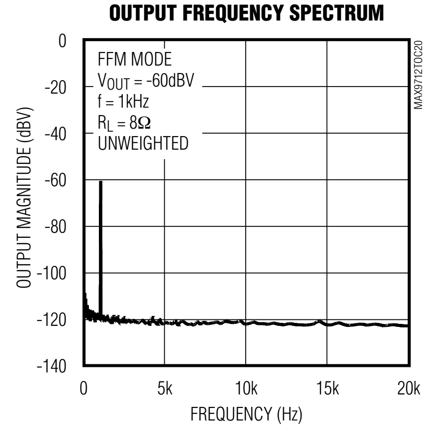
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



GSM POWER-SUPPLY REJECTION



OUTPUT FREQUENCY SPECTRUM

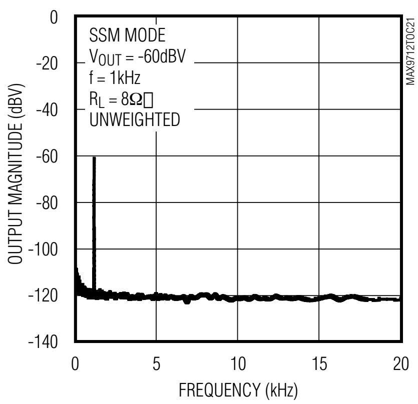


500mW, Low EMI, Filterless, Class D Audio Amplifier

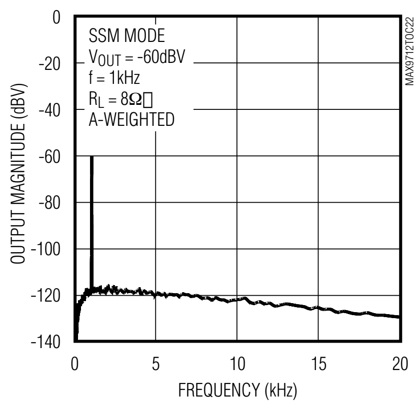
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SYNC} = GND, T_A = +25°C, unless otherwise noted.)

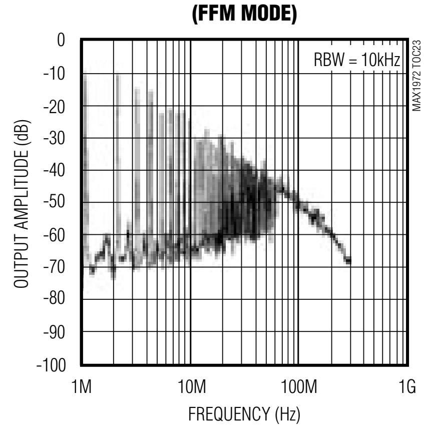
OUTPUT FREQUENCY SPECTRUM



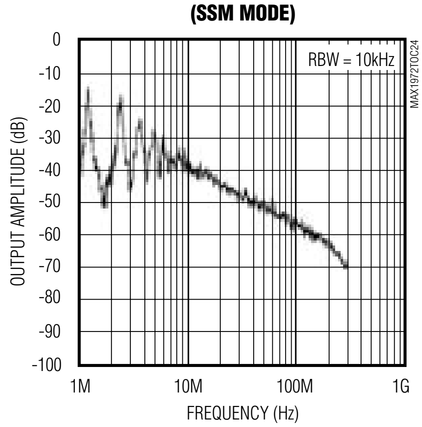
OUTPUT FREQUENCY SPECTRUM



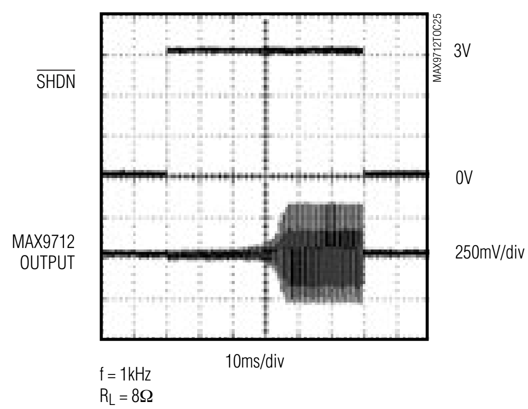
WIDEBAND OUTPUT SPECTRUM (FFM MODE)



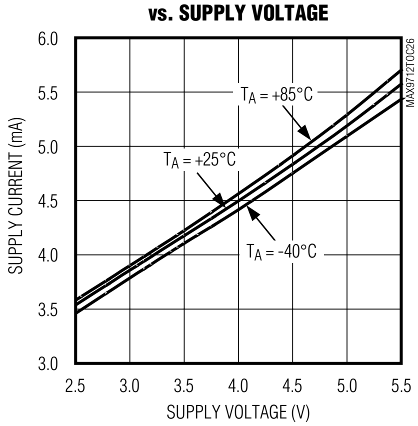
WIDEBAND OUTPUT SPECTRUM (SSM MODE)



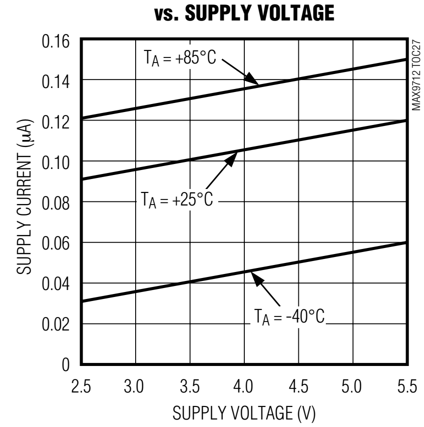
TURN-ON/TURN-OFF RESPONSE



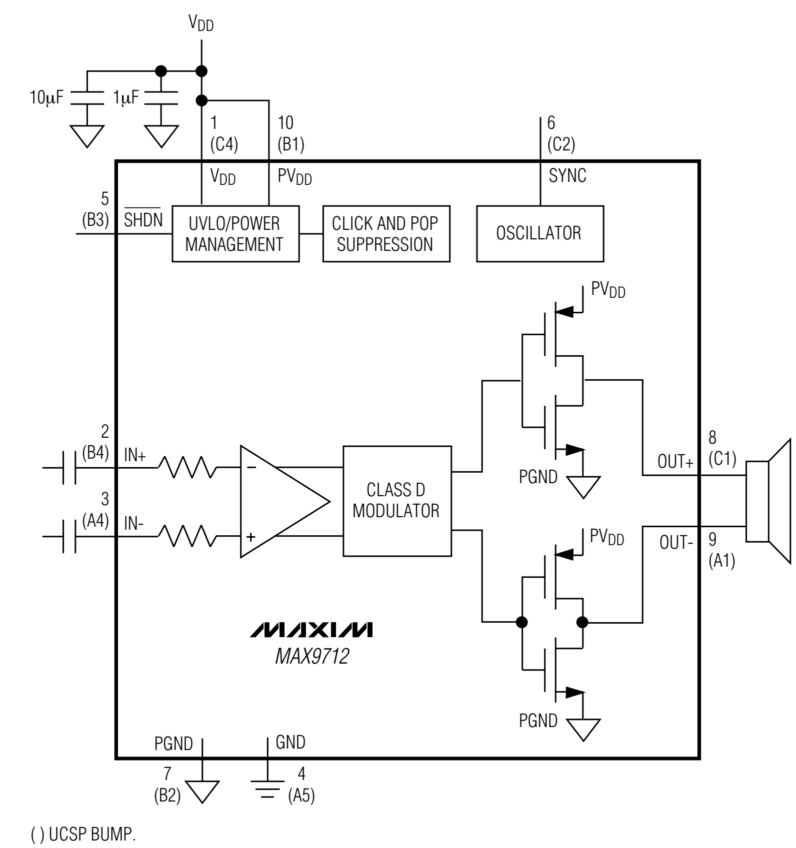
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



Functional Diagram



Pin Description

PIN TDFN/µMAX	BUMP UCSP	NAME	FUNCTION
1	C4	V_{DD}	Analog Power Supply
2	B4	IN+	Noninverting Audio Input
3	A4	IN-	Inverting Audio Input
4	A3	GND	Analog Ground
5	B3	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to V_{DD} for normal operation.
6	C2	SYNC	Frequency Select and External Clock Input. **SYNC = GND:** Fixed-frequency mode with f_S = 1100kHz. **SYNC = Float:** Fixed-frequency mode with f_S = 1450kHz. **SYNC = V_{DD}:** Spread-spectrum mode with f_S = 1220kHz ±120kHz. **SYNC = Clocked:** Fixed-frequency mode with f_S = external clock frequency.
7	B2	PGND	Power Ground
8	C1	OUT+	Amplifier Output Positive Phase
9	A1	OUT-	Amplifier Output Negative Phase
10	B1	PV_{DD}	H-Bridge Power Supply

Detailed Description

The MAX9712 filterless, class D audio power amplifier features several improvements to switch-mode amplifier technology. The MAX9712 offers class AB performance with class D efficiency, while occupying minimal board space. A unique filterless modulation scheme, synchronizable switching frequency, and SSM mode create a compact, flexible, low-noise, efficient audio power amplifier. The differential input architecture reduces common-mode noise pick-up, and can be used without input-coupling capacitors. The device can also be configured as a single-ended input amplifier.

Comparators monitor the MAX9712 inputs and compare the complementary input voltages to the sawtooth waveform. The comparators trip when the input magnitude of the sawtooth exceeds their corresponding input voltage. Both comparators reset at a fixed time after the rising edge of the second comparator trip point, generating a minimum-width pulse $t_{ON(min)}$ at the output of the second comparator (Figure 1). As the input voltage increases or decreases, the duration of the pulse at one output increases (the first comparator to trip) while the other output pulse duration remains at $t_{ON(min)}$. This causes the net voltage across the speaker (V_{OUT+} - V_{OUT-}) to change.

Operating Modes

Fixed-Frequency Modulation (FFM) Mode

The MAX9712 features two FFM modes. The FFM modes are selected by setting SYNC = GND for a 1.1MHz switching frequency, and SYNC = FLOAT for a 1.45MHz switching frequency. In FFM mode, the frequency spectrum of the class D output consists of the fundamental switching frequency and its associated harmonics (see the Wideband FFT graph in the *Typical Operating Characteristics*). The MAX9712 allows the switching frequency to be changed by +32%, should the frequency of one or more of the harmonics fall in a sensitive band. This can be done at any time and does not affect audio reproduction.

Spread-Spectrum Modulation (SSM) Mode

The MAX9712 features a unique spread-spectrum mode that flattens the wideband spectral components, improving EMI emissions that may be radiated by the speaker and cables by 5dB. Proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency (see the *Typical Operating Characteristics*). Select SSM mode by setting SYNC = V_{DD}. In SSM mode, the switching frequency varies randomly by ±120kHz around the center frequency (1.22MHz). The modulation scheme remains the same, but the period of the sawtooth waveform changes from cycle to cycle (Figure 2). Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over

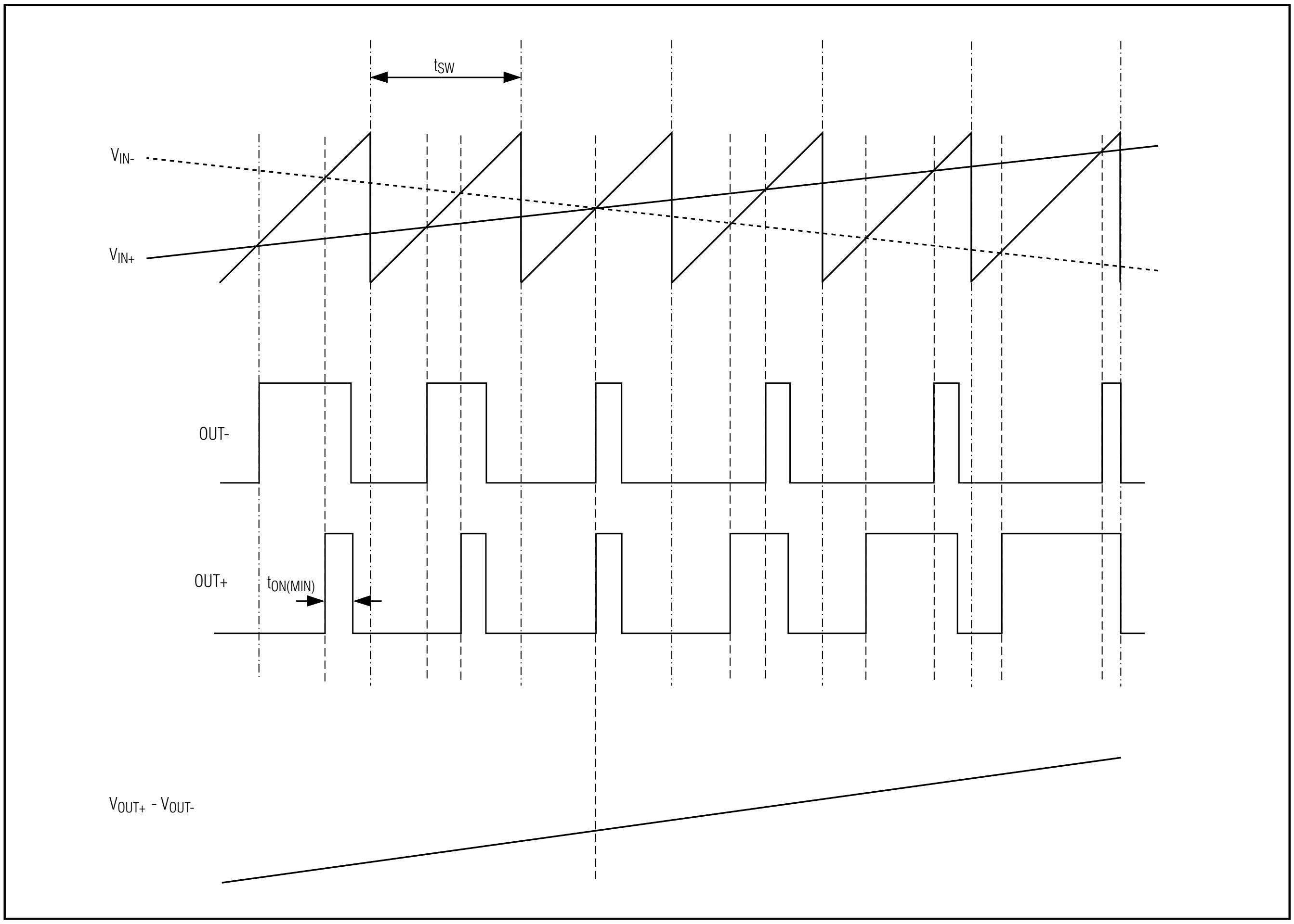


Figure 1. MAX9712 Outputs with an Input Signal Applied

Table 1. Operating Modes

SYNC INPUT	MODE
GND	FFM with f_S = 1100kHz
FLOAT	FFM with f_S = 1450kHz
V_{DD}	SSM with f_S = 1220kHz ±120kHz
Clocked	FFM with f_S = external clock frequency

a bandwidth that increases with frequency. Above a few MHz, the wideband spectrum looks like white noise for EMI purposes (Figure 3).

External Clock Mode

The SYNC input allows the MAX9712 to be synchronized to a system clock (allowing a fully synchronous system), or allocating the spectral components of the switching harmonics to insensitive frequency bands. Applying an external TTL clock of 800kHz to 2MHz to SYNC synchronizes the switching frequency of the MAX9712. The period of the SYNC clock can be randomized, enabling the MAX9712 to be synchronized to another MAX9712 operating in SSM mode.

Filterless Modulation/Common-Mode Idle

The MAX9712 uses Maxim's unique modulation scheme that eliminates the LC filter required by traditional class D amplifiers, improving efficiency, reducing component count, conserving board space and system cost. Conventional class D amplifiers output a 50% duty cycle square wave when no signal is present. With no filter, the square wave appears across

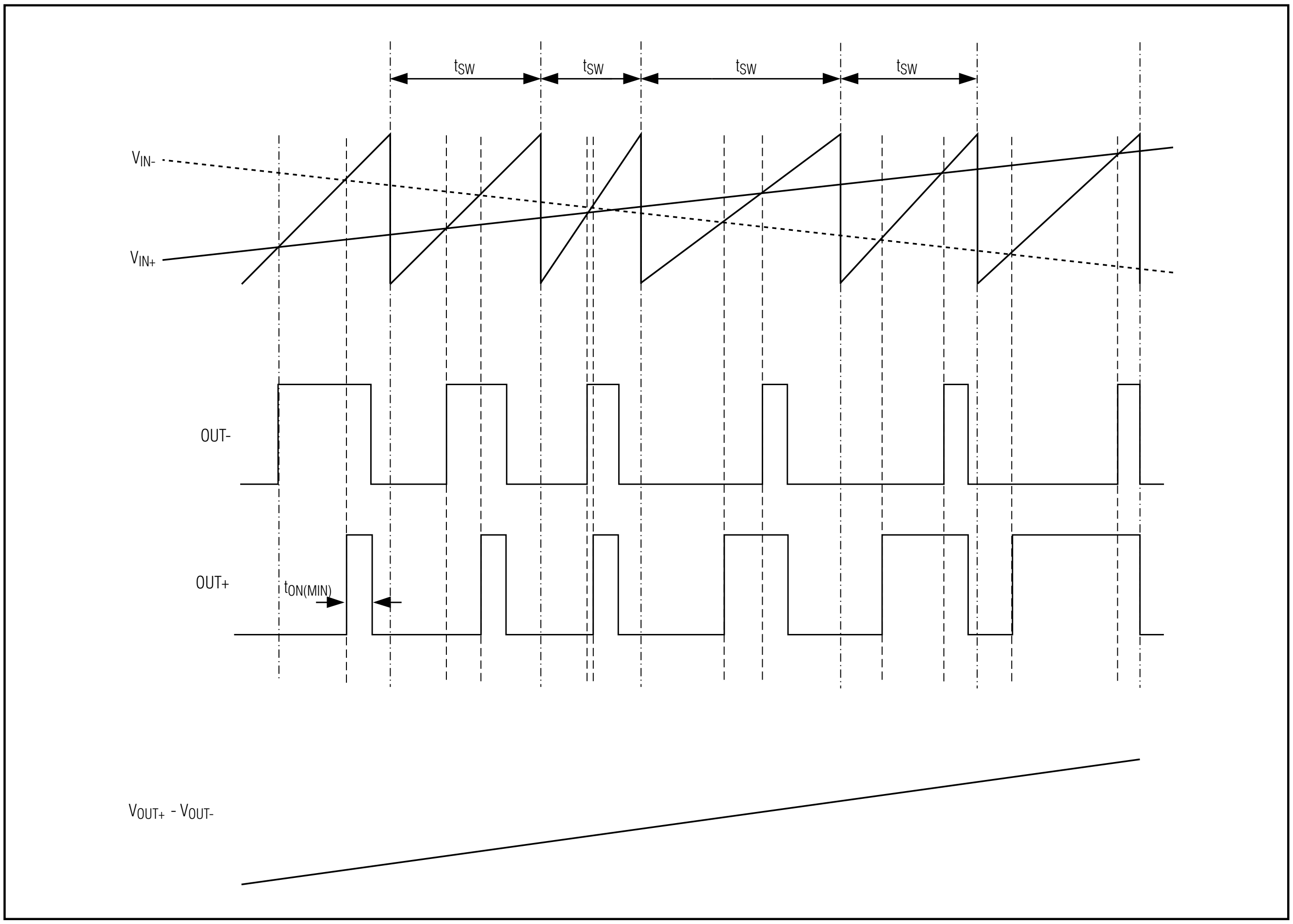


Figure 2. MAX9712 Output with an Input Signal Applied (SSM Mode)

the load as a DC voltage, resulting in finite load current, increasing power consumption. When no signal is present at the input of the MAX9712, the outputs switch as shown in Figure 4. Because the MAX9712 drives the speaker differentially, the two outputs cancel each other, resulting in no net idle mode voltage across the speaker, minimizing power consumption.

Efficiency

Efficiency of a class D amplifier is attributed to the region of operation of the output stage transistors. In a class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the class D output stage is mostly due to the I × R loss of the MOSFET on-resistance, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78%, however, that efficiency is only exhibited at peak output powers. Under normal operating levels (typical music reproduction levels), efficiency falls below 30%, whereas the MAX9712 still exhibits >80% efficiencies under the same conditions (Figure 5).

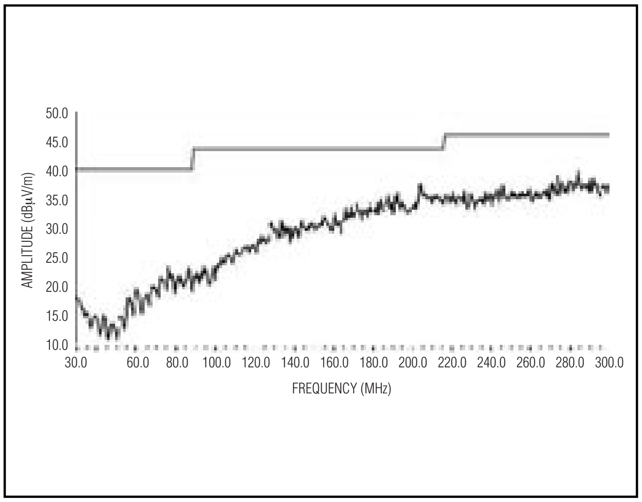


Figure 3. MAX9712 with 76mm of Speaker Cable

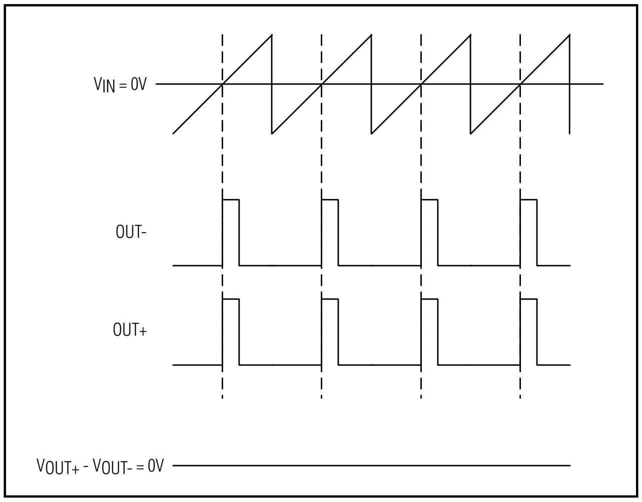


Figure 4. MAX9712 Outputs with No Input Signal

Shutdown

The MAX9712 has a shutdown mode that reduces power consumption and extends battery life. Driving $\overline{SHDN}$ low places the MAX9712 in a low-power (0.1µA) shutdown mode. Connect $\overline{SHDN}$ to V_{DD} for normal operation.

Click-and-Pop Suppression

The MAX9712 features comprehensive click-and-pop suppression that eliminates audible transients on startup and shutdown. While in shutdown, the H-bridge is in a high-impedance state. During startup, or power-up, the input amplifiers are muted and an internal loop sets the modulator bias voltages to the correct levels, preventing clicks and pops when the H-bridge is subsequently enabled. For 35ms following startup, a soft-start function gradually unmutes the input amplifiers.

Applications Information

Filterless Operation

Traditional class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency. The traditional PWM scheme uses large differential output swings (2 x V_{DD} peak-to-peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

The MAX9712 does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, less costly, more efficient solution.

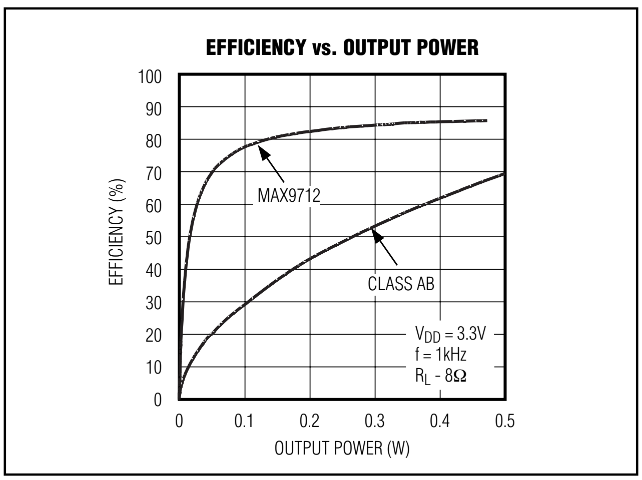


Figure 5. MAX9712 Efficiency vs. Class AB Efficiency

Because the frequency of the MAX9712 output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. Although this movement is small, a speaker not designed to handle the additional power may be damaged. For optimum results, use a speaker with a series inductance >10µH. Typical 8Ω speakers exhibit series inductances in the range of 20µH to 100µH.

Power Conversion Efficiency

Unlike a class AB amplifier, the output offset voltage of a class D amplifier does not noticeably increase quiescent current draw when a load is applied. This is due to the power conversion of the class D amplifier. For example, an 8mV DC offset across an 8Ω load results in 1mA extra current consumption in a class AB device. In the class D case, an 8mV offset into 8Ω equates to an additional power drain of 8μW. Due to the high efficiency of the class D amplifier, this represents an additional quiescent current draw of: $8\mu W/(V_{DD}/100\eta)$, which is on the order of a few microamps.

Input Amplifier

Differential Input

The MAX9712 features a differential input structure, making it compatible with many CODECs, and offering improved noise immunity over a single-ended input amplifier. In devices such as cellular phones, high-frequency signals from the RF transmitter can be picked up by the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs, any signal common to both inputs is canceled.

Single-Ended Input

The MAX9712 can be configured as a single-ended input amplifier by capacitively coupling either input to GND, and driving the other input (Figure 6).

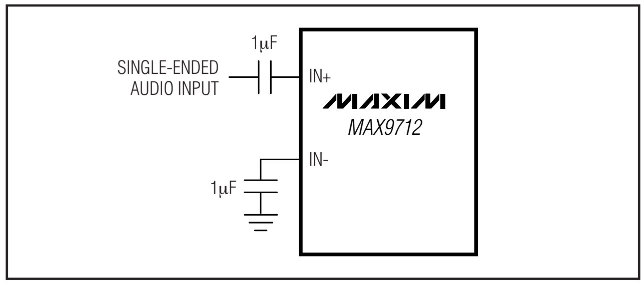


Figure 6. Single-Ended Input

DC-Coupled Input

The input amplifier can accept DC-coupled inputs that are biased within the amplifier's common-mode range (see the *Typical Operating Characteristics*). DC coupling eliminates the input-coupling capacitors, reducing component count to potentially one external component (see the *System Diagram*). However, the low-frequency rejection of the capacitors is lost, allowing low-frequency signals to feedthrough to the load.

Component Selection

Input Filter

An input capacitor, C_{IN}, in conjunction with the input impedance of the MAX9712 forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Choose C_{IN} so f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the low-frequency response of the amplifier. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, may result in increased distortion at low frequencies.

Other considerations when designing the input filter include the constraints of the overall system and the actual frequency band of interest. Although high-fidelity audio calls for a flat-gain response between 20Hz and 20kHz, portable voice-reproduction devices such as cellular phones and two-way radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 150Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

Output Filter

The MAX9712 does not require an output filter. The device passes FCC emissions standards with 100mm of unshielded speaker cables. However, output filtering can be used if a design is failing radiated emissions due to board layout or cable length, or the circuit is near EMI sensitive devices. Use an LC filter when radiated emissions are a concern, or when long leads are used to connect the amplifier to the speaker.

Supply Bypassing/Layout

Proper power-supply bypassing ensures low distortion operation. For optimum performance, bypass VDD to GND and PVDD to PGND with separate 0.1μF capacitors as close to each pin as possible. A low-impedance, high-current power-supply connection to PVDD is assumed. Additional bulk capacitance should be added as required depending on the application and power-supply characteristics. GND and PGND should be star connected to system ground. Refer to the MAX9712 Evaluation Kit for layout guidance.

Stereo Configuration

Two MAX9712s can be configured as a stereo amplifier (Figure 7). Device U1 is the master amplifier; its unfil-

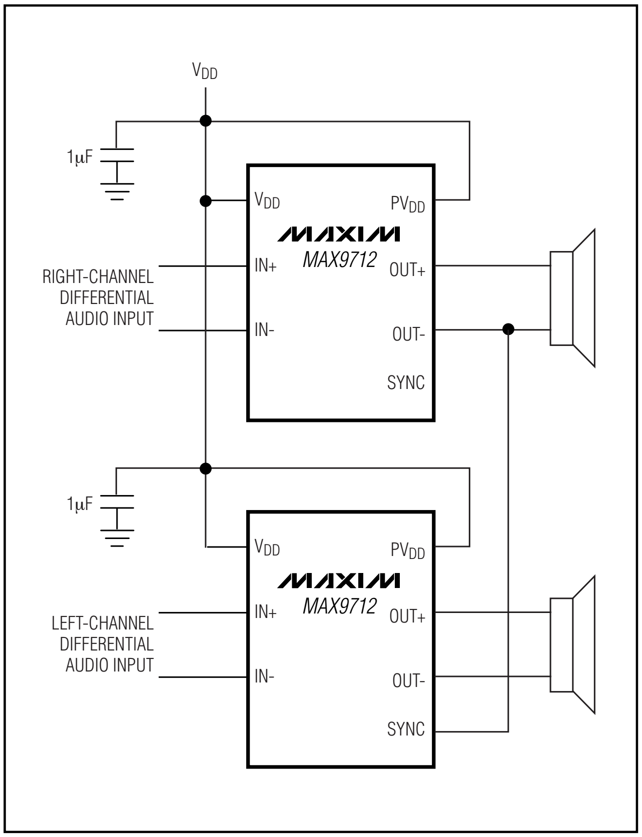


Figure 7. Master-Slave Stereo Configuration

tered output drives the SYNC input of the slave device (U2), synchronizing the switching frequencies of the two devices. Synchronizing two MAX9712s ensures that no beat frequencies occur within the audio spectrum. This configuration works when the master device is in either FFM or SSM mode. There is excellent THD+N performance and minimal crosstalk between devices due to the SYNC connection (Figures 8 and 9). U2 locks onto only the frequency present at SYNC, not the pulse width. The internal feedback loop of device U2 ensures that the audio component of U1's output is rejected.

UCSP Applications Information

For the latest application details on UCSP construction, dimensions, tape carrier information, printed circuit board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note: *UCSP—A Wafer-Level Chip-Scale Package* available on Maxim's website at www.maxim-ic.com/ucsp.

Chip Information

TRANSISTOR COUNT: 3595

PROCESS: BiCMOS

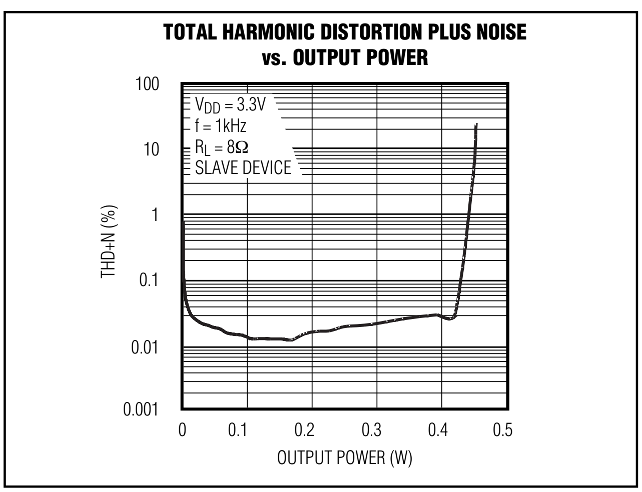


Figure 8. Master-Slave THD

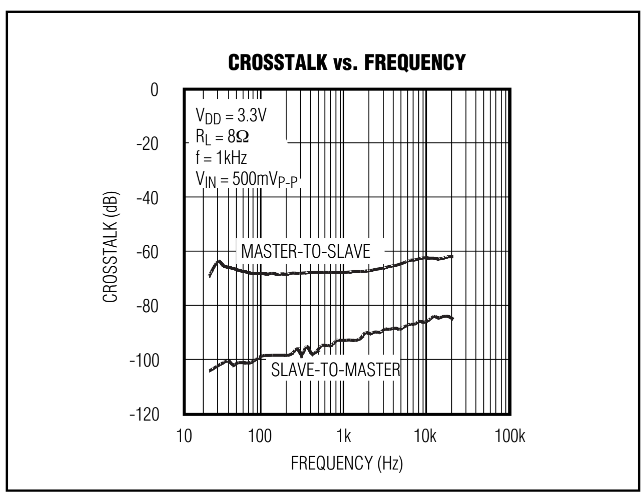
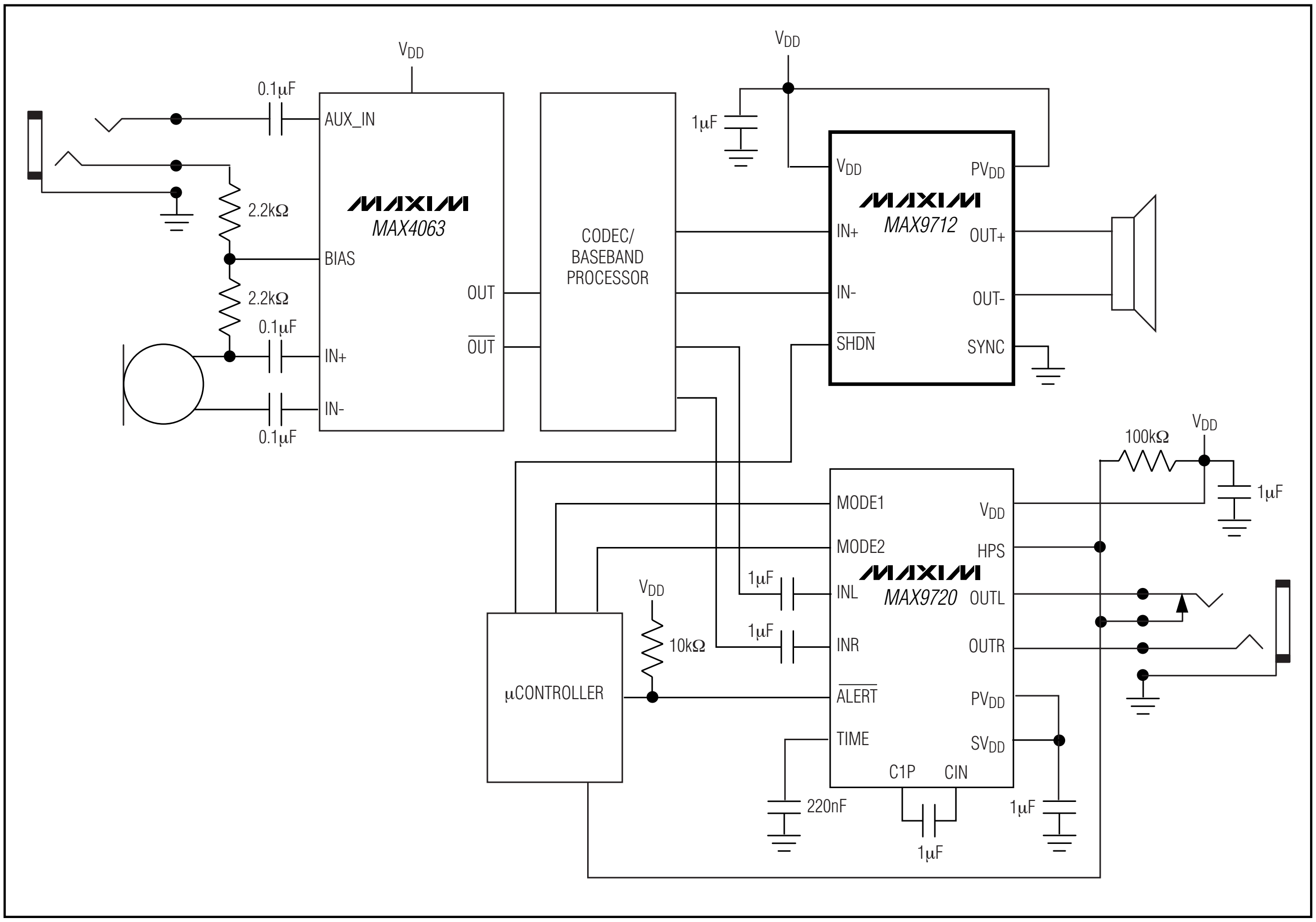
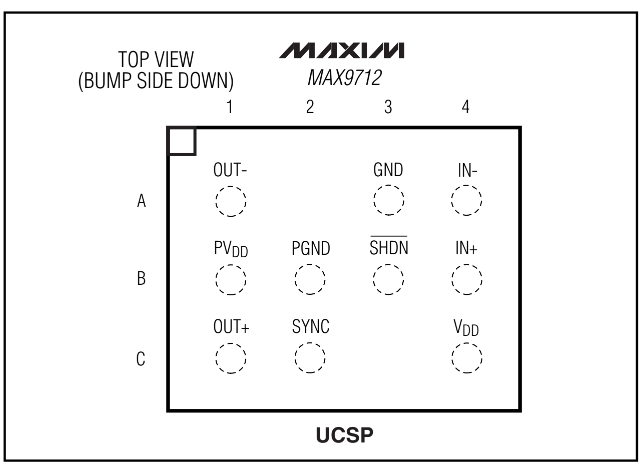


Figure 9. Master-Slave Crosstalk

System Diagram



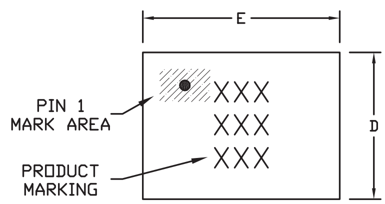
Pin Configurations (continued)



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

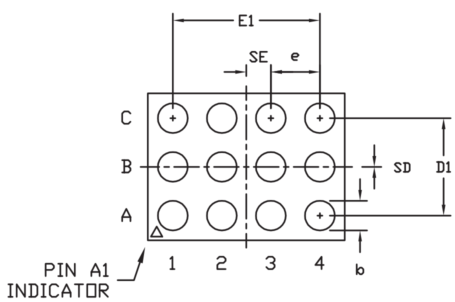
12L, UCSP 4x3.EPS



TOP VIEW

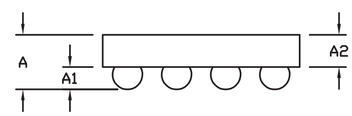
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

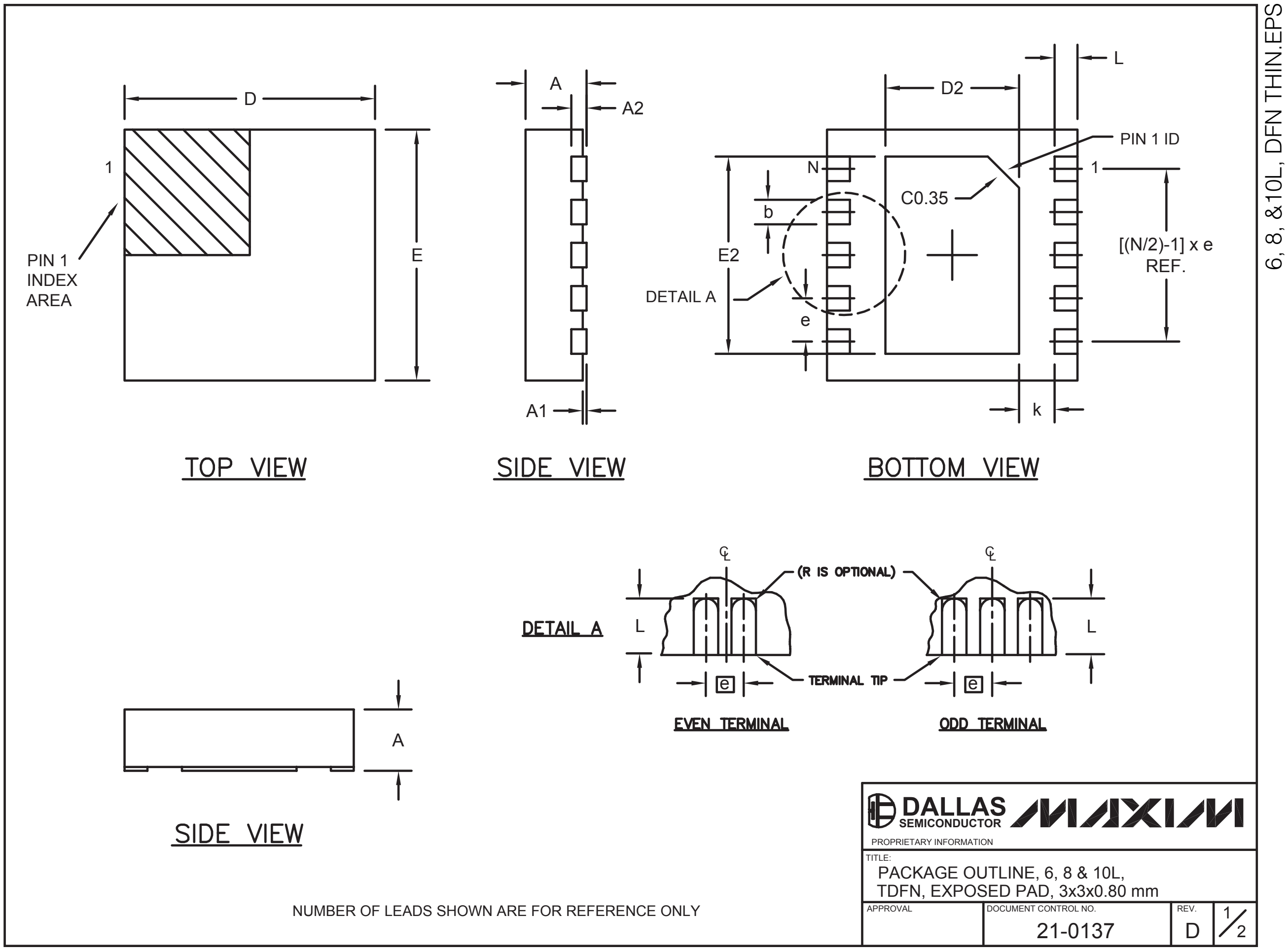
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM

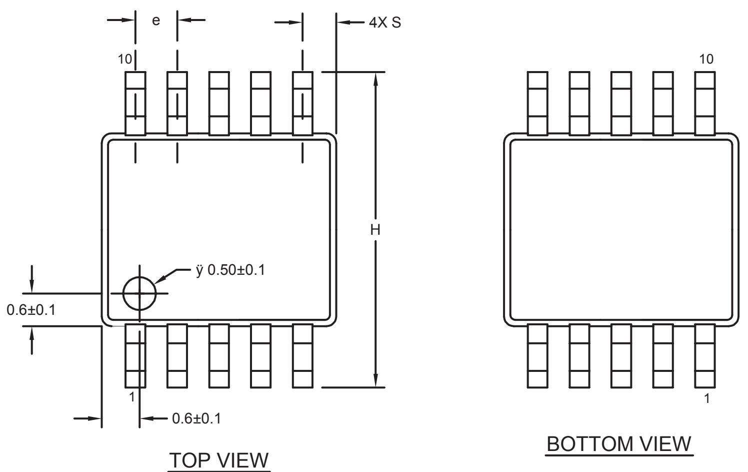
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 6, 8 & 10L, TDFN, EXPOSED PAD, 3x3x0.80 mm

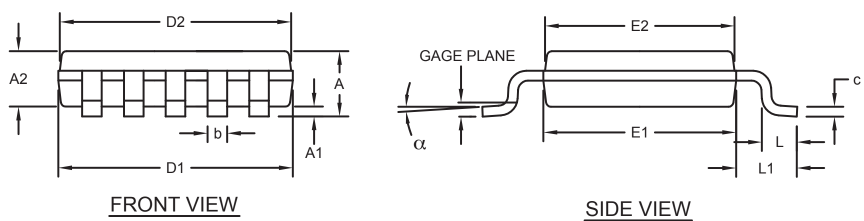
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	D	2/2

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



10LUMAX.EPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.