19-2338; Rev 4; 11/05

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

General Description

The MAX4366/MAX4367/MAX4368 are bridged audio power amplifiers intended for devices with internal speakers and headsets. The MAX4366/MAX4367/MAX4368 are capable of delivering 330mW of continuous power into a 32Ω load, or 200mW into a 16Ω load with 1% THD+N from a single 5V supply.

The MAX4366/MAX4367/MAX4368 bridged outputs eliminate the need for output-coupling capacitors minimizing external component count. The MAX4366/MAX4367/MAX4368 also feature a low-power shutdown mode, clickless power-up/power-down and internal DC bias generation. The MAX4366 is a unity-gain stable, programmable gain amplifier. The MAX4367/MAX4368 feature internally preset gains of 2V/V and 3V/V, respectively.

All devices are available in space-saving 8-pin SOT23, TDFN, and µMAX® packages, and an 8-bump chip-scale package (UCSP™).

Applications

Cellular Phones
Two-Way Radios
PDAs
Headphones
Headsets
General-Purpose Audio

Features

- **Drives 330mW into 32Ω (200mW into 16Ω)**
- **0.02% THD+N at 1kHz (120mW into 32Ω)**
- **Internal Bridged Configuration**
- **No Output-Coupling Capacitors**
- **2.3V to 5.5V Single-Supply Operation**
- **2mA Supply Current**
- **Low-Power Shutdown Mode**
- **Clickless Power-Up and Shutdown**
- **Thermal Overload Protection**
- **Available in SOT23, TDFN, µMAX, and UCSP Packages**

Ordering Information

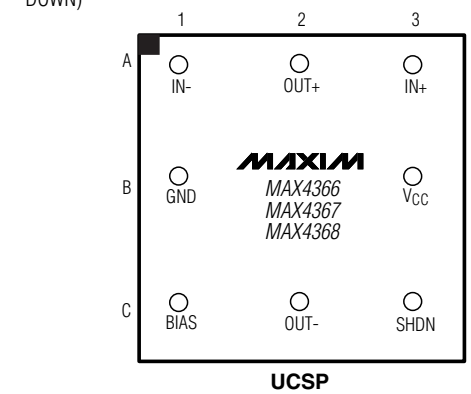
PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4366EBL-T	-40°C to +85°C	8 UCSP-8	AAK
MAX4366EKA-T	-40°C to +85°C	8 SOT23-8	AAIO
MAX4366EUA	-40°C to +85°C	8 µMAX	—
MAX4366ETA-T	-40°C to +85°C	8 TDFN-8-EP*	AFZ
MAX4366ETA+T	-40°C to +85°C	8 TDFN-8-EP*	+AFZ

*EP = Exposed paddle.
+Denotes lead-free package.

Ordering Information continued at end of data sheet.

Selector Guide and Functional Diagrams appear at end of data sheet.

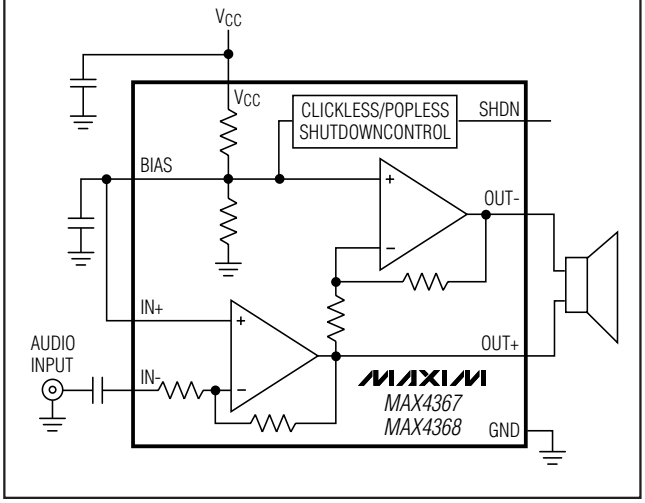
Pin Configurations



UCSP

Pin Configurations continued at end of data sheet.

Typical Operating Circuit



UCSP is a trademark and µMAX is a registered trademark of Maxim Integrated Products, Inc.

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
IN+, IN-, BIAS, SHDN to GND .....-0.3V to (V_{CC} + 0.3V)
Output Short Circuit to V_{CC} or GND (Note 1).....Continuous
Output Short Circuit (OUT+ to OUT-) (Note 1).....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Bump UCSP (derate 4.7mW/°C above +70°C).....379mW
8-Pin SOT23 (derate 9.7mW/°C above +70°C).....777mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) 362mW
8-Pin TDFN (derate 24.4mW°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Bump Temperature (soldering) (Note 2)
Infrared (15s) .....+220°C
Vapor Phase (60s) .....+215°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, R_L = ∞, R_{IN} = R_F = 30kΩ, C_{BIAS} = 1µF to GND, SHDN = GND, IN+ = BIAS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}	Inferred from PSRR test		2.3		5.5	V
Supply Current	I_{CC}	(Note 4)			2	4.3	mA
Shutdown Supply Current	I_{SHDN}	SHDN = V_{CC}			35	100	µA
SHDN Threshold	V_{IH}			1.8			V
	V_{IL}					0.8	
SHDN Input Bias Current					-400		nA
Common-Mode Bias Voltage	V_{BIAS}	(Note 5)		V_{CC}/2 - 5%	V_{CC}/2	V_{CC}/2 + 5%	V
Output Offset Voltage	V_{OS}	MAX4366, R_{IN} = ∞			±5	±15	mV
		MAX4367, IN- = open			±5	±15	
		MAX4368, IN- = open		±5	±7.5	±15	
Differential Voltage Gain	A_V	(Note 6)	MAX4366 (open loop)		100		dB
			MAX4367 (internally set)		2		V/V
			MAX4368 (internally set)		3		
Input Common-Mode Range	V_{CM}			0.3		V_{CC} - 1.0	V
Differential Input Resistance	$R_{IN(DIFF)}$	MAX4366, V_{IN+} - V_{IN-} = 10mV			500		kΩ
Input Resistance		V_{IN-} = 0V to V_{CC} (MAX4367/MAX4368)			20		kΩ
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.3V to 5.5V	T_A = +25°C	70	80		dB
			T_A = T_{MIN} to T_{MAX}	66			
Common-Mode Rejection Ratio	CMRR	0V ≤ V_{CM} ≤ V_{CC} - 1.0V (MAX4366)			80		dB
Output Source/Sink Current	I_{OUT}	(Note 7)	2.7V ≤ V_{CC} ≤ 5.5V, 0.6V ≤ V_{OUT} ≤ V_{CC} - 0.6V	±87	±125		mA
			2.3V ≤ V_{CC} ≤ 2.7V, 0.6V ≤ V_{OUT} ≤ V_{CC} - 0.6V		±115		
Output Power	P_O	f = 1kHz, THD+N <1% (Note 8)	R_L = 16Ω	60	200		mW
			R_L = 32Ω	120	330		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 5V, R_L = ∞, R_{IN} = R_F = 30kΩ, C_{BIAS} = 1µF to GND, SHDN = GND, IN+ = BIAS, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion Plus Noise	THD+N	A_V = -2V/V, f = 1kHz (MAX4366) (Notes 9 and 10)	P_O = 60mW, R_L = 16Ω		0.04		%
			P_O = 120mW, R_L = 32Ω		0.02	0.15	
Noise		f = 10kHz, referred to input			20		nV/√Hz
Short-Circuit Current	I_{SC}	To V_{CC}			185		mA
		To GND			215		
Thermal Shutdown Threshold					165		°C
Thermal Shutdown Hysteresis					10		°C
Power-Up Time	t_{PU}				60		ms
Shutdown Time	t_{SHDN}				20		ms
Enable Time from Shutdown	t_{ENABLE}				60		ms

Note 1: Continuous power dissipation must also be observed.

Note 2: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Note 3: All specifications are 100% tested at T_A = +25°C; temperature limits are guaranteed by design.

Note 4: Quiescent power-supply current is specified and tested with no load on the outputs. Quiescent power-supply current depends on the offset voltage when a practical load is connected to the amplifier.

Note 5: Common-mode bias voltage is the voltage on BIAS and is nominally V_{CC}/2.

Note 6: Differential voltage gain for the MAX4366 is specified as an open-loop parameter because external resistors are used to set the closed-loop gain. The MAX4367/MAX4368 contain internal feedback resistors that preset the differential voltage gain. Differential voltage gain is defined as (V_{OUT+} - V_{OUT-}) / (V_{IN} - V_{BIAS}). All gains are specified over an output voltage range of 0.6V ≤ V_{OUT} ≤ 4.4V.

Note 7: Specification applies to either output. An amplifier peak output current of 87mA is required to support an output load power of 60mW for a 16Ω load, or 120mW for a 32Ω load.

Note 8: Output power specifications are inferred from the output current test. For 60mW into a 16Ω load, $I_{OUT(PEAK)}$ is 87mA and $V_{OUT(P-P)}$ is 1.39V per amplifier. For 120mW into a 32Ω load, $I_{OUT(PEAK)}$ is 87mA and $V_{OUT(P-P)}$ is 2.77V per amplifier.

Note 9: Guaranteed by design. Not production tested.

Note 10: Measurement bandwidth for THD+N is 20Hz to 20kHz.

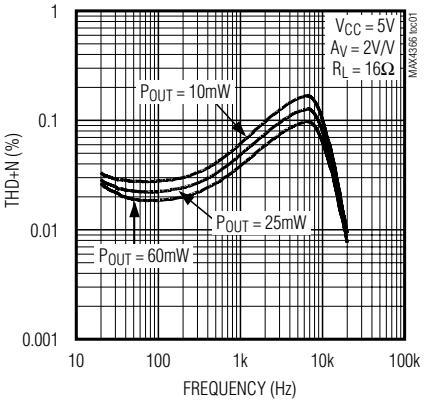
Note 11: Power-up and shutdown times are for the output to reach 90% of full scale with C_{BIAS} = 1µF.

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

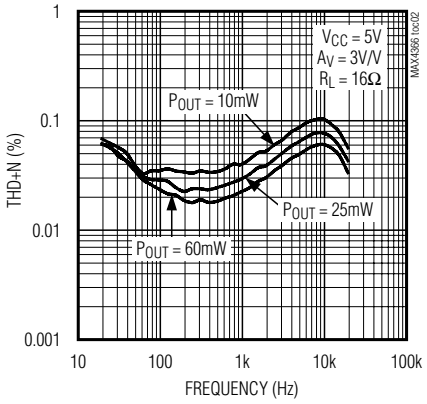
Typical Operating Characteristics

(Bridge-Tied Load, THD+N Bandwidth = 22Hz to 22kHz, C_{BIAS} = 1µF.)

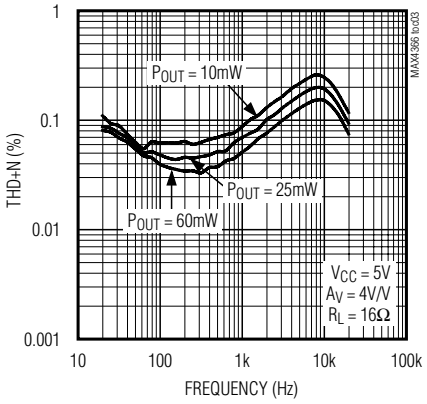
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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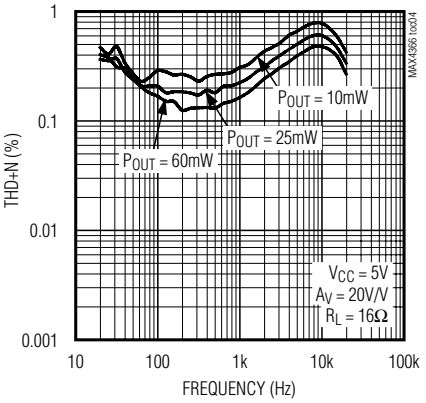

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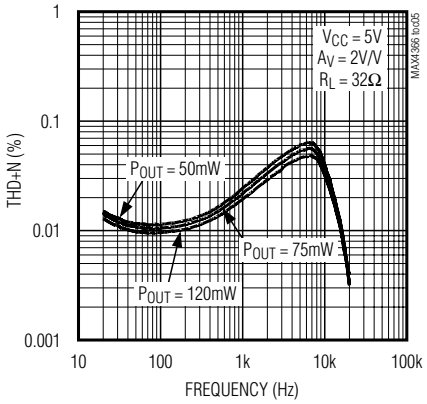

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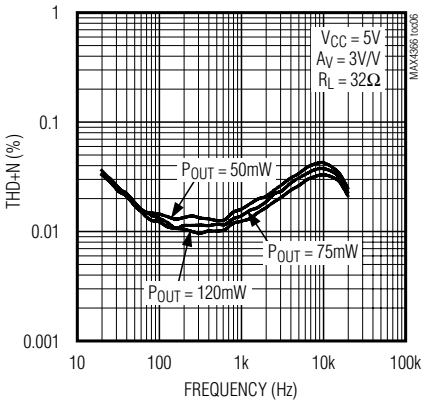

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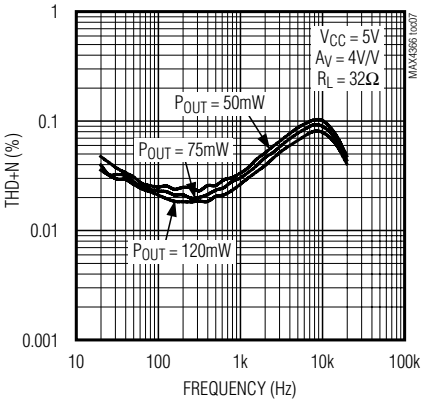

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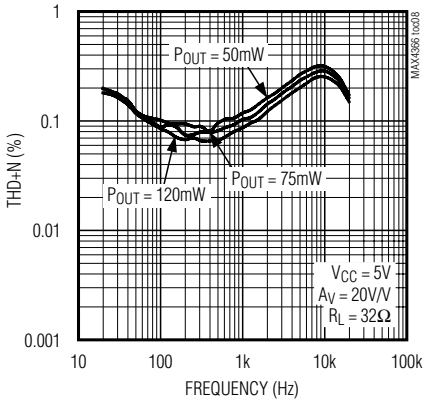

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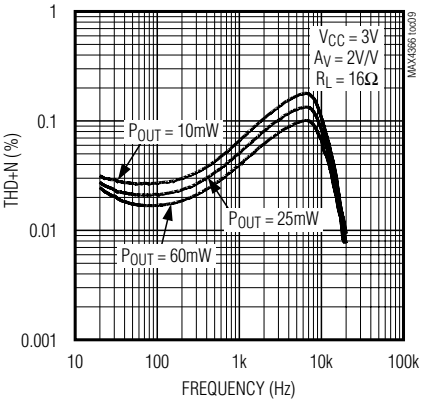
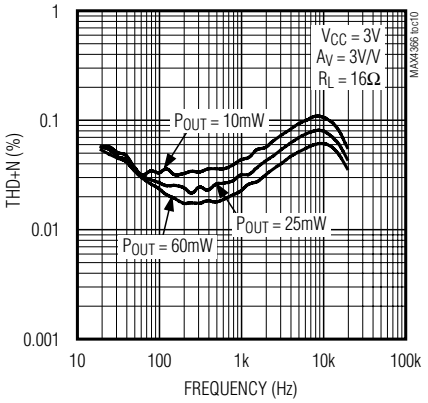


Typical Operating Characteristics (continued)

(Bridge-Tied Load, THD+N Bandwidth = 22Hz to 22kHz, C_{BIAS} = 1µF.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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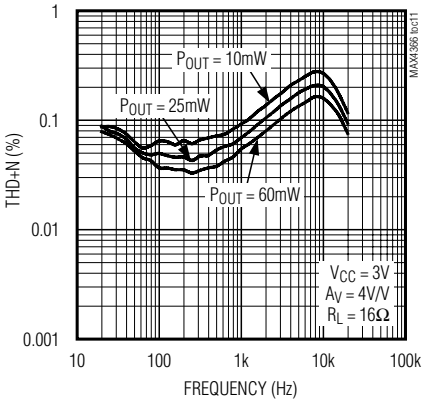

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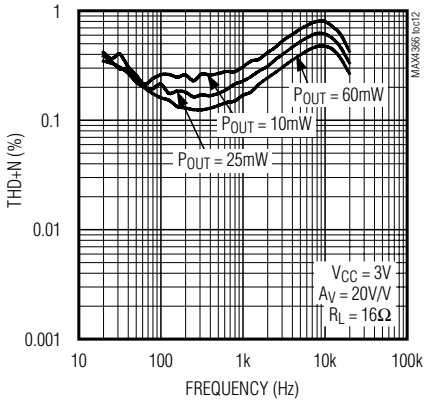

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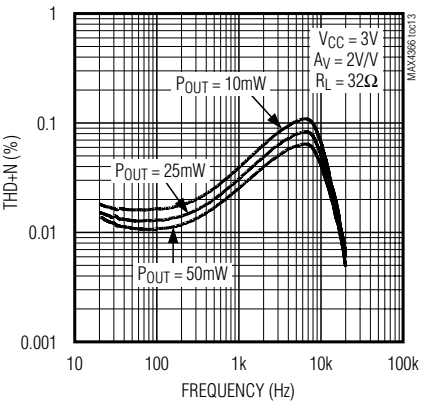

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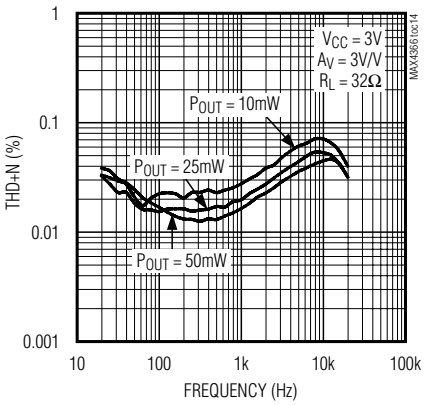

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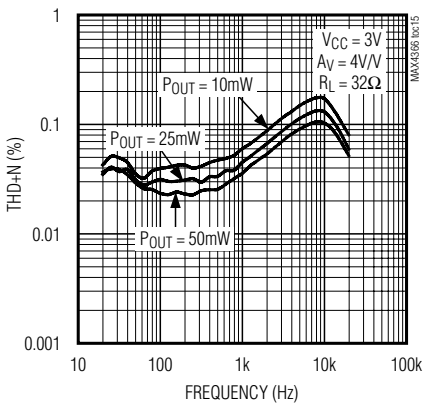

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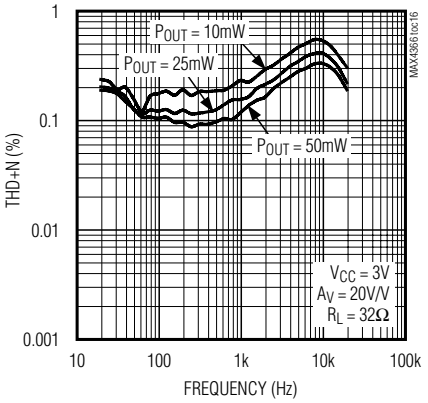
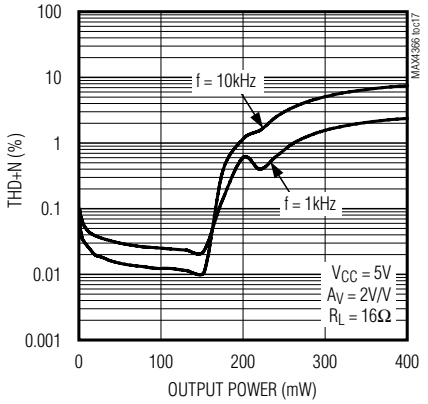
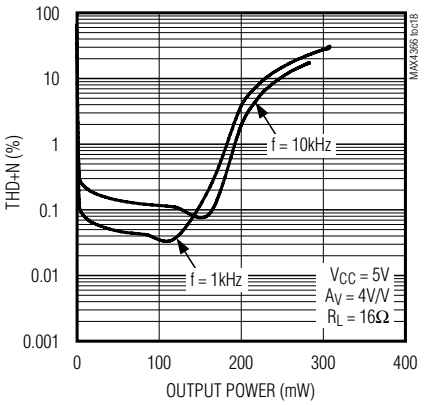


TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

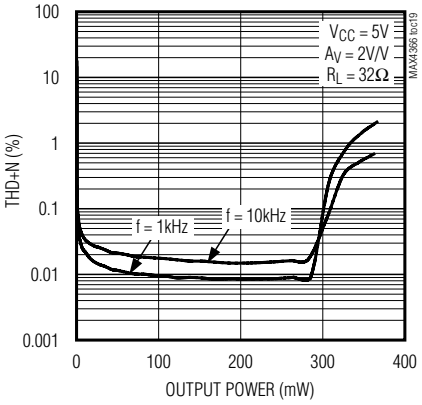


330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

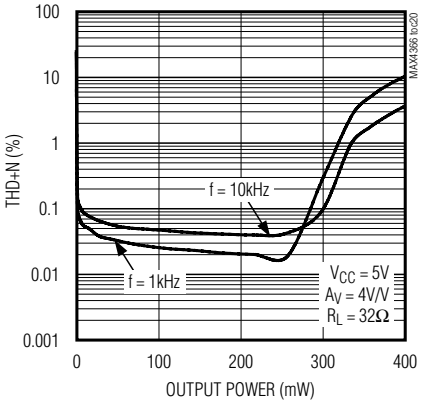
Typical Operating Characteristics (continued)

(Bridge-Tied Load, THD+N Bandwidth = 22Hz to 22kHz, C_{BIAS} = 1µF.)

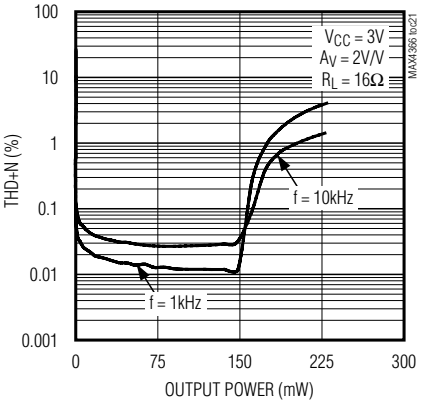
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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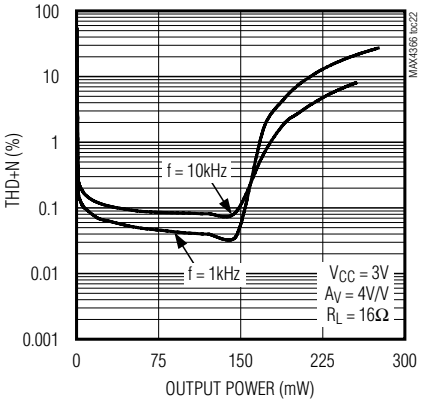

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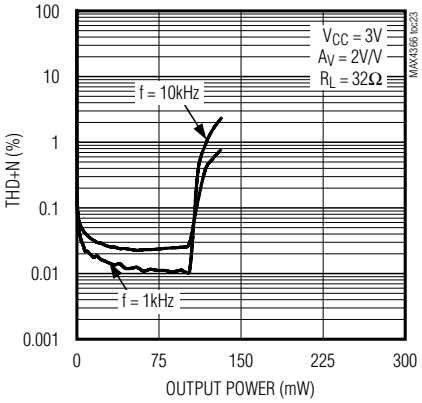
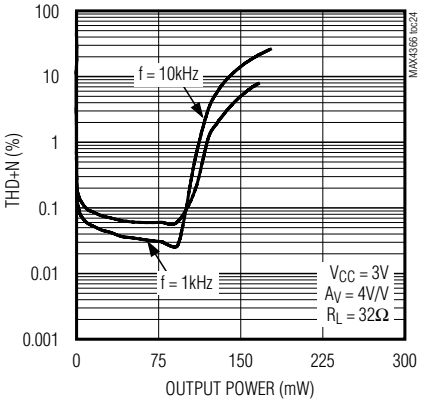
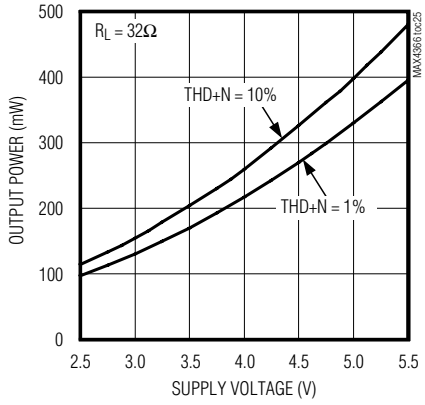


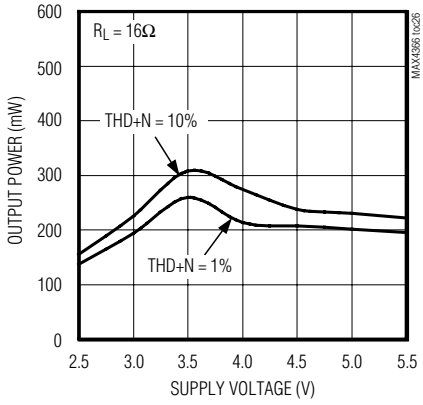
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



OUTPUT POWER vs. SUPPLY VOLTAGE



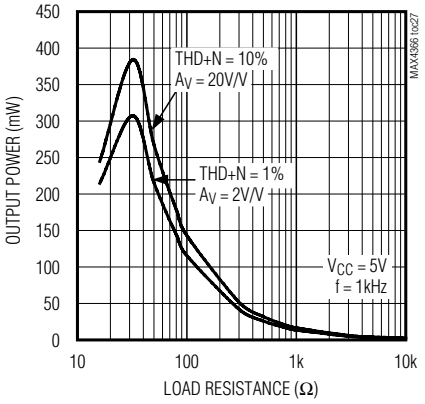
OUTPUT POWER vs. SUPPLY VOLTAGE



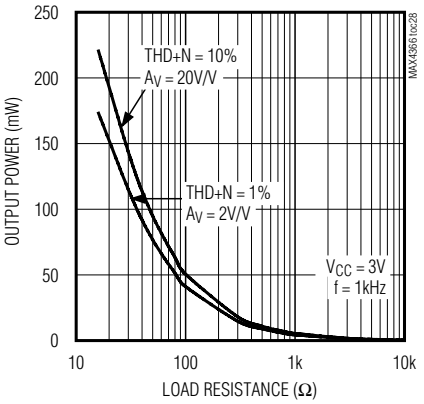
Typical Operating Characteristics (continued)

(Bridge-Tied Load, THD+N Bandwidth = 22Hz to 22kHz, C_{BIAS} = 1µF.)

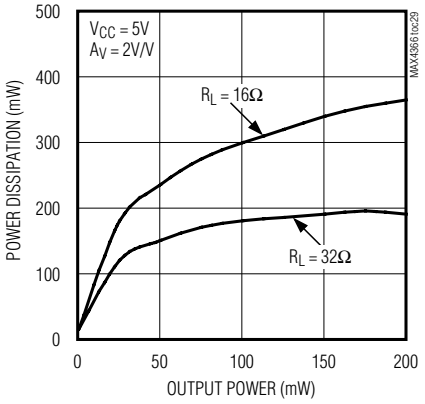
OUTPUT POWER vs. LOAD



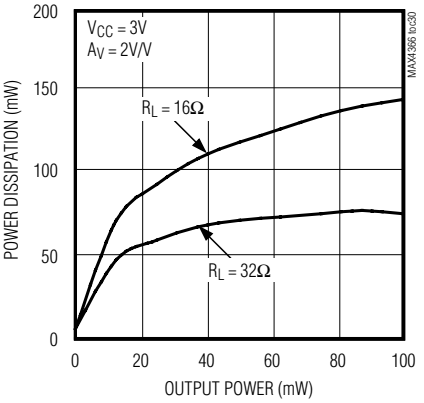
OUTPUT POWER vs. LOAD



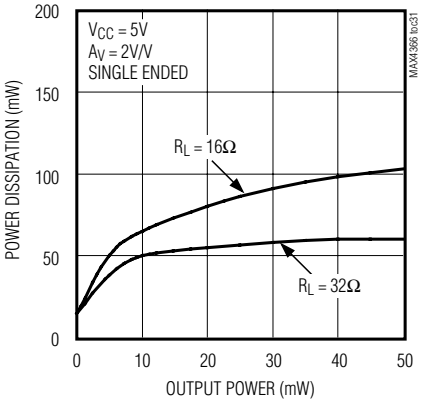
POWER DISSIPATION vs. OUTPUT POWER



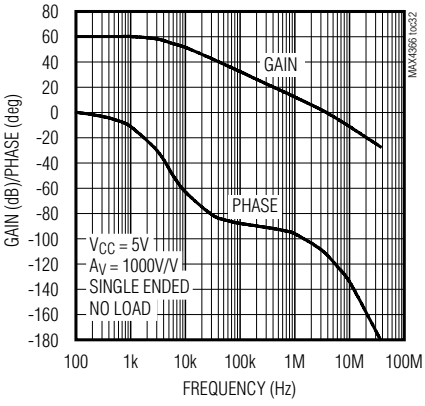
POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



GAIN AND PHASE vs. FREQUENCY

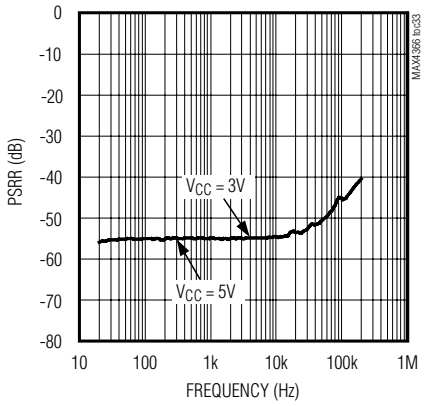


330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

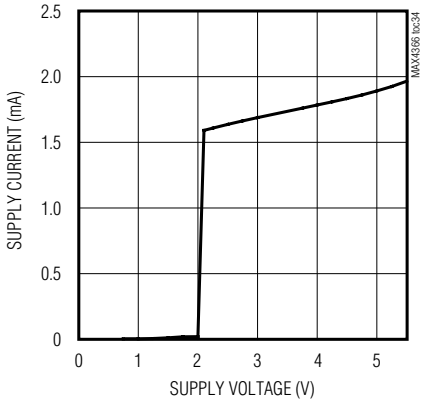
Typical Operating Characteristics (continued)

(Bridge-Tied Load, THD+N Bandwidth = 22Hz to 22kHz, C_{BIAS} = 1µF.)

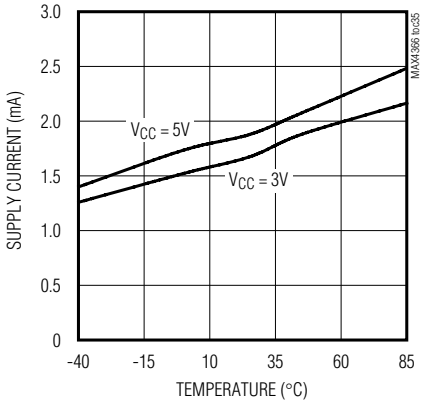
DIFFERENTIAL POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



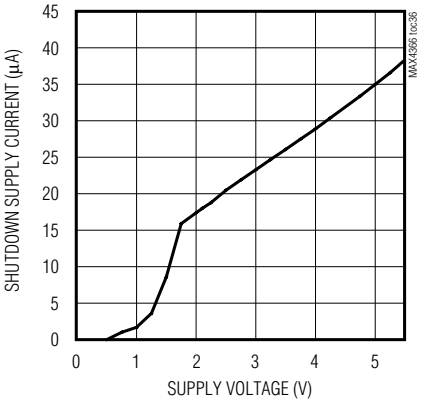
SUPPLY CURRENT vs. SUPPLY VOLTAGE



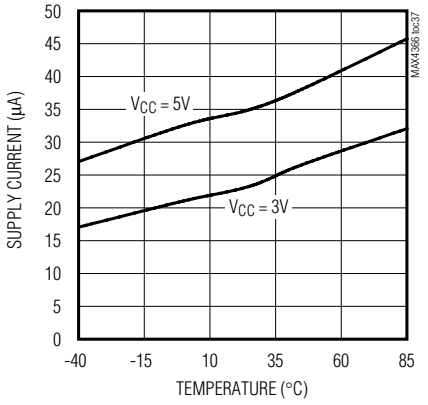
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN/BUMP			NAME	FUNCTION
SOT23/ µMAX	TDFN	UCSP		
1	1	C3	SHDN	Active-High Shutdown. Connect SHDN to GND for normal operation.
2	2	C1	BIAS	DC Bias Bypass. See *BIAS Capacitor* section for capacitor selection. Connect C_{BIAS} capacitor from BIAS to GND.
3	3	A3	IN+	Noninverting Input
4	4	A1	IN-	Inverting Input
5	5	A2	OUT+	Bridged Amplifier Positive Output
6	6	B3	V_{CC}	Power Supply
7	7	B1	GND	Ground
8	8	C2	OUT-	Bridged Amplifier Negative Output
—	EP	—	EP	Exposed Paddle. Connect exposed pad to GND.

Detailed Description

The MAX4366/MAX4367/MAX4368 bridged audio power amplifiers can deliver 330mW into a 32Ω load, or 200mW into a 16Ω load, while operating from a single 5V supply. These devices consist of two high-output-current op amps configured as a bridge-tied load (BTL) amplifier (see *Functional Diagram*). The closed-loop gain of the input op amp sets the single-ended gain of the device. Two external resistors set the gain of the MAX4366 (see *Gain-Setting Resistors* section). The MAX4367/MAX4368 feature internally fixed gains of 2V/V and 3V/V, respectively. The output of the first amplifier serves as the input to the second amplifier, which is configured as an inverting unity-gain follower in all three devices. This results in two outputs, identical in magnitude, but 180° out of phase.

BIAS

The MAX4366/MAX4367/MAX4368 feature an internally generated common-mode bias voltage of $V_{CC}/2$ referenced to GND. BIAS provides both click-and-pop suppression and the DC bias level for the audio signal. BIAS is internally connected to the noninverting input of one amplifier, and should be connected to the noninverting input of the other amplifier for proper signal biasing (*Typical Application Circuit*). Choose the value of the bypass capacitor as described in the *BIAS Capacitor* section.

Shutdown

The MAX4366/MAX4367/MAX4368 feature a 35µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. Pulling SHDN high disables the device's bias circuitry and drives OUT+, OUT-, and BIAS to GND. Connect SHDN to GND for normal operation.

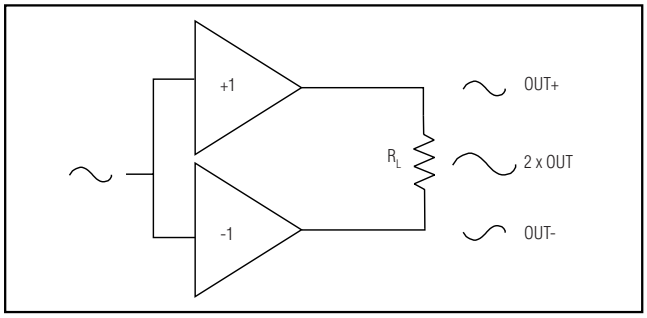


Figure 1. Bridge-Tied Load Configuration

Applications Information

Bridge-Tied Load

The MAX4366/MAX4367/MAX4368 are designed to drive a load differentially, a configuration referred to as bridge-tied load (BTL). The BTL configuration (Figure 1) offers advantages over the single-ended configuration, where one side of the load is connected to ground. Driving the load differentially doubles the output voltage compared to a single-ended amplifier under similar conditions. The differential gain of the device is twice the closed-loop gain of the input amplifier. The effective gain of the MAX4366 is given by:

$$A_{VD} = 2 \times \frac{R_F}{R_{IN}}$$

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

The effective gains of the MAX4367 and MAX4368 are A_{VD} = 2V/V and A_{VD} = 3V/V respectively. Substituting 2 x $V_{OUT(P-P)}$ for $V_{OUT(P-P)}$ into the following equations yields four times the output power due to doubling of the output voltage.

$$V_{RMS} = \frac{V_{OUT(P-P)}}{2\sqrt{2}}$$

$$P_{OUT} = \frac{V_{RMS}^2}{R_L}$$

Since the differential outputs are biased at midsupply, there is no net DC voltage across the load. This eliminates the need for DC-blocking capacitors required for single-ended amplifiers. These capacitors can be large, expensive, consume board space, and degrade low-frequency performance.

Single-Ended Configuration

The MAX4366/MAX4367/MAX4368 can be used as single-ended amplifiers (Figure 2). The gain of the device in single-ended mode is 1/2 the gain in BTL configuration and the output power is reduced by a factor of 4. The single-ended gains of the MAX4367 and MAX4368 are 1V/V and 1.5V/V, respectively. Set the MAX4366 gain according to the *Gain-Setting Resistors* section.

In single-ended mode, the load must be capacitively coupled to the device output to block the half-supply DC voltage from the load (see *Output Coupling Capacitor* section). Leave the unused output floating.

Power Dissipation

Under normal operating conditions, linear power amplifiers like the MAX4366/MAX4367/MAX4368 can dissipate a significant amount of power. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under *Continuous Power Dissipation* or can be calculated by the following equation:

$$P_{DISS(MAX)} = \frac{T_{J(MAX)} - T_A}{\Theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C and T_A is the reciprocal of the derating factor in °C/W as specified in the *Absolute*

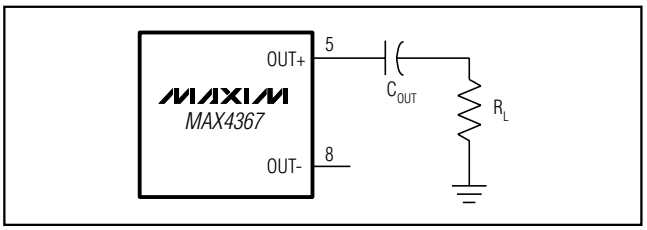


Figure 2. MAX4367 Single-Ended Configuration

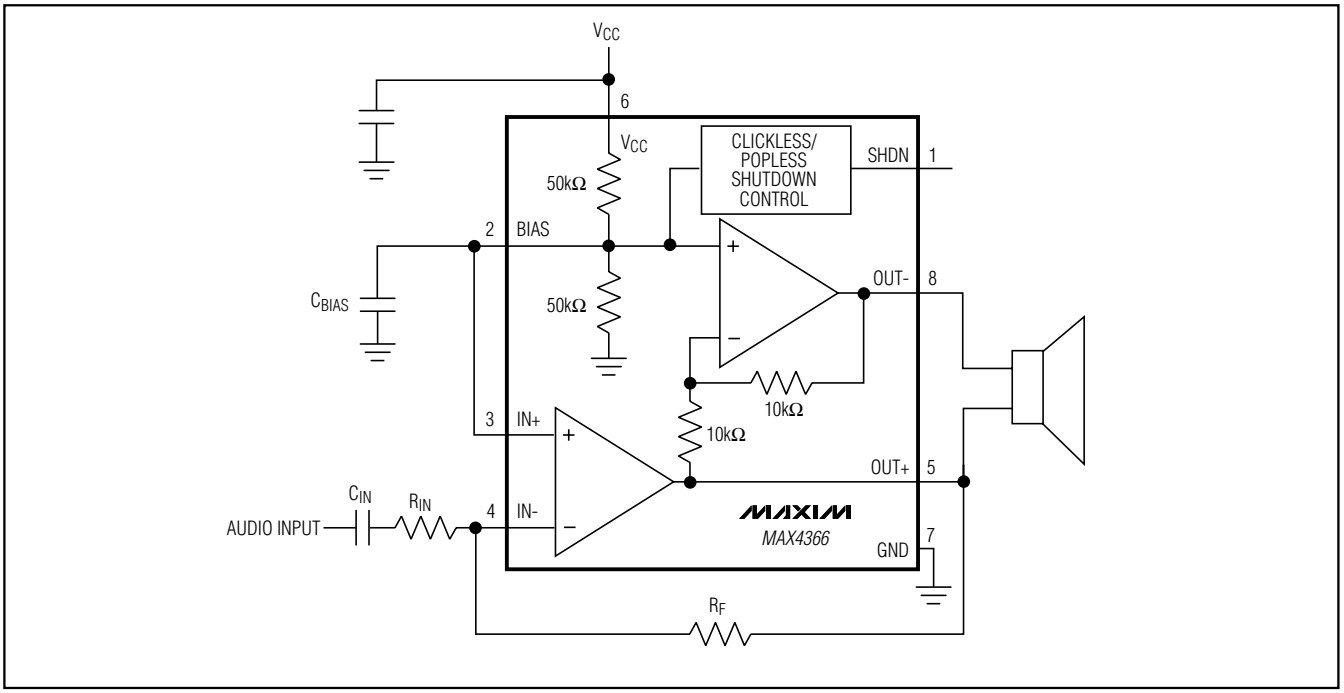


Figure 3. MAX4366 Typical Application Circuit

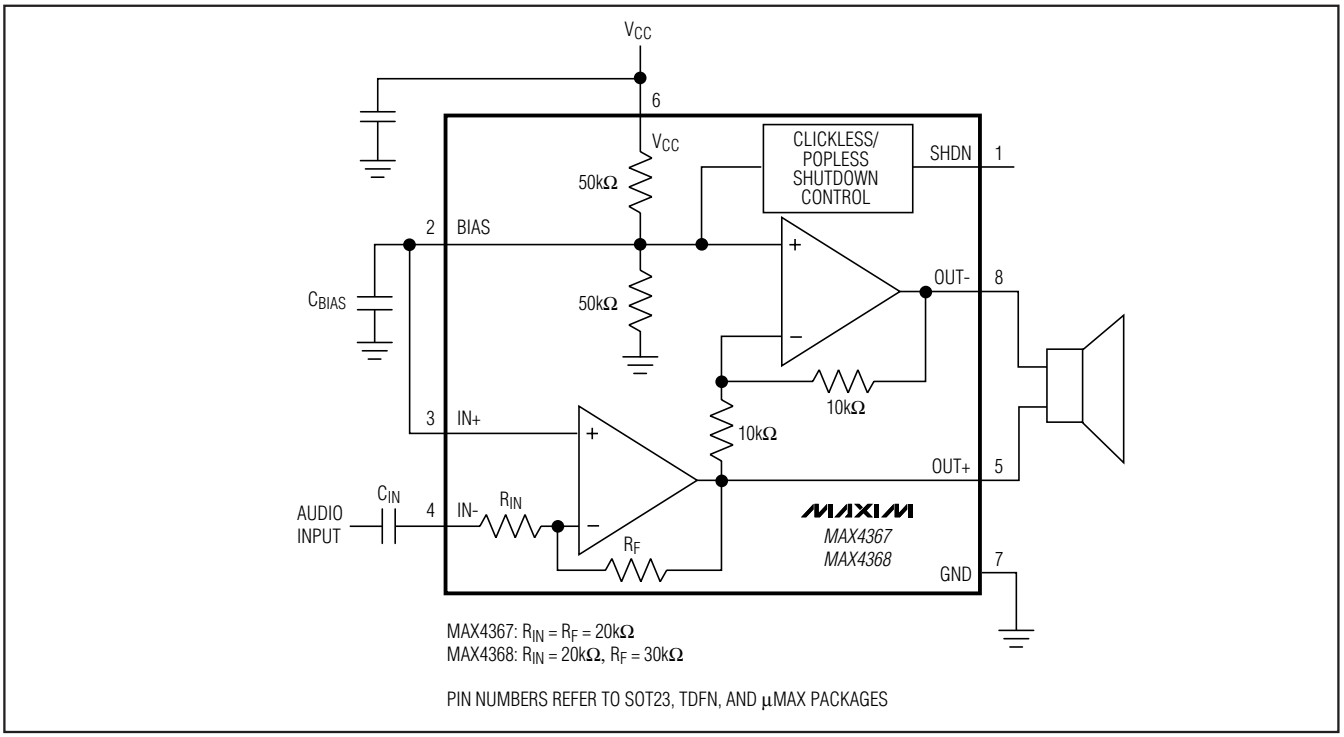


Figure 4. MAX4367/MAX4368 Typical Application Circuit

Maximum Ratings section. For example, Θ_{JA} of a µMAX package is 222°C/W.

The increase in power delivered by the BTL configuration directly results in an increase in internal power dissipation over the single-ended configuration. If the power dissipation exceeds the maximum allowed for a given package, either reduce V_{CC}, increase load impedance, decrease the ambient temperature, or add heat sinking to the device. Large output, supply, and ground traces improve the maximum power dissipation in the package.

Thermal overload protection limits total power dissipation in the MAX4366/MAX4367/MAX4368. When the junction temperature exceeds +165°C, the thermal protection circuitry disables the amplifier output stage. The amplifiers are re-enabled once the junction temperature cools by +10°C. This results in a pulsing output under continuous thermal overload conditions avoiding damage to the port.

Component Selection

Gain-Setting Resistors

External feedback components set the gain of the MAX4366. Resistors R_F and R_{IN} (Figure 3) set the gain of the input amplifier as follows:

$$A_{VD} = 2\left(\frac{R_F}{R_{IN}}\right)$$

The gain of the device in a single-ended configuration is half the gain of the BTL case. Choose R_F between 10kΩ and 50kΩ. The gains of the MAX4367/MAX4368 are set internally (Figure 4).

Input Filter

The input capacitor (C_{IN}), in conjunction with R_{IN} forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

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Choose R_{IN} according to the *Gain-Setting Resistors* section. Choose the C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the low-frequency response of the system.

Other considerations when designing the input filter include the constraints of the overall system, the actual frequency band of interest and click-and-pop suppression. Although high-fidelity audio calls for a flat-gain response between 20Hz and 20kHz, portable voice-reproduction devices such as cellular phones and two-way radios need only concentrate on the frequency range of the spoken human voice (typically 300Hz to 3.5kHz). In addition, speakers used in portable devices typically have a poor response below 150Hz. Taking these two factors into consideration, the input filter may not need to be designed for a 20Hz to 20kHz response, saving both board space and cost due to the use of smaller capacitors.

BIAS Capacitor

The BIAS bypass capacitor, C_{BIAS} improves power-supply rejection ratio and THD+N by reducing power-supply noise at the common-mode bias node, and serves as the primary click-and-pop suppression mechanism. C_{BIAS} is fed from an internal 25kΩ source, and controls the rate at which the common-mode bias voltage rises at startup and falls during shutdown. For optimum click-and-pop suppression, ensure that the input capacitor (C_{IN}) is fully charged (ten time constants) before C_{BIAS}. The value of C_{BIAS} for best click-and-pop suppression is given by:

$$C_{BIAS} \le 10\left[\frac{C_{IN}R_{IN}}{25k\Omega}\right]$$

In addition, a larger C_{BIAS} value yields higher PSRR, especially in single-ended applications.

Output-Coupling Capacitor

The MAX4366/MAX4367/MAX4368 require output-coupling capacitors only when configured as a single-ended amplifier. The output capacitor blocks the DC component of the amplifier output, preventing DC current flowing to the load. The output capacitor and the load impedance form a highpass filter with the -3dB point determined by:

$$f_{-3dB} = \frac{1}{2\pi R_L C_{OUT}}$$

As with the input capacitor, choose the output capacitor (C_{OUT}) such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the low-frequency response of the system.

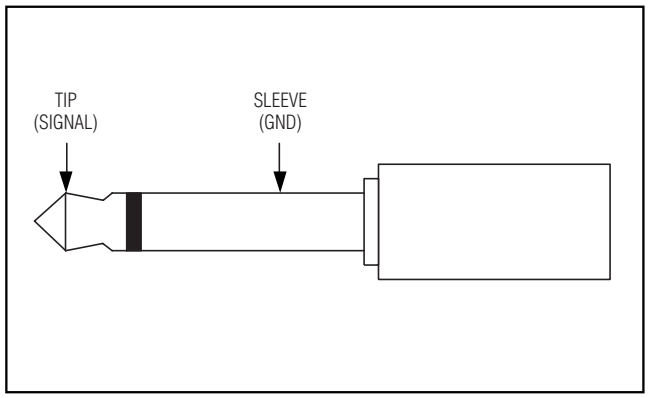


Figure 5. Typical 2-Wire Headphone Plug

In addition to click-and-pop suppression and frequency band considerations, the load impedance is another concern when choosing C_{OUT}. Load impedance can vary, changing the -3dB point of the output filter. A lower impedance increases the corner frequency, degrading low-frequency response. Select C_{OUT} such that the worst-case load/C_{OUT} combination yields an adequate response.

Clickless/Popless Operation

Proper selection of AC-coupling capacitors and C_{BIAS} achieves clickless/popless shutdown and startup. The value of C_{BIAS} determines the rate at which the mid-rail bias voltage rises on startup and falls when entering shutdown. The size of the input capacitor also affects clickless/popless operation. On startup, C_{IN} is charged to its quiescent DC voltage through the feedback resistor (R_F) from the output. This current creates a voltage transient at the amplifier's output, which can result in an audible pop. Minimizing the size of C_{IN} reduces this effect, improving click-and-pop suppression.

Supply Bypassing

Proper supply bypassing ensures low-noise, low-distortion performance. Place a 0.1µF ceramic capacitor in parallel with a 10µF capacitor from V_{CC} to GND. Locate the bypass capacitors as close to the device as possible.

Headphone Applications

The MAX4366/MAX4368 can drive a mono headphone when configured as a single-ended amplifier. Typical 2-wire headphone plugs consist of a tip and sleeve. The tip is the signal carrier while the sleeve is the ground connection (Figure 5). Figure 6 shows the device configured to drive headphones. OUT+ is connected to the tip, delivering the signal to the headphone, while OUT- remains unconnected.

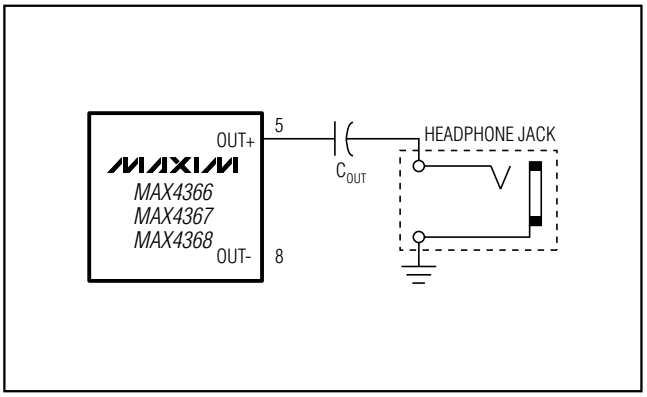


Figure 6. MAX4367 Headphone Application Circuit

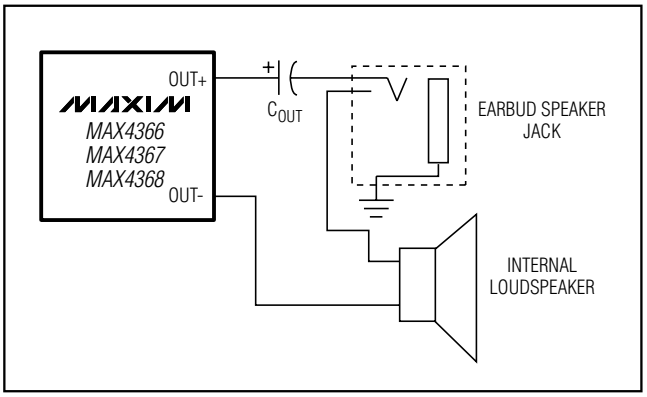


Figure 7. Headset with Internal Speaker Application Circuit

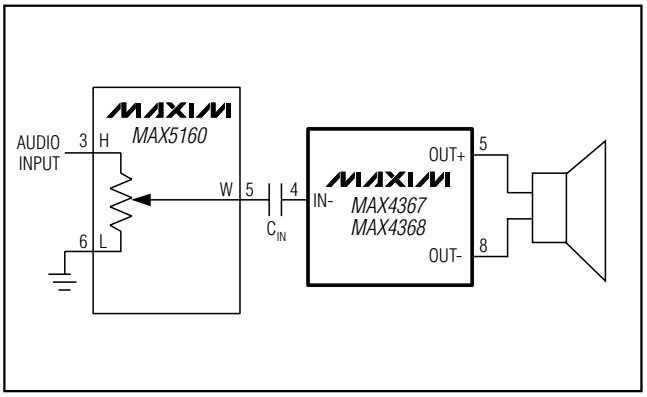


Figure 8. MAX4367/MAX5160 Volume Control Circuit

Wireless-Phone Headset Application

Many wireless telephones feature an earbud speaker/in-line microphone combination for hands-free use. One common solution is to use a BTL amplifier that drives the internal speaker and an earplug jack that mutes the internal speaker by physically disconnecting OUT- when a headset is plugged in (Figure 7). The headset is driven single-endedly, requiring an output-coupling capacitor, C_{OUT}, and resulting in a 4x reduction in output power.

Adding Volume Control

The addition of a digital potentiometer provides simple volume control. Figure 8 shows the MAX4367/MAX4368 with the MAX5160 digital potentiometer used as an input attenuator. Connect the high terminal of the MAX5160 to the audio input, the low terminal to ground and the wiper to C_{IN}. Setting the wiper to the top position passes the audio signal unattenuated. Setting the wiper to the lowest position fully attenuates the input. Use the 100kΩ version of the MAX5160.

Layout Considerations

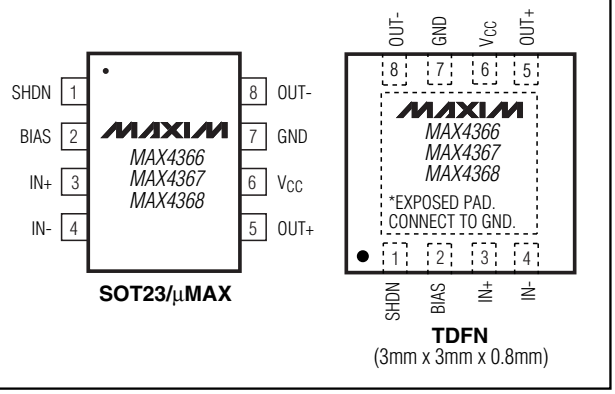
Good layout improves performance by decreasing the amount of stray capacitance and noise at the amplifier's inputs and outputs. Decrease stray capacitance by minimizing PC board trace lengths, using surface-mount components and placing external components as close to the device as possible.

UCSP Considerations

For general UCSP information and PC layout considerations, please refer to the Maxim Application Note: UCSP–A *Wafer-Level Chip-Scale Package.*

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

Pin Configurations (continued)



Ordering Information (continued)

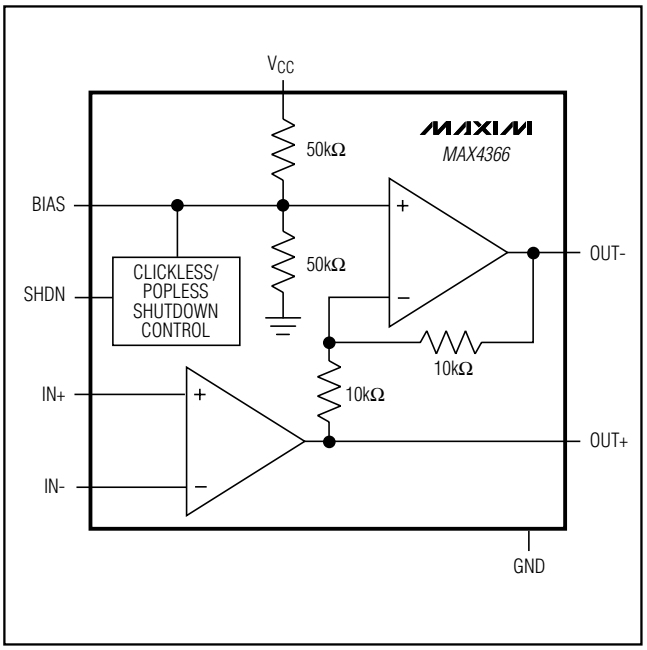
PART	TEMP RANGE	PIN/BUMP-PACKAGE	TOP MARK
MAX4367EBL-T	-40°C to +85°C	8 UCSP-8	AAL
MAX4367EKA-T	-40°C to +85°C	8 SOT23-8	AAIP
MAX4367EUA	-40°C to +85°C	8 µMAX	—
MAX4367ETA-T	-40°C to +85°C	8 TDFN-8-EP*	AGA
MAX4367ETA+T	-40°C to +85°C	8 TDFN-8-EP*	+AGA
MAX4368EBL-T	-40°C to +85°C	8 UCSP-8	AAM
MAX4368EKA-T	-40°C to +85°C	8 SOT23-8	AAIQ
MAX4368EUA	-40°C to +85°C	8 µMAX	—
MAX4368ETA-T	-40°C to +85°C	8 TDFN-8-EP*	AGB
MAX4368ETA+T	-40°C to +85°C	8 TDFN-8-EP*	+AGB

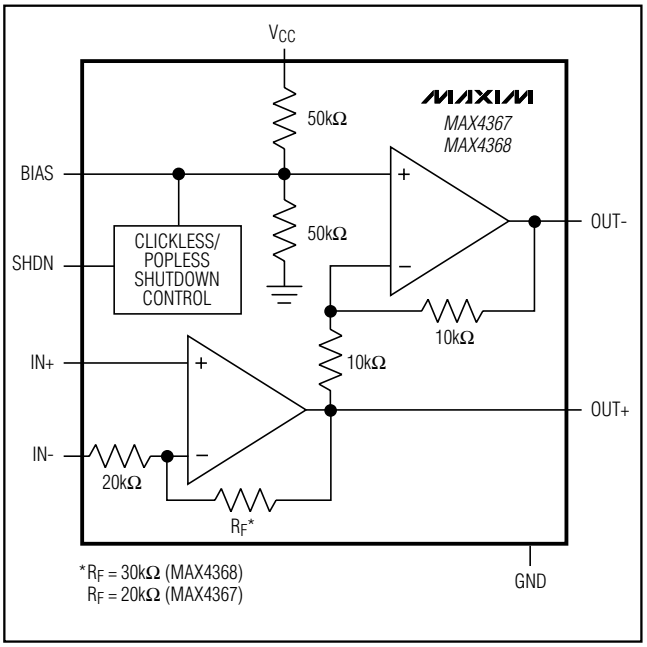
**EP = Exposed paddle.*
+Denotes lead-free package.

Selector Guide

PART	GAIN
MAX4366	External
MAX4367	2V/V
MAX4368	3V/V

Functional Diagrams





Chip Information

TRANSISTOR COUNT: 669

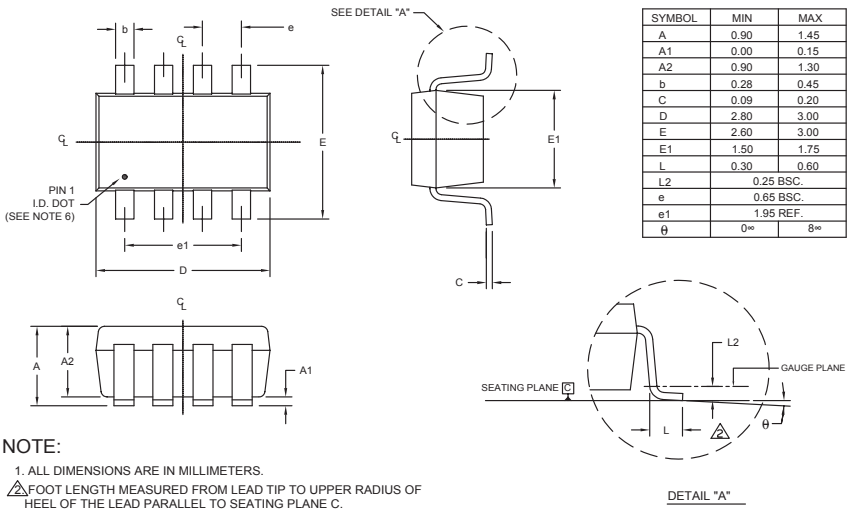
PROCESS: Bipolar

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L .EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.30	0.60
L2	0.25 BSC.	
e	0.65 BSC.	
e1	1.95 REF.	
θ	0∞	8∞

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED FROM LEAD TIP TO UPPER RADIUS OF HEEL OF THE LEAD PARALLEL TO SEATING PLANE C.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. COPLANARITY 4 MILS. MAX.
6. PIN 1 I.D. DOT IS 0.3 MM ÿ MIN. LOCATED ABOVE PIN 1.
7. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEAD TIP.
8. MEETS JEDEC MO178.

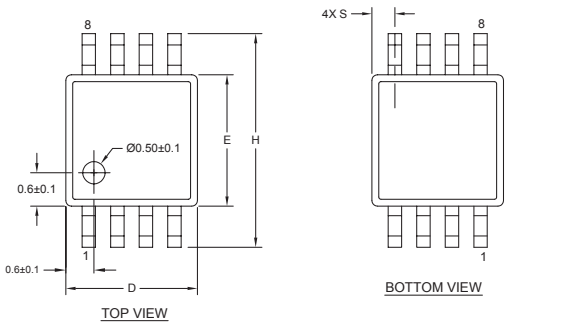
DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT-23, 8L BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0078	D	1/1

8LUMAXD.EPS



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-AA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

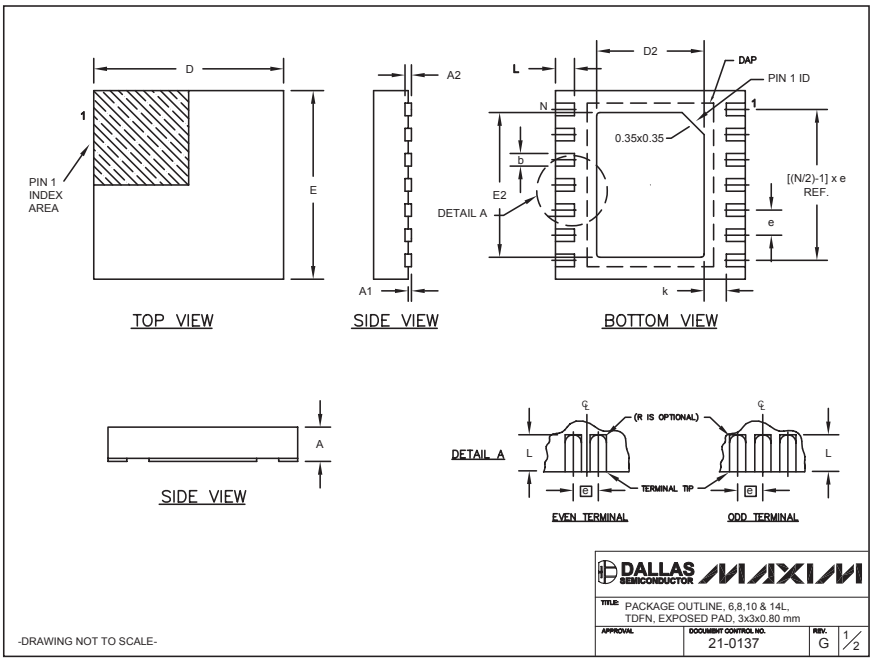
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0036	J	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS

PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	----	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. G
2/2

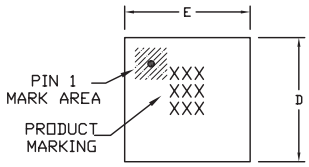
Note: *MAX4366/MAX4367/MAX4368 Package Code: T833-1*

330mW, Ultra-Small, Audio Power Amplifiers with Shutdown

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

9LUCSP, 3x3.EPS

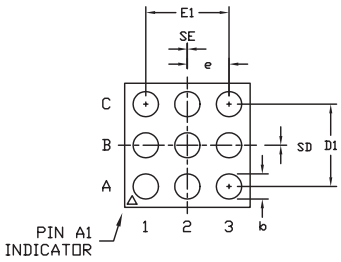


TOP VIEW

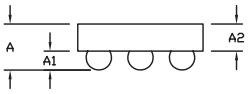
COMMON DIMENSIONS	
A	0.62±0.05–0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.60±0.05	1.60±0.05	A2, B1, B2, B3, C2

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	J	1/1

-DRAWING NOT TO SCALE-

Note: *Bump B2 is not present.*